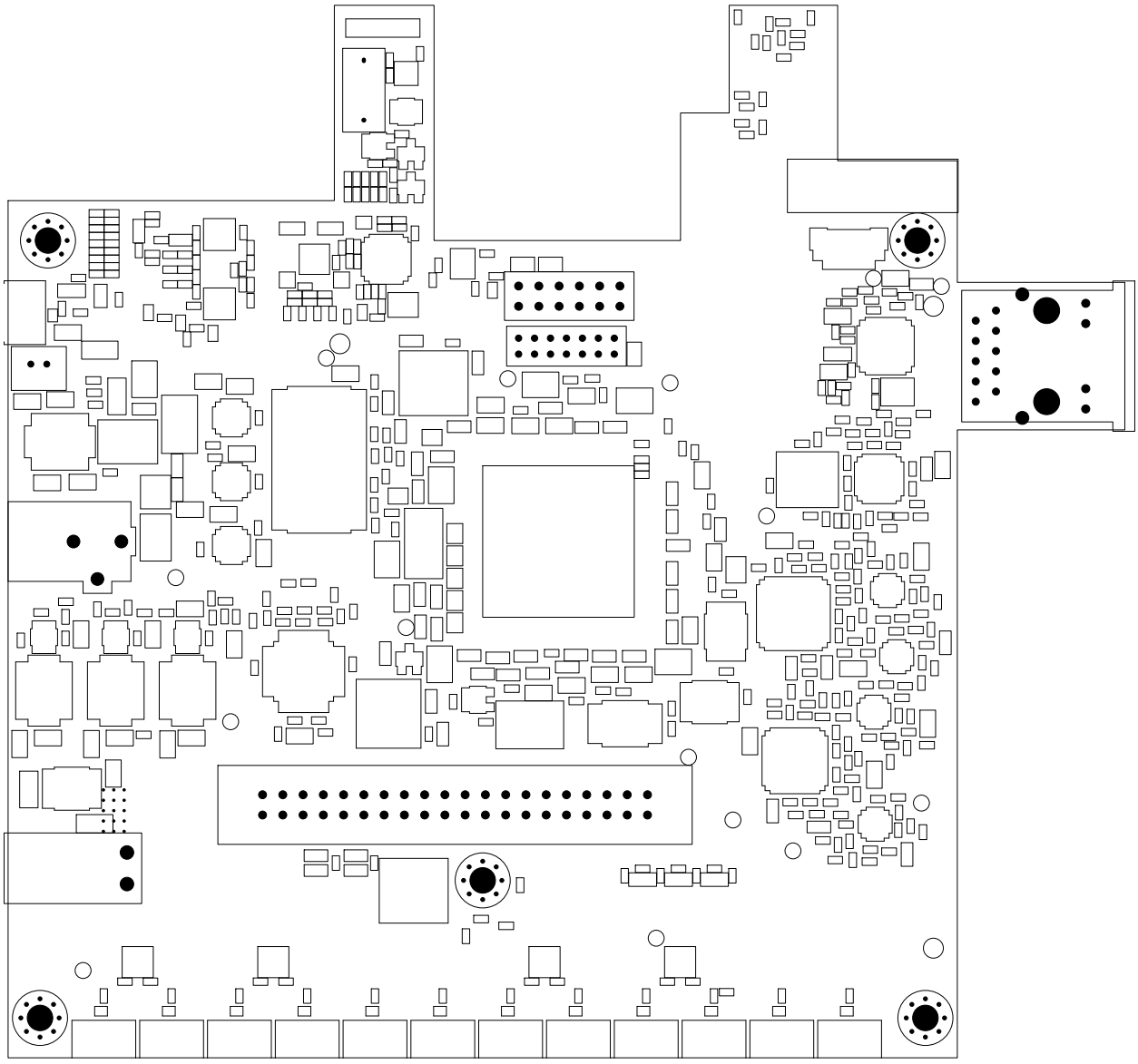
TECHNICAL DOCUMENTATION

KV260-IAS2RF

RF front-end adapter for the AMD Kria KV260

Radar (AERIS-10, 10.5 GHz) and wideband SDR · Artix-7 front-end FPGA · 8-layer PCB



Top view: board outline and component courtyards (KiCad), 140 × 132 mm

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Platform Baseline Summary

PCB & Stackup:	8-layer JLC08161H-2116C (140 x 132 mm, 0 DRC / 0 ERC, openEMS S11 = -30.9 dB @ 1 GHz)
High-Speed Link:	2-lane IAS1 LVDS (2.0-2.5 Gb/s UL, 1.0 Gb/s DL) + dedicated-pin 1000BASE-T RTL8211FSI UDP
Artix-7 (XC7A50T):	25,279 LUTs (77.5 %), 28,970 FFs (44.4 %), 18.0 BRAM36 eq., 119 DSPs (99.2 %), WNS = +0.007 ns
Kria K26 (XCK26):	Full BD: 53,336 LUTs (45.5 %), 46,896 FFs (20.0 %), 44.0 BRAM36 eq., 229 DSPs (18.3 %), WNS = +1.043 ns
RF Missions:	AERIS-10 X-Band Radar (10.5 GHz, 20 km, 8x ADAR1000) + Wideband SDR (HF to 30 MHz, VHF/UHF 25 MHz to 1.1 GHz on J961)
HF input:	J951: 30 MHz 7th-order elliptic anti-alias filter on the board, >= 60 dB from 50 MHz; no RF switch in the path
Thermal & Mech.:	Enclosure v2 (50x15 mm filtered lid fan, HS1-HS3, 50 g FEA BGA <= 96 ue): rated 56 C ambient with the stock KV260, 71 C with a K26I SOM
XSim Co-Sim:	Dual-FPGA Artix-7 + PCB channels + K26 PL + RTL8211FSI/GEM3 UDP end-to-end PASS (S1..S6)

Compendium Structure

- Part I: Board Overview — 2 item(s)
- Part II: Dual-FPGA Gateware & XSim Verification — 10 item(s)
- Part III: Schematic Subsystem Specifications — 12 item(s)
- Part IV: 8-Layer PCB Layout & Signal/Power Integrity — 4 item(s)
- Part V: Mechanical Integration, Heatsinks & Enclosure v2 — 3 item(s)
- Part VI: Fabrication & Costing — 3 item(s)
- Appendix A: Vector Vivado FPGA Silicon Floorplans & Schematics — 5 item(s)
- Appendix B: Vector Heatsink Mechanical Map — 1 item(s)
- Appendix C: Vector 14-Page Hierarchical KiCad Schematic — 14 item(s)
- Appendix D: Vector 10-Sheet 8-Layer PCB Layout — 10 item(s)
- Appendix E: Vector PSU Board Schematic & 4-Layer Layout — 6 item(s)

Part I: Board Overview

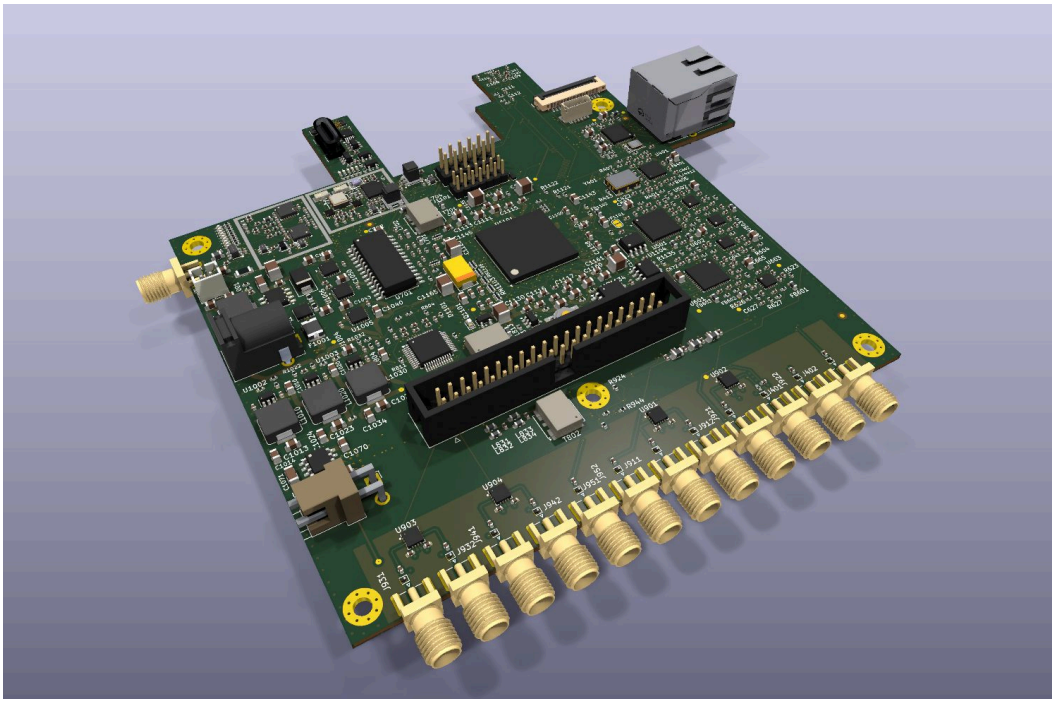
2 technical document(s)

Source: README.md

KV260-IAS2RF: an RF front-end carrier for the AMD Kria KV260

Status (20 November 2026, Rev08.1): schematic and layout complete, on 8 layers. The board is fully routed, with zero DRC errors and zero schematic-parity problems. It has not been fabricated, and no hardware has been validated. The hardware, dual-FPGA Vivado gateware, Enclosure v2 cooling, and full-system co-simulation are complete (**Status**).

> **Current `main` Hardware & Gateware Baseline: 8-layer `JLC08161H-2116C` RF front-end adapter PCB with dedicated-pin 1000BASE-T Ethernet (`U1201` `RTL8211FSI`) + dual-lane `IAS1` (`~2.94 Gb/s` aggregate)**, failover in the dual-FPGA Vivado 2026.1 gateware (**docs/FPGA_GATEWARE.md**), `5 V` header `J1002` for filtered Enclosure v2 active cooling (**ENCLOSURE.md**), and `0` KiCad DRC / parity errors. Historical design evolution from initial drafts is archived in **docs/history/README.md** and tagged `rev01` to `rev08.1`.



The board, 3D render

Explore it in 3-D: pablosoage.github.io/kv260-ias2rf. Turn the board, the KV260 and the enclosure, open the case, hover a part to see what it is and what it does, and look at the board layer by layer.

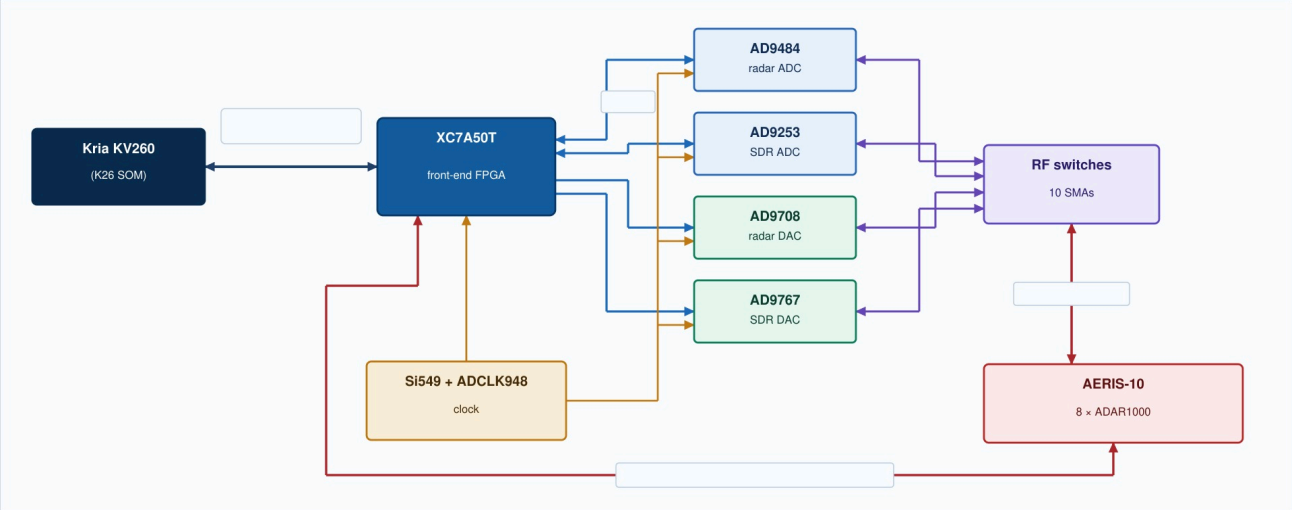
An adapter board for the **AMD Kria KV260 Vision AI Starter Kit**. It plugs into the KV260's IAS1 camera connector and carries the converters, a common clock and a front-end FPGA. It serves two signal chains:

- **Software-defined radio**: HF to 30 MHz directly; FM, airband, VHF/UHF amateur bands, PMR446 and ADS-B through the on-board VHF/UHF front end on its own SMA, 30 MHz to 3 GHz (**RX_VU_SPEC**). Receive, and transmit on the bands a licence covers.
- **Radar at 10.5 GHz**: the IF of the X-band chain from the open AERIS-10 / PLFM_RADAR project, with ADAR1000 beamforming. The 10.5 GHz chain itself is reused from AERIS-10, not redesigned here. The board is sized for 8 ADAR1000s (32 channels), so it covers both the Nexus variant (4 chips) and the Extended one (8 chips).

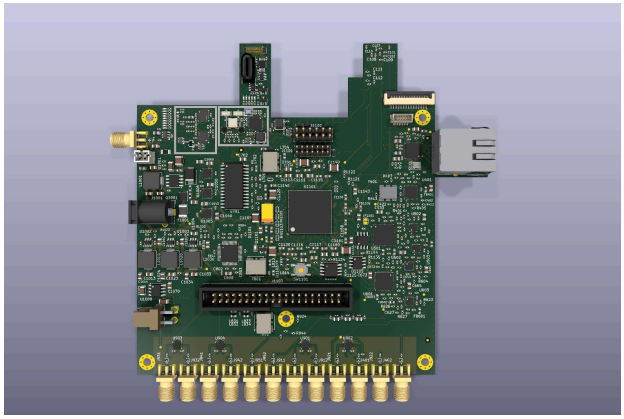
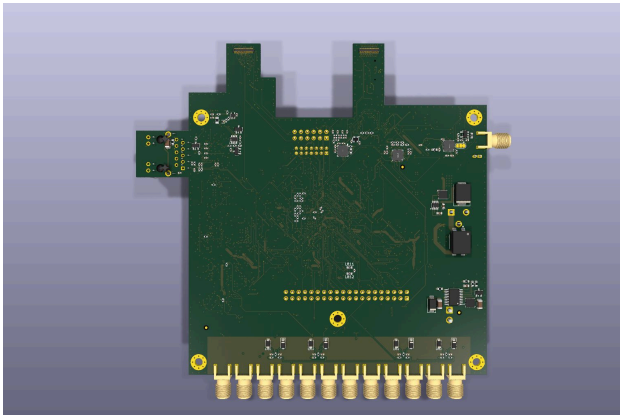
> ### The finding that shapes the whole project
>
> The **IAS0 (J7) connector on the KV260 does not reach the programmable logic**: its MIPI lanes run into an AP1302 ISP soldered on the carrier card. Only **IAS1 (J8)** is wired straight to the SOM. On top of that, **the KV260 has no 40-pin Raspberry Pi header** (J9 is a 15-pin camera connector), and **the GTH transceivers are not exposed**.
>
> The real I/O budget between a KV260 and an external board is **8 differential pairs and about 14 single-ended signals**. That is why the board has its own FPGA. The evidence and sources are in **docs/BLOCKERS_AND_RISKS.md**.

The board at a glance

Stackup	8 layers, JLCPCB `JLC08161H-2116C`: `L1 SIG – L2 GND – L3 SIG – L4 PWR (split) – L5 GND – L6 SIG – L7 GND – L8 SIG` (**LAYOUT §3**)
Parts	785 fitted, the same count as the BOM and the placement file: 620 on the top face and 165 on the bottom (the Hirose connectors, the LVDS terminations and VCCINT caps under the FPGA, the switches' bias parts, the input protection)
Front-end FPGA	Xilinx XC7A50T-2FTG256I (the same part as AERIS-10) with a 128 Mb QSPI flash, plus JTAG
Radar ADC	AD9484, 8 bit: 400 MSPS with the 400 MHz master clock (radar), 500 MSPS with the 500 MHz one (the D2 path), driven by two cascaded AD8352s
SDR ADC	AD9253, 14 bit, two channels at 62.5 MSPS (one LVDS lane each)
Radar DAC	AD9708, with reconstruction filter and balun
SDR DAC	AD9767, dual 14 bit, two output chains
Clock	Si549 programmable XO (400 or 500 MHz, GPS-disciplinable) into an ADCLK948 LVPECL fan-out
RF routing	Four M3SWA2-34DR+ SPDT switches and ten edge SMAs, plus two clock SMAs and the VHF/UHF antenna SMA `J961` on the back wall: thirteen in all. The HF ports J951 (receive, through an on-board 30 MHz 7th-order elliptic anti-alias filter) and J952 (transmit) have no switch in their path (**SIGNAL_INTEGRITY §9.9**)
Link to the Kria	IAS1 (Hirose BM20B), five LVDS pairs at up to 1 Gb/s each, AC-coupled; the Pmod J2 for control
Ethernet	Gigabit RJ45 through an RTL8211FSI SGMII PHY on its own FPGA pins, so it runs alongside IAS1 (**CONTROL_SPEC §8**)
To AERIS-10	2×20 IDC ribbon for eight ADAR1000s
Power	12 V single power entry (`J1001` via `L1004` to adapter + `U1010`/`J1004` 3.0 A output to KV260 `J12`); buck and LDO tree for 5 V, 3.3 V, 2.5 V, 1.8 V and 1.0 V, plus -3.3 V for the switches (**POWER_SPEC §1.4**, **BOARD_MANUAL §6**). In a vehicle, the **PSU board** feeds both boards from the battery



System Architecture & Signal-Chain Flowchart

Top	Bottom
	
Top	*Bottom*

The renders come from KiCad. The shield frames' walls show only their pads; the debug USB-C `J1501` has a model drawn from its maker's drawing, since no library has one (**3D_MODELS**).

<!-- board-manual:start -->

Board manual

Every connector, LED, switch and chip, numbered as in the drawing; the bottom side, the switches, the chips, troubleshooting and typical uses are in **docs/BOARD_MANUAL.md**. Generated with the tables from the board file by `_work/manual/board_manual.py`.



Board manual, top side

No.	Ref	Side	Name	What it is for
1	`J101`	bottom	BM20B(0.8)-34DP	IAS1 to the KV260 (its `J8`), underneath: five LVDS pairs at up to 1 Gb/s each (three data lanes, two clocks), the housekeeping I2C (temperature sensor, ID EEPROM) and the FPGA's interrupt. The board's only data link to the Kria
2	`J102`	bottom	BM20B(0.8)-34DP	IAS0 to the KV260 (its `J7`), underneath. Every pin is passed through to `J103`; the board uses none
3	`J103`	top	BM20B(0.8)-34DS-0.4V(51)	IAS0 pass-through receptacle on the tongue's top face, pin for pin with `J102`: an IAS camera module plugs in here as it would on the carrier

No.	Ref	Side	Name	What it is for
4	J401	top	CLK_REF_IN	Reference clock input (SMA) to the ADCLK948, 0.4-3.4 V p-p differential range, 50 ohm on chip. Leave open to run from the on-board Si549
5	J402	top	CLK_OUT	Clock output (SMA), ADCLK948 Q3, LVPECL: to share the master clock with an instrument
6	J911	top	SDR_RX_A	SDR receive A (SMA): through SW1's default throw to the AD9253 channel A. Full scale about -2.4 dBm; DC-blocked
7	J912	top	AERIS_IF_A	Radar IF into the 14-bit AD9253 (SMA), through SW1's second throw
8	J921	top	AERIS_IF	Radar IF from AERIS-10 (SMA): through SW2's default throw to the AD9484 (400 or 500 MSPS with the master clock). Full scale about -17.6 dBm
9	J922	top	SDR_RX_WB	Wideband SDR receive (SMA), SW2's second throw. Not connected as built: C926 is not fitted and the VHF/UHF front end takes the throw (C927); swap the two 0402s to use this port
10	J931	top	SDR_TX_A	SDR transmit A (SMA): AD9767 DAC1 through SW3's default throw, 10 mA full scale
11	J932	top	AERIS_TX_A	Radar chirp from the 14-bit AD9767 DAC1 (SMA), SW3's second throw
12	J941	top	AERIS_TX	Radar chirp to AERIS-10 (SMA): the AD9708 through SW4's default throw, 20 mA full scale into a 2:1 balun
13	J942	top	SDR_TX_WB	Wideband SDR transmit from the AD9708 (SMA), SW4's second throw
14	J951	top	SDR_RX_C	HF receive (SMA), no switch: a 30 MHz 7th-order elliptic low-pass, then the AD9253 channel B. Full scale about -3.0 dBm. The default HF input
15	J952	top	SDR_TX_C	HF transmit (SMA), no switch: AD9767 DAC2. The default HF output
16	J961	top	VU_ANT	VHF/UHF antenna (SMA, back wall): the Rev08 front end, direct 30-170 MHz and converted from 300 MHz to 3 GHz (170-300 MHz not covered: the converter's 300 MHz high-pass, AUDIT_Rev08 R1), into the AD9484 through SW2. Bias tee for an active antenna (off at power-up, 5 V or 3.3 V by JP1301, 125 mA limit; prefer 3.3 V where the antenna accepts it). Full scale -52 dBm at maximum gain, up to about +2 dBm with the attenuator and the LNA bypassed. No limiter: keep it away from a transmitter on the same vehicle (+25 dBm destroys the LNA)
17	J1001	top	12V IN	12 V input, barrel jack (CUI PJ-102AH, 5 A). Single power entry for both boards (L1004 on both lines): feeds the adapter (11.7 W typical, 13.4 W / 1.12 A worst; F1001 2 A PTC, 18.3 V OVP) and the KV260 via U1010/J1004 (3.0 A / 3.19 A max limit; 1.89 A typical, 4.12 A rated, 4.31 A worst combined). See POWER_SPEC section 1.4 and section 6
18	J1002	top	FAN 5V	Enclosure fan, JST PH 2-pin: pin 1 +5 V (0.5 A PTC F1002), pin 2 GND
19	J1004	top	B2PS-VH	12 V output to the KV260's J12 (JST VH 2-pin right-angle, 10 A: pin 1 +12V_KV, pin 2 GND): protected by U1010 (8.0 V UVLO, 14.4 V OVP, 3.0 A limit via R1043 6.04 kohm, -60 V reverse); see section 6
20	J1101	top	JTAG 2x7 2mm	Xilinx JTAG for the XC7A50T and its flash (Platform Cable or any 2 mm 14-pin JTAG adapter)
21	J1102	top	Pmod	Pmod from the KV260's J2 (cable): SPI to the FPGA's register file, beam strobe, PPS and the debug UART. Pin by pin below
22	J1103	top	AERIS ADAR	AERIS-10 beam-steering ribbon (2x20 IDC): the ADAR1000 SPI and its control lines
23	J1201	top	HR911130C	Gigabit Ethernet (RJ45, magnetics and LEDs inside), from the RTL8211FS over SGMII to the FPGA: the board standalone
24	J1501	top	TYPE-C-31-E-17	Debug USB-C (vertical, on the tongue): the FPGA's console through a CH340X, 115,200 baud 8N1, powered from the cable. Lid off
25	J1502	top	FPC-1.0FX-15PWCR-H20	GPS PPS and the vehicle CAN to the KV260's J9 (Raspberry Pi camera connector) by a 100 mm 15-way 1 mm FFC, either cable type: the pulse reaches J9 pin 12, a PL pin (kria_pps); CAN TX leaves on J9 pin 6 and RX comes back on pin 8 (PS CAN1, R5F core 1)
26	J1503	top	BM06B-SRSS-TB	GPS receiver and vehicle CAN, JST-SH 6-pin, vertical, the plug from above: 1 GND, 2 CANL, 3 CANH, 4 GND, 5 PPS in (3.3 V), 6 +3.3 V out (0.2 A PTC) (no termination: it taps the car's bus)

No.	LED	Meaning when lit
30	D1501 CFG green	FPGA configured and the clock sequencer finished
30	D1502 CLK yellow	Master clock mode: on 500 MHz, off 400 MHz
30	D1503 LINK green	IAS1 link to the Kria trained
30	D1504 ADCR red	The radar ADC (AD9484) clipped since the last read (sticky)
30	D1505 ADCS red	The SDR ADC (AD9253) clipped since the last read (sticky)
30	D1506 LO green	The RFFC5072 synthesiser is locked
30	D1507 TX red	A DAC is driving an SMA
30	D1508 ERR red	Any sticky error: CRC, FIFO overflow, I2C no-acknowledge, over-temperature

No.	LED	Meaning when lit
30	`D1509` HB blue	Heartbeat: flickers with every line the FPGA prints on the debug UART, once a second
31	`D1520` +12V green	+12V present (after the input protection)
31	`D1521` +5V0 green	+5V0 present
31	`D1522` +3V3_D green	+3V3_D present
31	`D1523` +1V8_D green	+1V8_D present (switched from +3V3_D by `Q1520`)
31	`D1524` +1V0 green	+1V0 (FPGA core) present (switched from +3V3_D by `Q1521`)
32	`D1101` green	DONE: the FPGA has loaded a bitstream

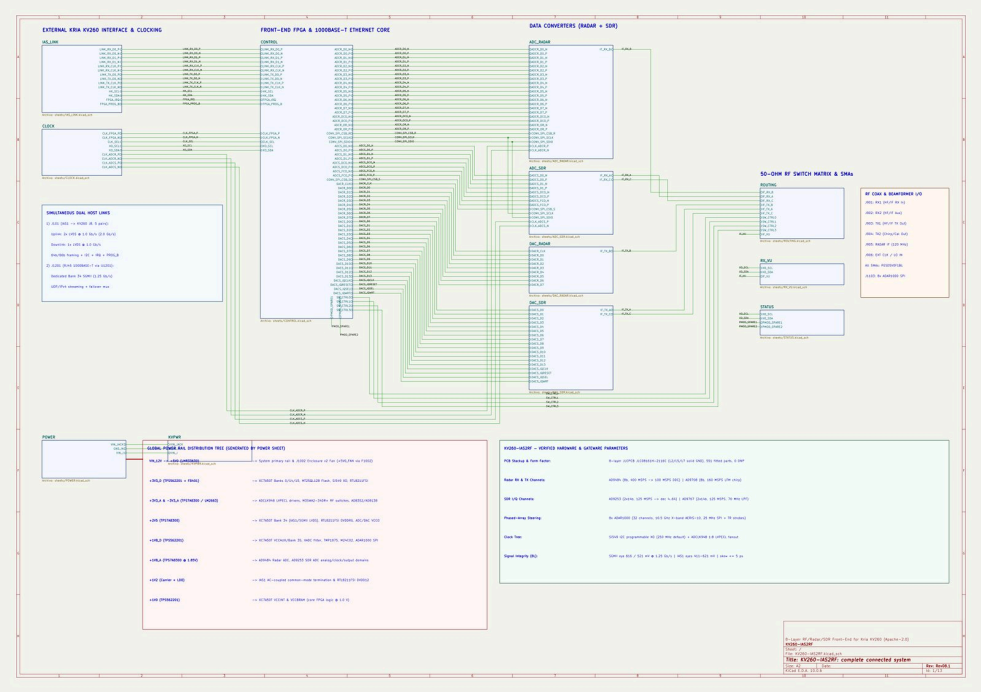
<!-- board-manual:end -->

Schematics and layout

The PDFs and the high-resolution files are not in the repository: they are assets of the `rev08.1` release (each older tag has its own), and the books open in the online reader.

- **Schematic, all 12 sheets including full wired overview (PDF)** · High-res SVGs & 4K PNGs (**index**)
- **Layout, all 8 copper layers + combined + transparent tracks (PDF)** · Per-layer SVGs & 4K PNGs (**index**)
- **Complete Project Documentation Book (PDF)**, and the same book lighter, with the normal renders instead of the 4K ones: Lite PDF (both reproducible locally via `export_documentation.py`, `--lite` for the second)
- KiCad 10 sources: `KV260-IAS2RF.kicad_pro`, the root schematic and `sheets/` (twelve hierarchical sheets), the 8-layer board `KV260-IAS2RF.kicad_pcb`, and custom libraries in `symbols/` and `footprints/`. Every title block carries the revision, Rev08.1; the original Allied Vision Altium project the board started from stays in `PCB/` under its own name (**docs/history/README.md**).

Sheet	Contents	Specification
IAS_LINK	The Hirose connectors, AC coupling and terminations of the link	**IAS_LINK_SPEC**
CLOCK	Si549, reference select and LVPECL fan-out	**CLOCK_SPEC**
ADC_RADAR	AD9484 and its two AD8352 drivers	**ADC_RADAR_SPEC**
ADC_SDR	AD9253, two channels	**ADC_SDR_SPEC**
DAC_RADAR	AD9708, filter and balun	**DAC_RADAR_SPEC**
DAC_SDR	AD9767 in interleaved mode, two output chains	**DAC_SDR_SPEC**
ROUTING	Four RF switches and the SMAs	**ROUTING_SPEC**
CONTROL	The front-end FPGA: banks, configuration, Pmod, AERIS ribbon, housekeeping	**CONTROL_SPEC**
POWER	The power tree	**POWER_SPEC**
RX_VU	VHF/UHF front end (`J961`), LNA, preselectors, RFFC5072 and IF chain	**RX_VU_SPEC**
STATUS	Status LEDs, TCA6416A expanders, debug USB-C UART, GPS PPS and vehicle CAN	**BOARD_MANUAL**
KVPWR	KV260 single-entry power feed: `J1004`, `L1004` CMC, `U1010` 3.0 A eFuse	**POWER_SPEC**



Full wired circuit overview (all sheets connected)

> *High-resolution vector PDF (*`sch/FULL_CIRCUIT.pdf` *in the high-res archive) and 4K schematic PNGs are indexed in* ***docs/img/highres/README.md****.*

Status

Check	Result
ERC	0 errors; 7 warnings, all explained: configuration and XADC pins tied to power on purpose (**CONTROL_SPEC §5**)
DRC, zones refilled	**0 errors, 0 unrouted connections, 0 schematic-parity problems** on the 8-layer `JLC08161H-2116C` board (`local/kvpwr`, 785 BOM parts; checked by `make_fab.py`)
Signal and power integrity	Full-wave openEMS + ngspice verification (**SIGNAL_INTEGRITY.md**): SMA launch `S11 = -30.9 dB` at 1 GHz (`-13.7 dB` at 3 GHz) with ESD diode, LVDS eyes within `1–26 mV` of ideal except `LINK_RX_D0` (`-52 mV`), worst intra-pair skew `9 ps`, `VCCINT` impedance `41 / 63 mΩ` (`target 120 mΩ`), ESD protection on every SMA, Pmod and JTAG, GND via within `3 mm` of all `89` LVDS layer changes
Planes	L2, L5, and L7 carry solid ground; L4 carries split power islands (`_work/layout/planechk.py`)
Dual-FPGA gateware	Both designs place, route and meet timing in Vivado 2026.1; utilisation and slack in the **FPGA figures** table, generated from the Vivado reports. They pass the end-to-end XSim suite (`tb_system`, `S1..S6`) and the G-8 simulations (**FPGA_GATEWARE.md**)
Final RF review (15 Nov)	Five limits found (**SIGNAL_INTEGRITY §9.8**) and addressed (**§9.9**): a 30 MHz 7th-order anti-alias filter on the HF input J951 (≥ 60 dB from 50 MHz); the switch-free J951/J952 as the default HF ports; DAC clocks from `CLK_FPGA` ÷ 4 without an MMCM (clock uncertainty `0.165 → 0.035 ns`); no transmit copper within 1.5 mm of any receive line; the enclosure's honest rating below. Still to measure on the first board: TX→RX isolation, the RF switches at 1–5 MHz, the filter above 700 MHz, switcher spurs
Rev08 front end and diagnostics (16–17 Nov)	VHF/UHF receive on `J961`, 30 MHz to 3 GHz: noise figure 2.0 dB and full scale −52 dBm at maximum gain in the direct VHF path, FM-reject ≥ 40 dB with real tolerances; `J961` launch `S11 ≤ -18.1 dB` to 1.1 GHz with its ESD diode and bias tee; no front-end copper within 1.5 mm of either ADC input or the clock tree (**REV08_PLAN §5.5, §11.7**, **SIGNAL_INTEGRITY §9.10**). 14 status and rail LEDs, a USB-C debug console, the IAS0 camera pass-through, and the **board manual**
Rev08.1 power and the PSU board (19 Nov)	One supply and one ground for both boards (sheet `KVPWR`, **POWER_SPEC §1.4**, **AUDIT_Rev08 §6**); the **PSU board** feeds both from the battery through ISO 16750-2 Load Dump A/B, jump start and cranking Levels I, II and IV; its audit, ERC 0 and DRC 0 / 0 (**PSU_SPEC §10**)

Design & verification highlights (**docs/LAYOUT.md**, **docs/SIGNAL_INTEGRITY.md**):

1. **Power & analog isolation.** Supply trunks widened (`865 mm` at `>= 0.5 mm`); `+1V8_A` trimmed to `1.85 V`; DAC1/DAC2 filters colocated under their baluns (`T801`/`T802`), dropping balun common mode by `9–21 dB` (DAC2) and `1–6 dB` (DAC1); `FB401` upgraded to a `2 A / <= 0.1 Ω` bead (`48 mV` drop max, `0.1–0.4 mVpp` ripple on the clock tree).
2. **Differential pairs & LVDS routing.** Nine of 19 data/link pairs plus `CLK_ADCS` and `CLK_FPGA` run coupled `100 Ω` end-to-end on L1/L3/L6; the remaining pairs use `50 Ω` legs matched to `<= 9 ps` worst-case intra-pair skew with on-pad `100 Ω`

terminations.

3. **ADCR data to DCO skew (`-90 to +5 ps`).** `ADCR_DCO` legs are swapped cleanly at the Artix-7 BGA (`N14 = DCO_N`, `P14 = DCO_P`); `adc_capture.v` compensates with `ISERDESE2` inversion + per-bit `IDELAYE2` calibration.
4. **8-layer `JLC08161H-2116C` fabrication stack.** Controlled impedances verified against JLCPCB's solver (**FABRICATION.md**); 5 bare boards quoted at `$287.96` (`140 × 132 mm` with Ethernet tab).
5. **Kria IAS1 I/O standard.** `DIFF_SSTL12` with `RTT_48` on-die split termination (`~96 Ω` to `0.6 V`) and `RDRV_60_60` driver (**INTERFACE_SPEC §6.3**); `2 Gb/s` uplink (`2` pairs) + `1 Gb/s` downlink (`1` pair), `1.25 Gb/s` per lane silicon headroom.
6. **3-D full-wave EM, RF cascade & thermal envelope.** openEMS 3-D sub-models cover L1–L6 vias (`S11 < -29 dB`), BGA escapes (`< -24 dB`), adjacent-pair NEXT (`1.9%`), and `J101` launch (`< -25 dB`). Receive cascades (`cascade.py`) give `NF = 26.8 dB` (radar) / `22 dB` (SDR). Enclosure v2 (`50 × 50 × 15 mm` filtered lid fan + `HS1`–`HS3` heatsinks) is rated for `56 °C` ambient with the stock KV260, whose commercial K26 is the limit (`Tj 85 °C`), and `70 °C` with an industrial K26I SOM, unchanged by Rev08's front end and camera (**ENCLOSURE_V2_THERMAL.md §8**).
7. **Dual-FPGA Vivado 2026.1 gateware & XSim verification.** Full RTL, constraints, Vivado post-route floorplans/schematics, and XSim end-to-end testbenches live in `fpga/` (**docs/FPGA_GATEWARE.md**). *(Design evolution history is archived in **docs/history/README.md**.)*

Estimated cost (**docs/JLCPCB_QUOTE.md**): about **$2,443 for two assembled boards** and **$4,785 for five** (19 Nov, single power entry + RJ45 shield RC; parts + assembly + `JLC08161H-2116C` bare boards).

Documentation

Document	Contents
docs/BOARD_MANUAL.md	**Board manual.** Every connector, LED, switch, jumper, test point and chip, with drawings of both sides, the Pmod pin-out, troubleshooting by LED and typical uses
docs/PSU_SPEC.md	**PSU board.** The battery-to-both-boards supply (`psu/`): LTC4364 surge stopper and LM5177 buck-boost, its simulations (steady state, loop, ISO 7637-2 and 16750-2 events, thermal, conducted noise) and installation
docs/PSU_ENCLOSURE.md	The PSU board's printed enclosure: honeycomb tray and lid, coupled thermal model (vents or sealed, ASA or PETG-CF), CalculiX FEA and renders
docs/FPGA_GATEWARE.md	**Dual-FPGA Gateware.** Artix-7 + Kria K26 RTL, Vivado 2026.1 utilization/timing/floorplans/schematics, CSR map, wideband SDR & AERIS-10 radar DSP, and XSim e2e simulation
docs/HMI.md	**In-car HMI.** The ten touchscreen screens, a Slint application in Rust that runs on the KV260 (Linux KMS), a PC or a phone's browser, its data service and the PL's result streams behind it, and which job runs on the PL, the A53s, the R5F cores, the GPU and the VCU
docs/INTEGRATIONS.md	**Possible integrations.** USB GPS, a 77 GHz radar over CAN, engine live data through opendash (measured against an emulated ECU), a 3D LiDAR, their behaviour in fog, and `kria_bev_grid`, a fusion occupancy grid for the PL
KV260-IAS2RF_Documentation.pdf (release asset)	**Unified Offline Book.** Every document of the project in one PDF, with the vector Vivado floorplans, the 14-page schematic (12 sheets), the 10-page 8-layer layout, the PSU board's schematic and 5-page 4-layer layout, 4K renders, and simulations (generated via **`export_documentation.py`**)
docs/SYMBOLS.md	Custom KiCad symbols cross-checked against datasheets and second sources
Sheet specifications	One per schematic sheet, in the table above
docs/LAYOUT.md	Outline, 8-layer stackup (`JLC08161H-2116C`), design rules, split power layer, placement, routing, and LVDS review
docs/SIGNAL_INTEGRITY.md	Full-wave openEMS & ngspice verification: impedance, SMA launch, LVDS eyes, PDN impedance and DC drop, crosstalk, return vias, DAC filters, RF cascade, and 2-D thermal map (`docs/sim/`)
docs/ENCLOSURE.md & **docs/ENCLOSURE_V2_THERMAL.md**	Enclosure v2 CAD, CalculiX 3-D shock/vibration FEA, 3-D CFD cooling, and `HS1`–`HS5` heatsink sizing
docs/FABRICATION.md	JLCPCB ordering instructions, stackup verification, and output script (`_work/fab/make_fab.py`)
docs/JLCPCB_QUOTE.md	Itemized JLCPCB board, assembly, and LCSC BOM pricing
docs/img/highres/README.md	Index of all 4K PNG renders and lossless SVG/PDF vector schematics, layouts, heatsinks, and Vivado FPGA views

Repository layout

Path	Contents
`KV260-IAS2RF.*`, `sheets/`	KiCad 10 hardware source project (root + twelve schematic sheets + 8-layer PCB)
`fpga/`	Synthesizable Verilog gateware (`artix/`, `kria/`, `link/`, `eth/`), Vivado constraints/build scripts, and full-system XSim co-simulation (**`fpga/README.md`**)
`sw/`	Linux PS software & control utilities
`symbols/`, `footprints/`, `mech/`	Custom KiCad libraries, 3-D models, and Enclosure v2 STL files
`export_documentation.py`	Standalone Python script to build the offline `docs/KV260-IAS2RF_Documentation.pdf` compendium
`_work/`	Reproducible automation scripts (symbol/sheet generators, `build_board.py`, field solvers, openEMS/ngspice/CFD/FEA, Vivado floorplan exporters)
`fab/`	Not tracked. `python _work/fab/make_fab.py` writes Gerbers, drill, BOM, and CPL for JLCPCB
`PCB/`, `Documents/`	Original Allied Vision reference sources

Reproducing hardware checks, Vivado gateware, and offline PDF documentation:

```
kicad-cli sch erc --severity-all KV260-IAS2RF.kicad_sch
kicad-cli pcb drc --schematic-parity --refill-zones --severity-all KV260-IAS2RF.kicad_pcb
python _work/fab/make_fab.py                                  # fab/: Gerbers, drill, BOM, CPL
python _work/layout/lvds_skew.py KV260-IAS2RF.kicad_pcb  # LVDS delays, skew and stubs
python export_documentation.py                                # docs/KV260-IAS2RF_Documentation.pdf
```

Related work

The DSP core this board will need already exists, runs on real silicon and is published separately:

scanner64: a real-time multichannel DDC bank for the KV260's PL. Measured on the board: 100.05 MSPS sustained, no samples dropped across 200 million, bit-exact against its Python model, 8.38 mW per channel, 169.9 MHz Fmax post-route.

That project answers, with hardware, the question this board is built around: whether the PL can sustain a converter stream in real time. It can.

Where the project came from, and attribution

This is a **fork** of the open hardware design Allied Vision Adapter Board CSI-2 for Kria KV260, published under the MIT licence (see **LICENSE**). What is kept from that design:

- the board's mechanical fit to the KV260 (the outline was extended)
- the two Hirose BM20B(0.8)-34DP connectors (IAS0 / IAS1) and their wiring to the SOM

Everything else (the MIPI camera electronics, level shifters, USB power) was removed and replaced by the RF chain described here. **This repository no longer produces an Allied Vision camera adapter board.** If that is what you want, use the original project.

Dual-FPGA Gateware, Silicon Floorplan & Vivado Circuit Schematics

Both FPGAs carry complete, post-route verified Vivado 2026.1 gateware and end-to-end mixed-signal/digital XSim co-simulation (**`fpga/`**, full specification in **docs/FPGA_GATEWARE.md**):

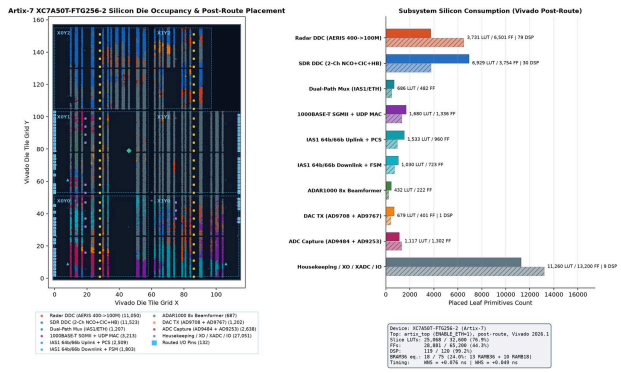
- **Wideband SDR (Front-End Artix-7):** Dual 14-bit `62.5 MSPS` ADC channels (`AD9253`) feeding a direct HF/CB bypass path (`stream_id = 8'h03`; first Nyquist zone `0–31.25 MHz` at `62.5 MSPS`, `0–25 MHz` at `50 MSPS`, and `0–30 MHz` on `J951` behind its low-pass) plus a tunable NCO + CIC + FIR DDC (`stream_id = 8'h02`); `VHF`, `FM`, walkie-talkie (`PMR446` / `GMRS`), `UHF` and ADS-B come from the Rev08 front end on `J961` into the AD9484 (radar ADC) path through SW2, not into this one; paired with the `14-bit 125 MSPS AD9767` TX DAC (`DAC_SDR`).
- **AERIS-10 X-Band Radar (`10.5 GHz` / `20 km` / `8× ADAR1000`):** `400 MSPS AD9484` IF capture into the verbatim `AERIS-10 / PLFM_RADAR` (`62d4c55`) 400 -> 100 MSPS I/Q DDC (`stream_id = 8'h01`), `AD9708` chirp DAC (`DAC_RADAR`), `ADF4382` LO + `8× ADAR1000` beamformer SPI controller (`u_adar_ctrl`), and `u_rf_switch` T/R sequencing.
- **High-Speed Interconnect:** Dual-lane Clause-49 `64B/66B IAS1` LVDS (`1.0–1.25 Gb/s` per lane, `2.0–2.5 Gb/s` uplink + `0.5–1.0 Gb/s` downlink) plus dedicated-pin `1000BASE-T` SGMII/UDP over `U1201 RTL8211FSI` (`~2.94 Gb/s` combined).

<!-- fpga-figures:begin -->

Design (Vivado 2026.1)	Device	LUTs	FFs	BRAM36 eq.	DSPs	WNS / WHS	Failing endpoints	Reports
`artix_top`	XC7A50T-FTG256-2	25,279 (77.5 %)	28,970 (44.4 %)	18.0 (24.0 %)	119 (99.2 %)	+0.007 / +0.033 ns	0 of 83,391	`artix/reports_rev06/` from `build_rev06.tcl`
`ias2rf_k26_bd_wrapper`	XCK26-SFVC784-2LV-c	53,336 (45.5 %)	46,896 (20.0 %)	44.0 (30.6 %), 1 URAM	229 (18.3 %)	+1.043 / +0.010 ns	0 of 188,554	`kria/reports/` from `bd.tcl`

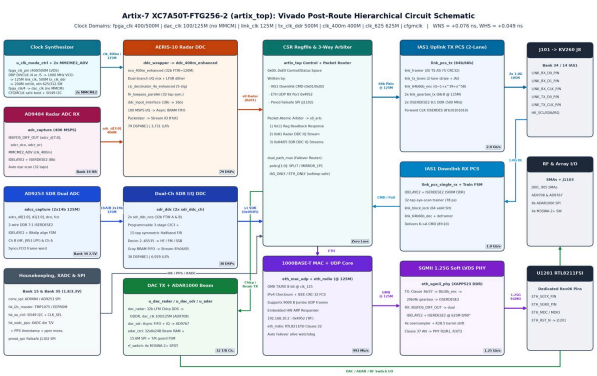
Post-route, generated from the Vivado reports by `_work/fpga_figures.py` (artix_top: Thu Nov 19 04:24:55 2026; ias2rf_k26_bd_wrapper: Thu Nov 19 09:53:51 2026). <!-- fpga-figures:end -->

Artix-7 Silicon Die Floorplan (XC7A50T)



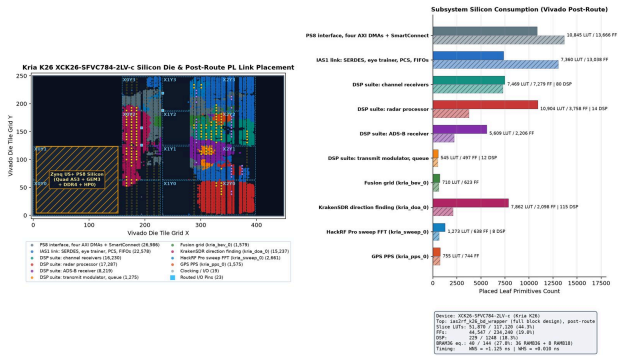
Artix-7 Silicon Floorplan

Artix-7 Post-Route Vivado Circuit Schematic



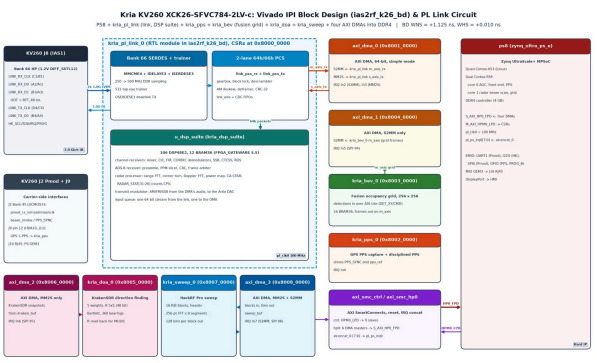
Artix-7 Vivado Schematic

Kria K26 Silicon Die Floorplan (XCK26)

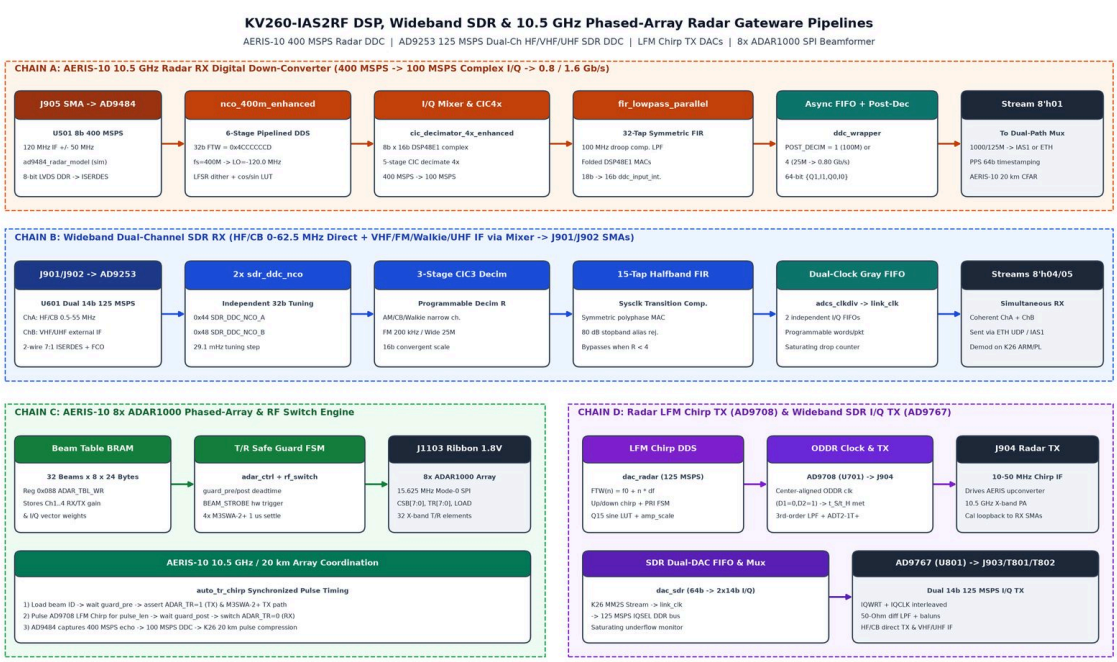


Kria K26 Silicon Floorplan

Kria K26 PS+PL Block Design Schematic



Kria K26 Vivado BD Schematic

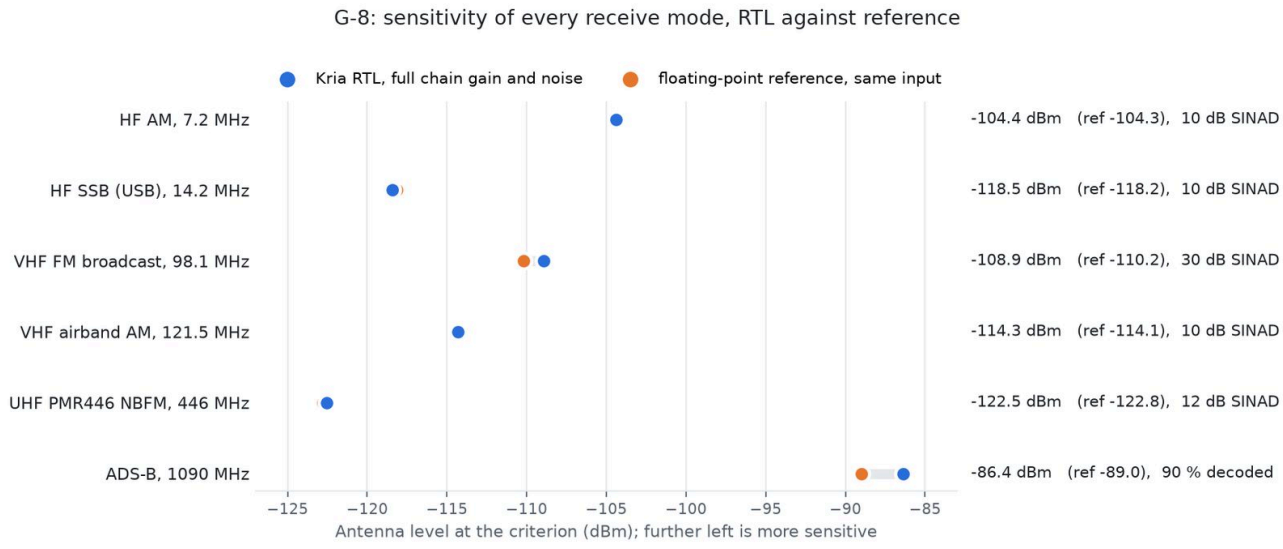


Dual-FPGA Radar & Wideband SDR Signal-Chain Schematic

(Lossless vector PDF/SVG and 4K PNGs of all Vivado floorplans and schematics live in `docs/img/highres/fpga/`.)

Receiver, transmitter and radar simulations (G-8)

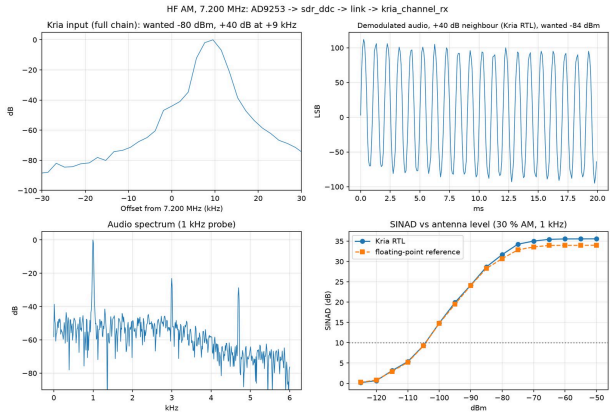
Every use of the board is simulated with realistic signals through the real RTL: the ADC model, the Artix DDC, the board's LVDS channel model, the IAS1 link and the Kria's DSP. Each result is compared with a floating-point reference fed the same input, and each case includes a deliberate fault (a mutation) that its checks must catch. All eight cases pass (**docs/FPGA_GATEWARE.md §6.1**; `python fpga/sim/signals/g8_suite.py`). Levels are at the antenna connector.



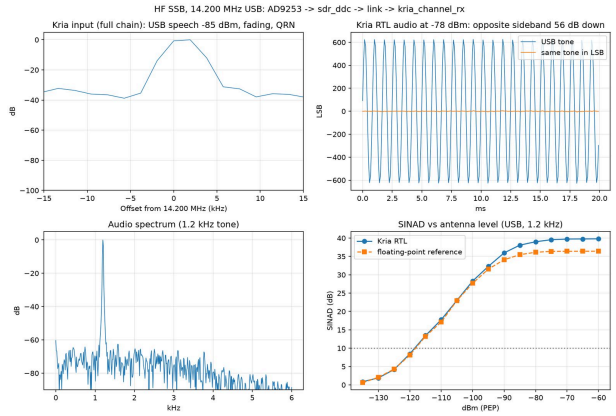
G-8 sensitivity of every receive mode

Case	Path	Result (RTL, with the reference in brackets)
HF AM, 7.2 MHz	AD9253, `sdr_ddc`, AM	10 dB SINAD at -104.4 dBm (-104.3); a +40 dB signal 9 kHz away costs 2.0 dB
HF SSB, 14.2 MHz USB	AD9253, `sdr_ddc`, USB	10 dB SINAD at -118.5 dBm (-118.2); opposite sideband 56.4 dB down
VHF FM broadcast, 98.1 MHz	AD9484, AERIS DDC, WBFM	30 dB SINAD at -108.9 dBm (-110.2); stereo separation 32.6 dB; RDS without errors from -105 dBm
VHF airband AM, 121.5 MHz	AD9484, AERIS DDC, AM	10 dB SINAD at -114.3 dBm (-114.1); 8.33 kHz neighbours cost 0.1 dB at most

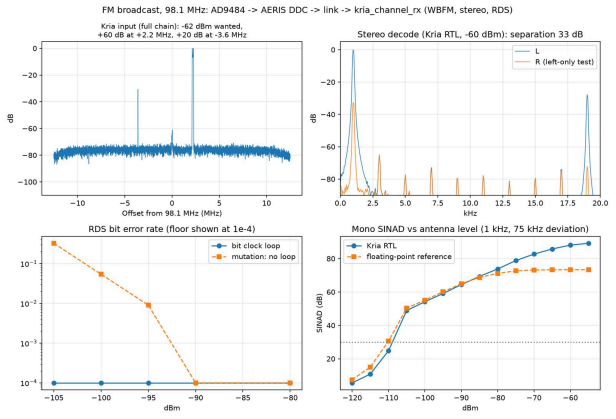
Case	Path	Result (RTL, with the reference in brackets)
UHF PMR446 NBFM, 446 MHz	Converter, AD9484, NBFM	12 dB SINAD at -122.5 dBm (-122.8); CTCSS detected at that level
ADS-B, 1090 MHz	Converter, AD9484, `kria_adsb_rx`	90 % of frames decoded at -86.4 dBm (-89.0); 3 of 3 overlapping replies decoded
Radar, FMCW	AD9484, `kria_radar_proc`	Pd 0.5 at -18.8 dB per sample (model -18.7); Pfa 1.99e-2 (2.00e-2); beam scan finds the target at -15 degrees
Transmit	`kria_tx_mod`, link, AD9767	AM and NBFM SINAD 83 and 58 dB; adjacent channel -80 and -66 dBc; USB opposite sideband 49.9 dB down



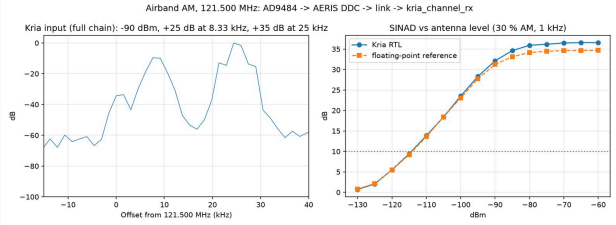
HF AM



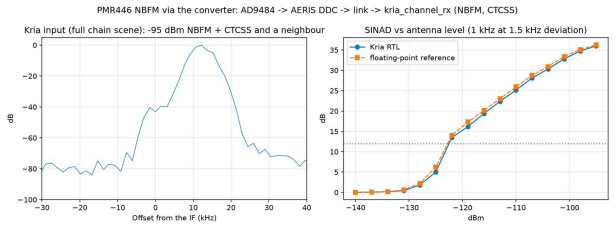
HF SSB



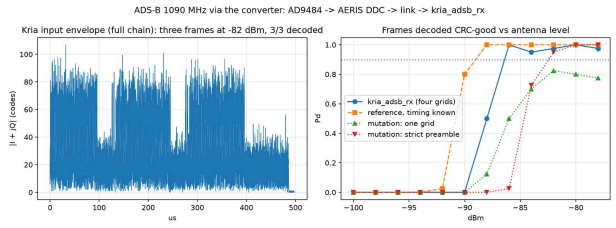
FM broadcast



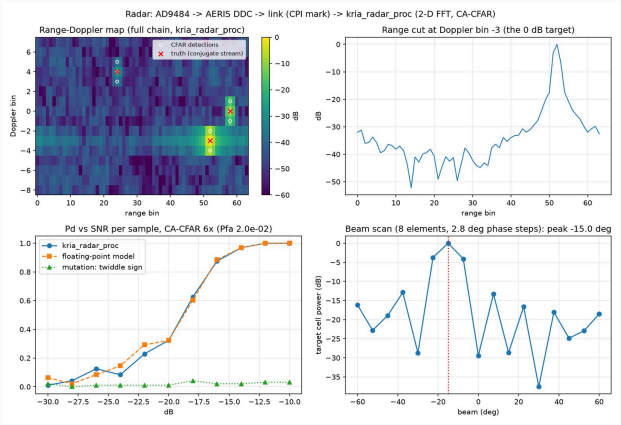
Airband AM



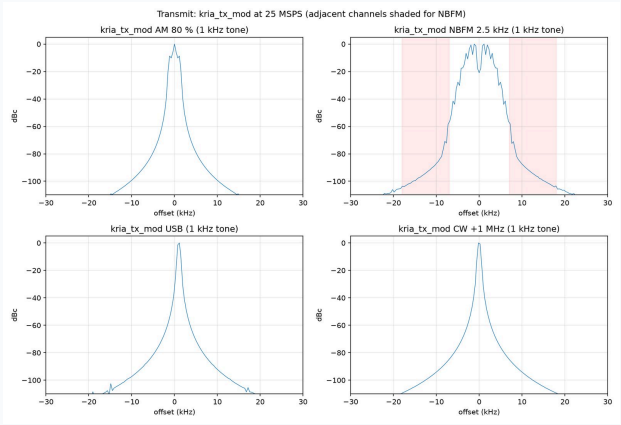
PMR446 NBFM



ADS-B



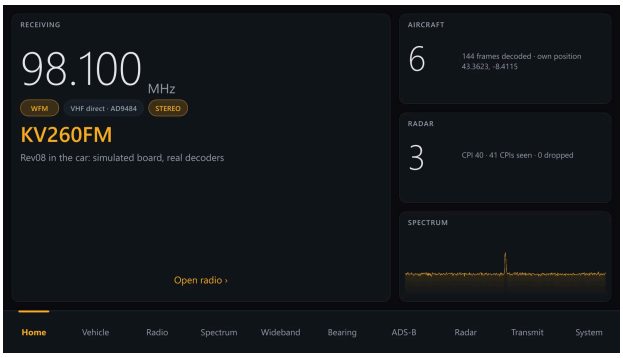
Radar range-Doppler and CFAR



Transmit spectra and masks

In-car screens

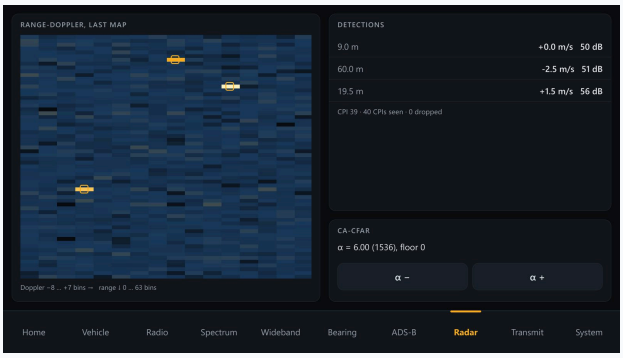
The touchscreen application (**docs/HMI.md**) is written in Rust and Slint and runs on the KV260, a PC or a phone's browser. These images are drawn by the application itself, from the data its service decodes out of the simulated board's DMA blocks.



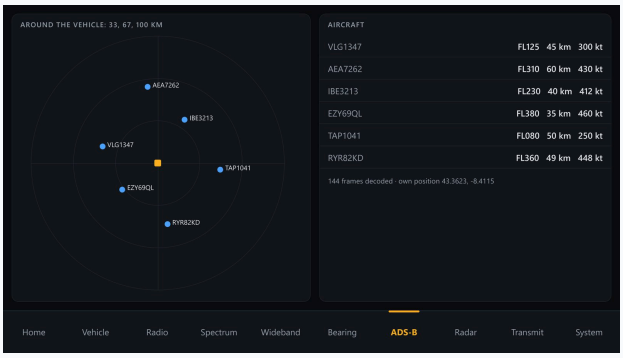
Home screen



Spectrum screen



Radar screen



ADS-B screen

Simulation results (8-layer JLC08161H-2116C)

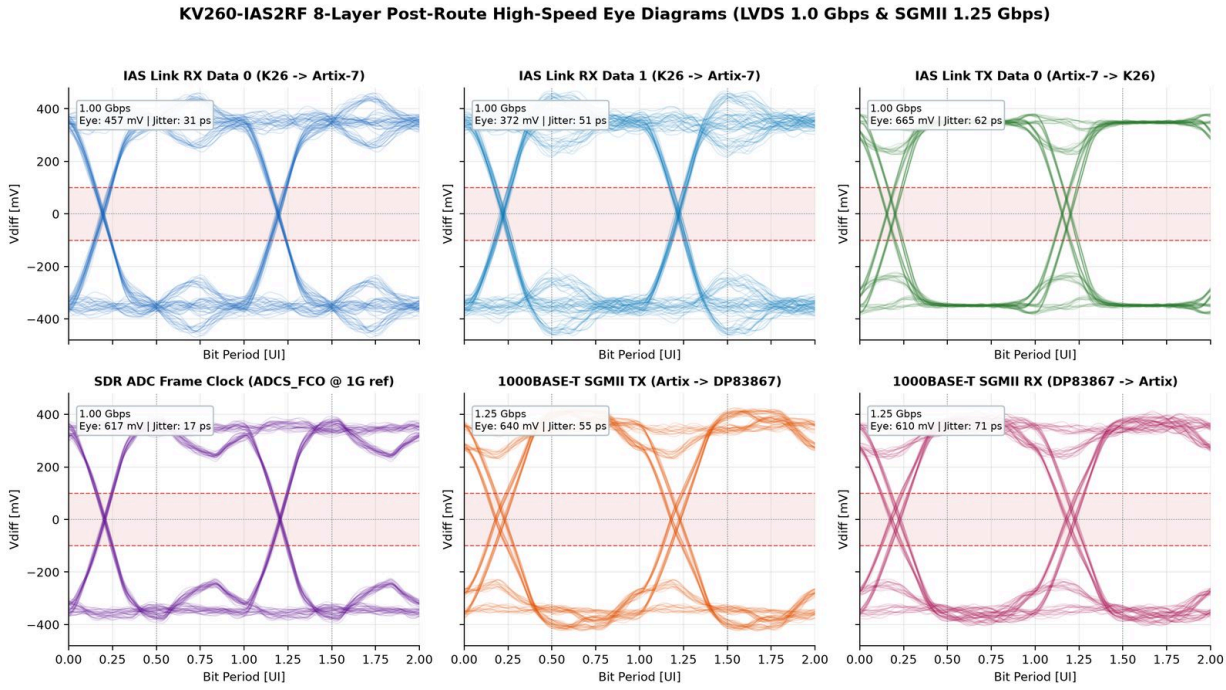
All electromagnetic, transient SPICE, thermal, and power integrity checks are run on the routed **8-layer `JLC08161H-2116C`** board (**docs/SIGNAL_INTEGRITY.md**; vector plots in **`docs/img/highres/sim/`**; historical comparisons archived in **`docs/history/`**).

Check	8-Layer `JLC08161H-2116C` Result
DRC / schematic parity	`0` violations, `0` unrouted connections, `0` parity mismatches
Differential coupling (`L1` / `L3` / `L6`)	`9` of `19` data/link pairs + `CLK_ADCS` & `CLK_FPGA` coupled `100 Ω` end-to-end
Worst intra-pair `|P−N|` skew (with package delay)	**`9 ps`**
Eye lost to routing vs. ideal (`20` pairs, `1 Gb/s` PRBS7)	mean **`-8 mV`**, worst **`-52 mV`**
Zero-crossing spread added by routing	mean **`1 ps`**, worst **`10 ps`**

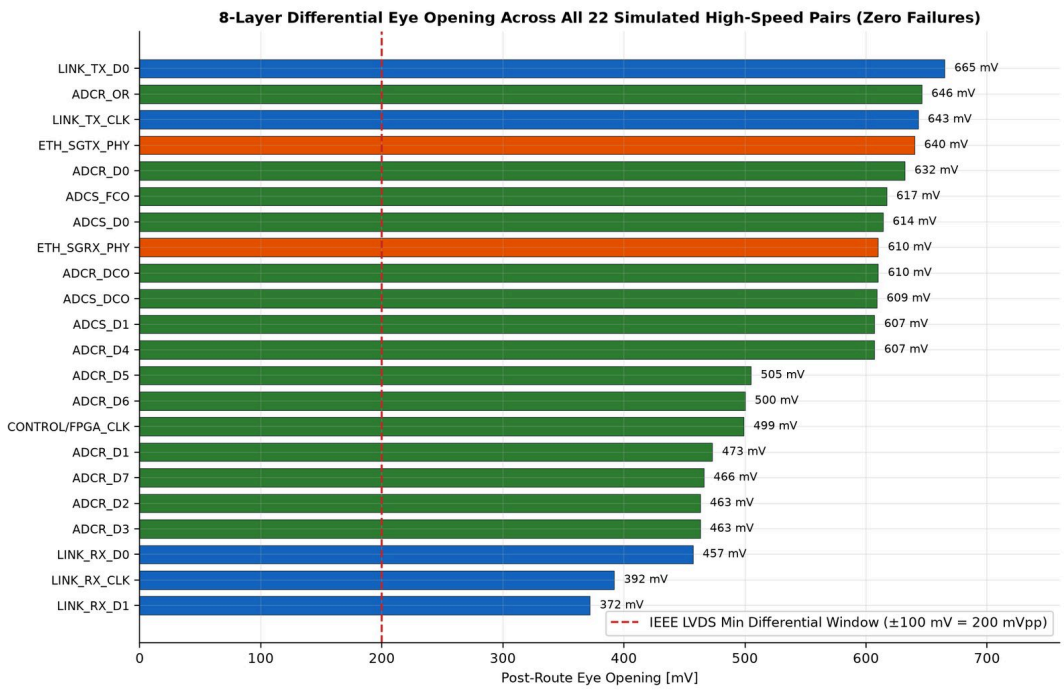
Check	8-Layer JLC08161H-2116C Result
Layer changes without a GND via within 3 mm	**0 of 89**
Parallel adjacent-pair legs within 0.25 mm	65.8 mm (3D NEXT <= 1.9%)
ADCR data minus DCO skew	-90 ... +5 ps (absorbed by per-bit IDELAYE2)
VCCINT PDN impedance (target 120 mΩ)	41 mΩ in-band max, 63 mΩ at 100 MHz
DC drop on +2V5 at 601 mA	122–129 mV
Edge SMA launch S11 (openEMS, with ESD diode)	**-30.9 dB at 1 GHz, -13.7 dB at 3 GHz**

LVDS & SGMII eyes (ngspice, PRBS7 at 1.0–1.25 Gb/s, real routed copper sections vs. ideal 100 Ω line):

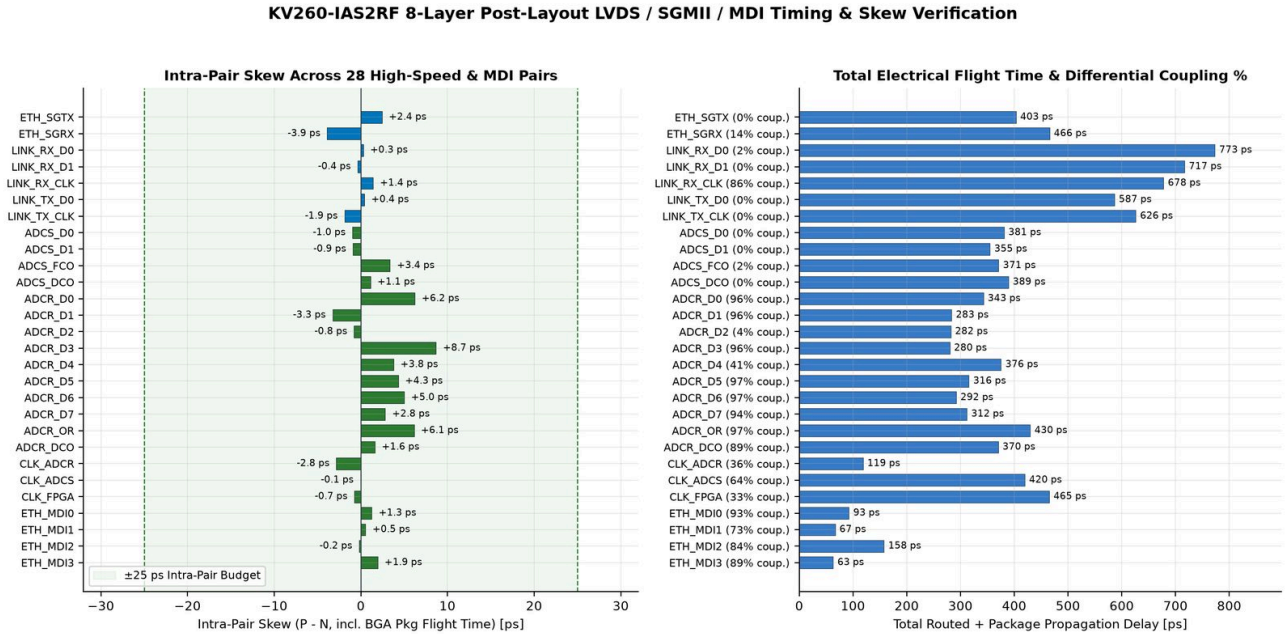
Pair	Ideal line	8-layer routed (eye / jitter)
LINK_RX_D1	385 mV, 41 ps	**372 mV, 51 ps**
LINK_RX_D0	509 mV, 25 ps	**457 mV, 31 ps**
LINK_RX_CLK	395 mV, 10 ps	**392 mV, 10 ps**
ADCS_FCO	628 mV, 17 ps	**617 mV, 17 ps**
ADCR_DCO	609 mV, 17 ps	**610 mV, 18 ps**
ETH_SGTX (1.25 Gb/s)	n/a	**> 350 mV open** (**eye_ETH_SGTX_1P25G.png**)
ETH_SGRX (1.25 Gb/s)	n/a	**> 600 mV open** (**eye_ETH_SGRX_1P25G.png**)



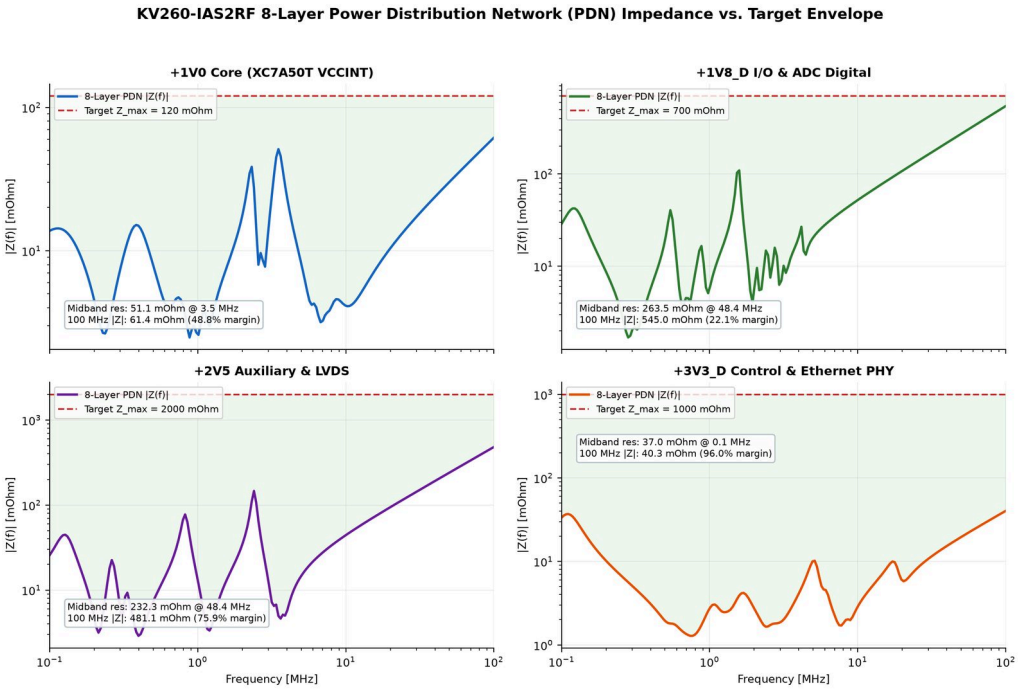
Folded 8-layer LVDS eyes



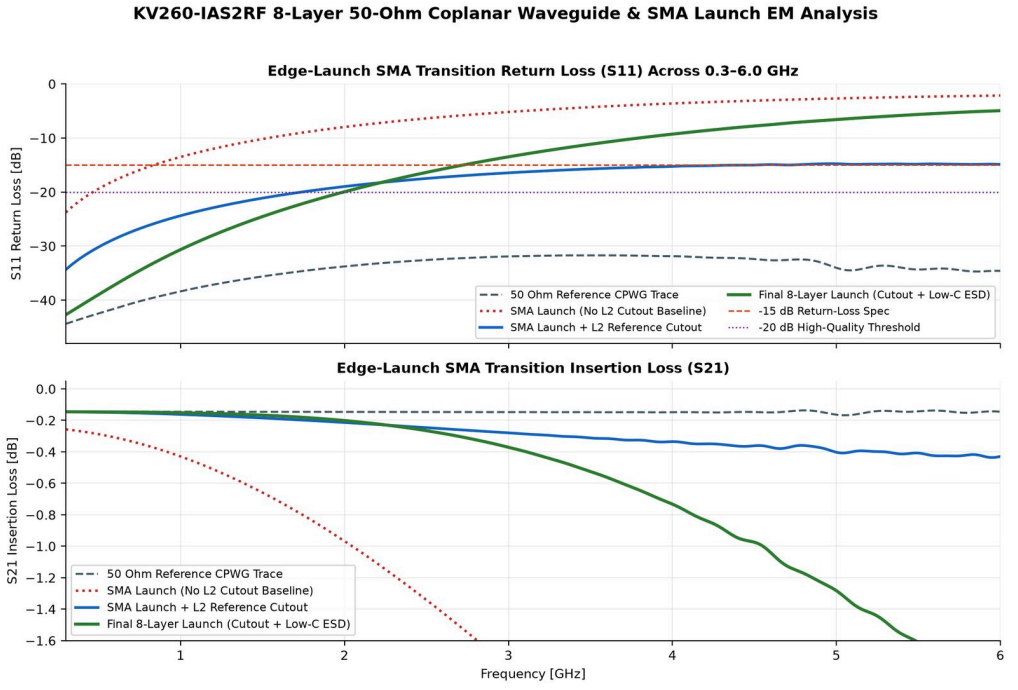
Eye openings and spread across all pairs



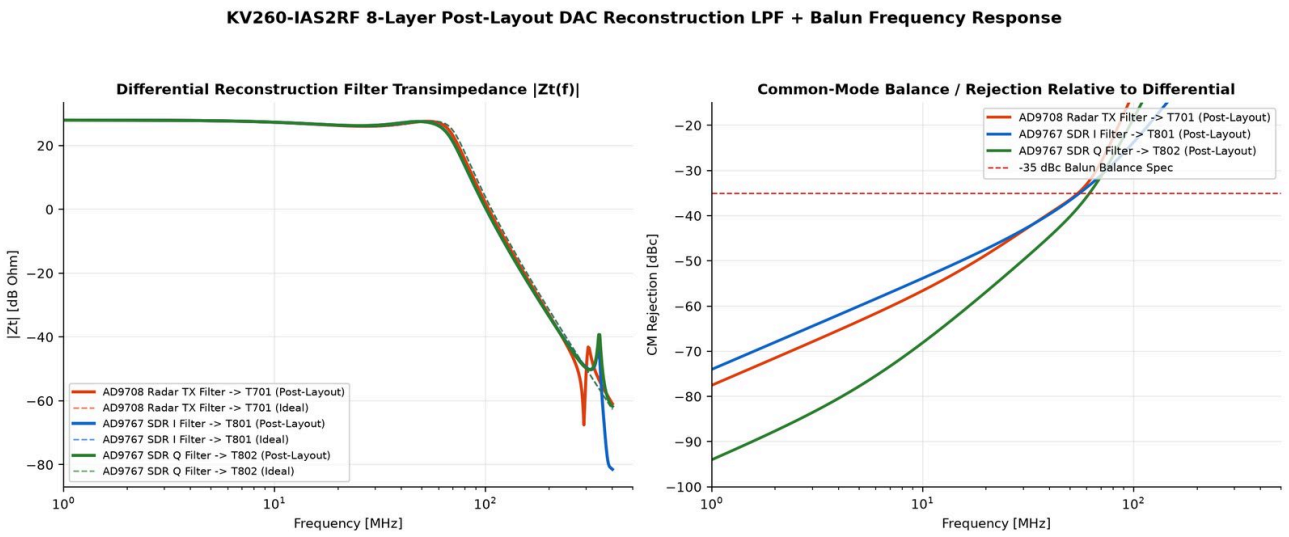
Intra-pair skew



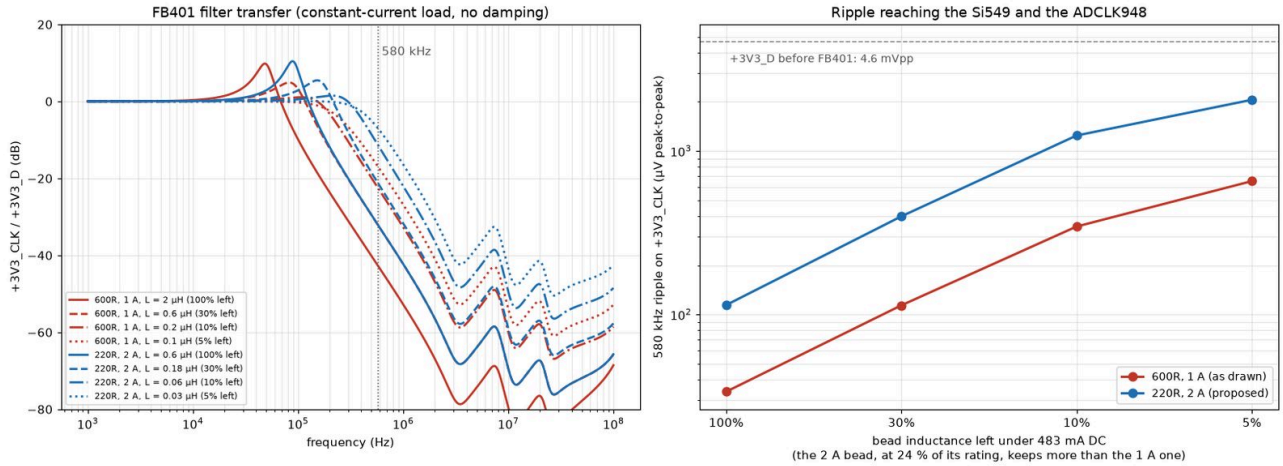
PDN impedance



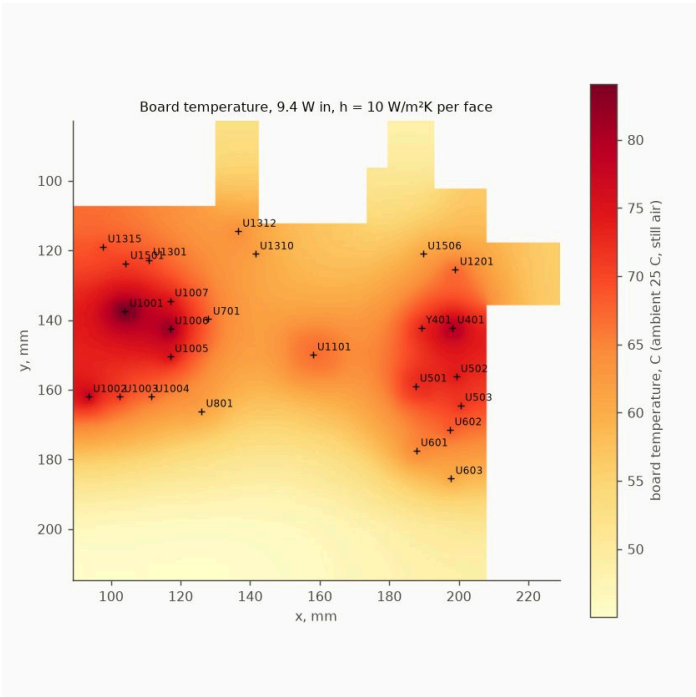
Edge SMA launch S11



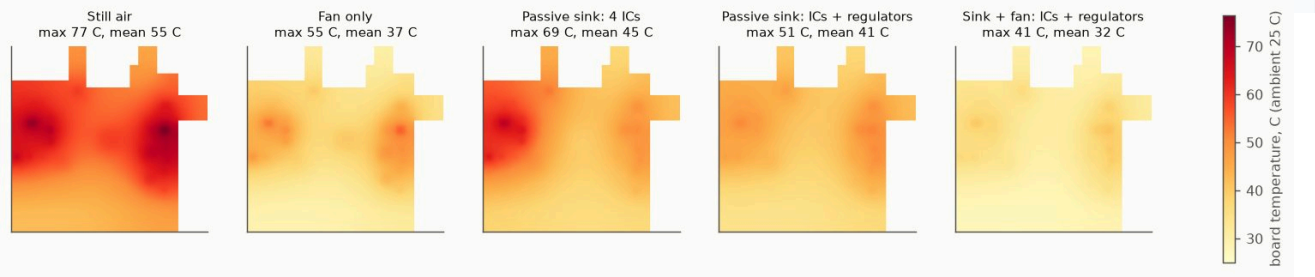
DAC reconstruction filters



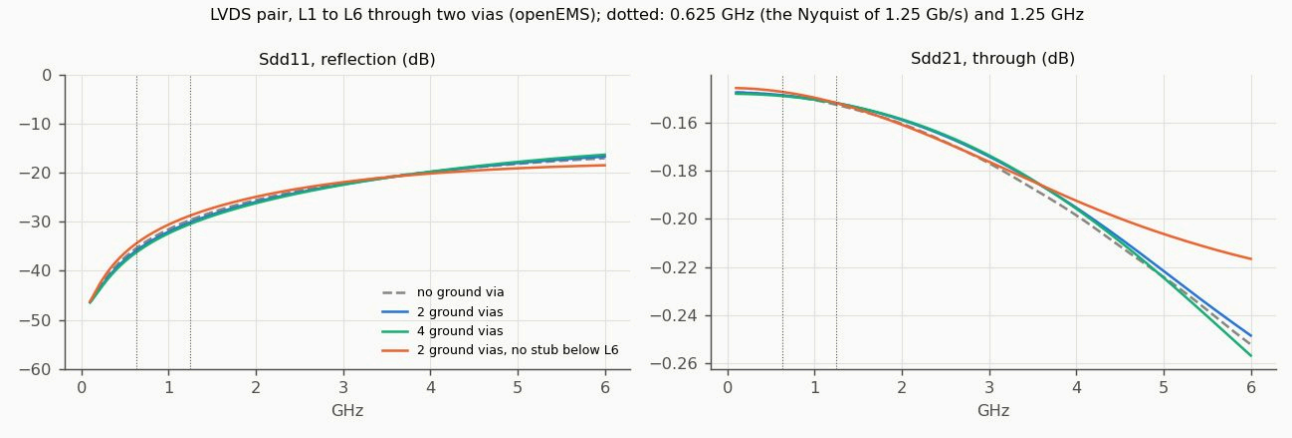
Clock ferrite filter FB401



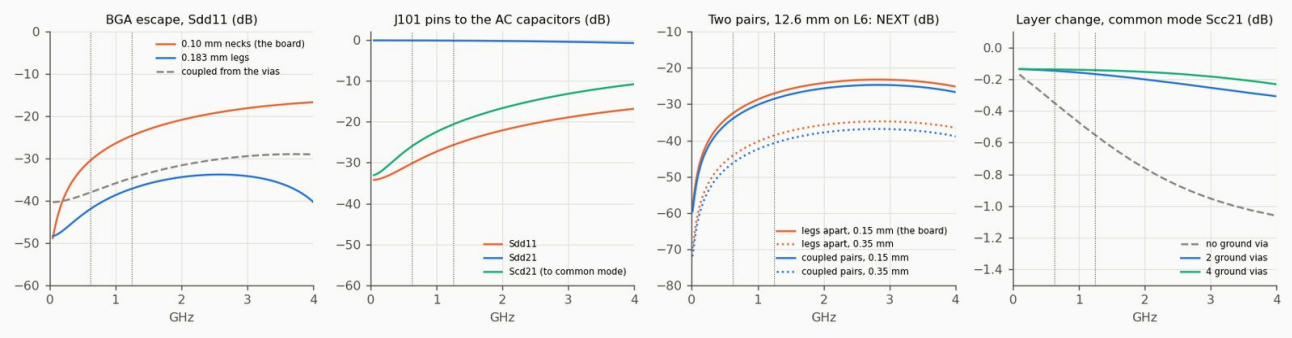
2-D PCB thermal map (8.2 W in still air)



Five cooling configurations compared



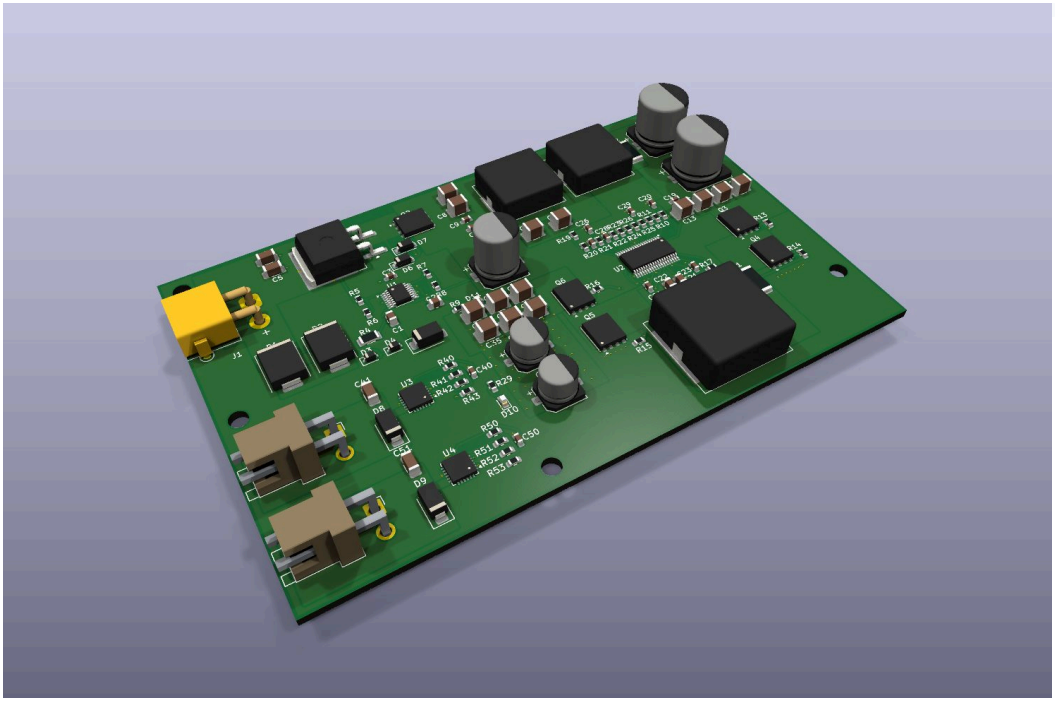
3-D LVDS via transition



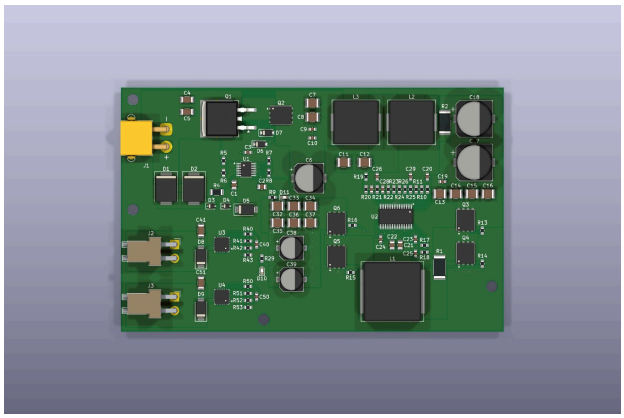
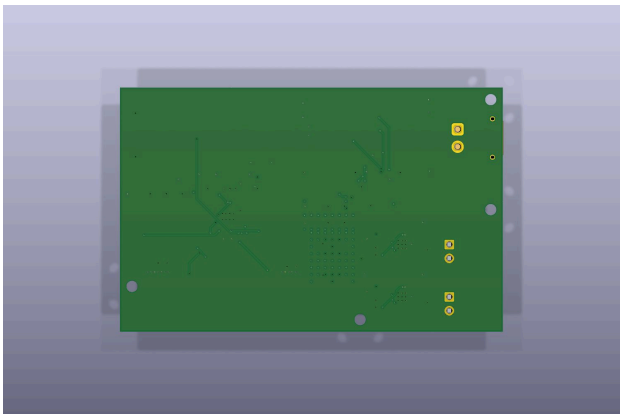
3-D openEMS full-wave sub-models

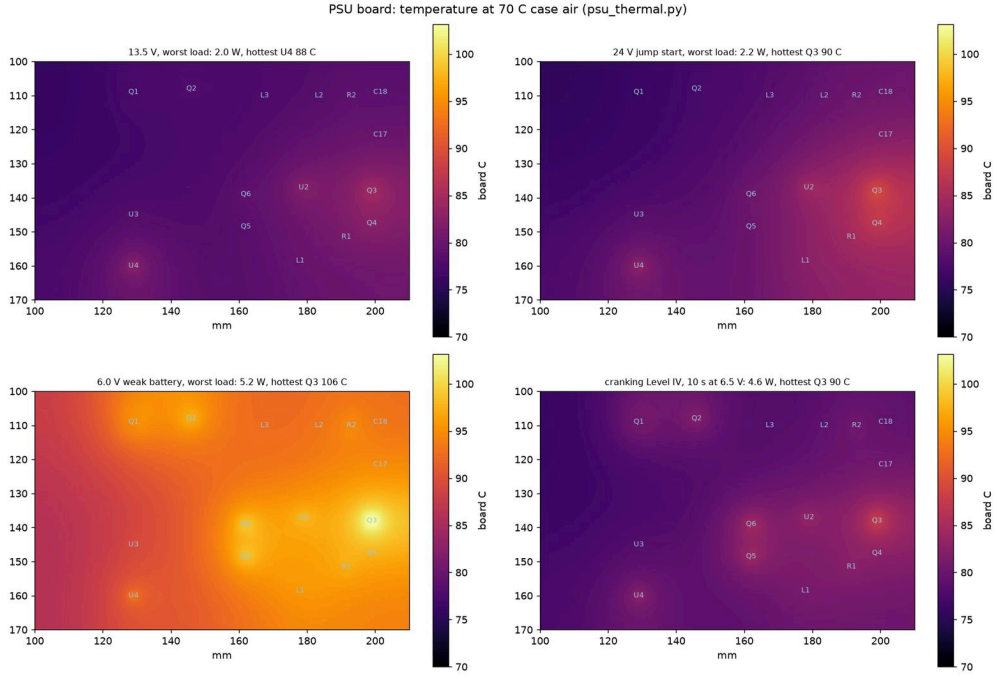
PSU board

A separate 110 x 70 mm, 4-layer board feeds both boards from the car's battery or a 6 to 36 V bench supply, each by its own cable from one ground: an LTC4364 surge stopper (Load Dump A clamped at 48 V, reverse input to -40 V), an LM5177 four-switch buck-boost to 12.0 V, and one TPS26631 eFuse per output (2.0 A to the adapter's `J1001`, 3.0 A to the KV260's `J12`). Both boards keep running through ISO 16750-2 Load Dump A and B, a 24 V jump start and cranking Levels I, II and IV; with two cables, the BM20 link carries 38 mA a contact at the worst load instead of 132 mA. Design values, simulations (steady state, loop, input filter, vehicle events, thermal, conducted noise), layout and installation: **docs/PSU_SPEC.md**; schematic PDF and 4-layer layout PDF (also in the 3-D explorer's Layers tab); KiCad project in `psu/`.



The PSU board, 3D render

Top	Bottom
	
PSU top	*PSU bottom*

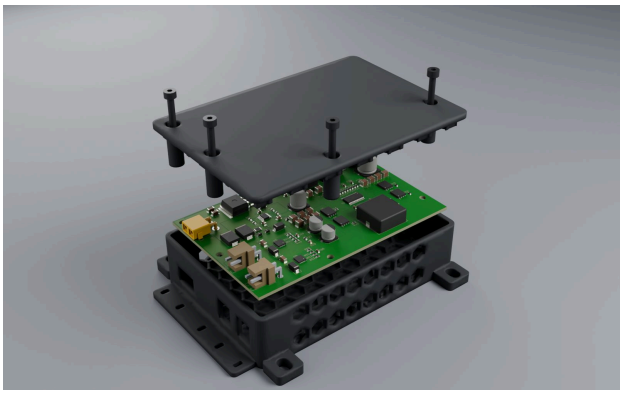


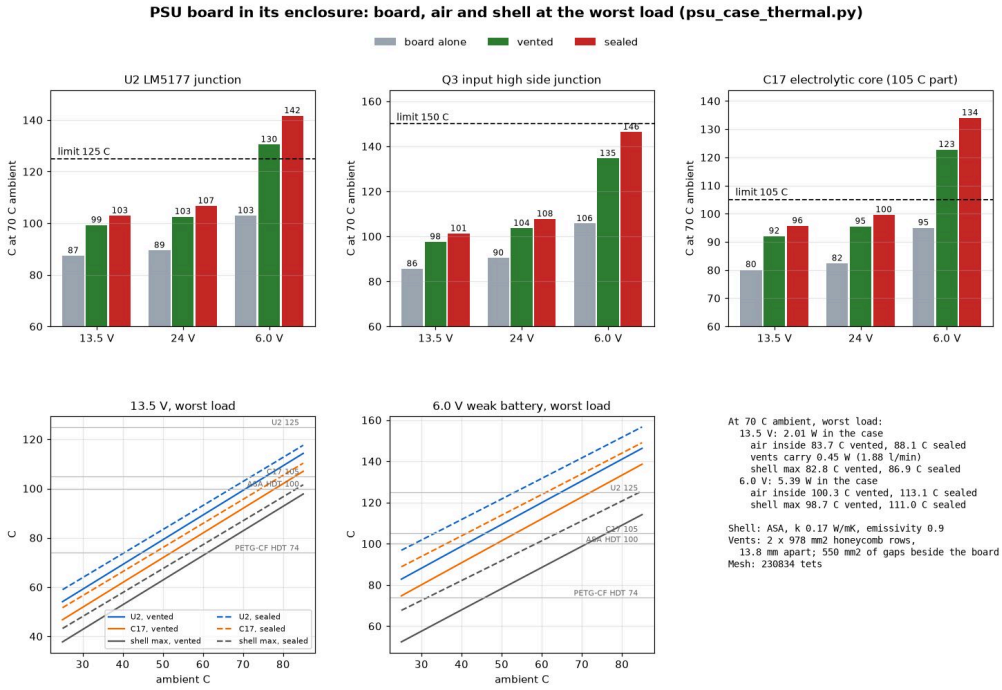
PSU board temperature at 70 C air

The PSU board is also in the 3-D explorer, with every part's nets, its audit row and its thermal results.

Its enclosure

A printed ASA case in the main enclosure's honeycomb: four M3 screws hold the board and close it, honeycomb vents in the long walls, a cable-tie shelf under the connectors and four M5 ears. The coupled board-and-shell thermal model shows the vents are needed (they take 11 C off the LM5177 at the worst load) and rates it, with the car running, to 85 C ambient; CalculiX checks it under 50 g shocks, cable pulls and 300 N on the lid (**docs/PSU_ENCLOSURE.md**).

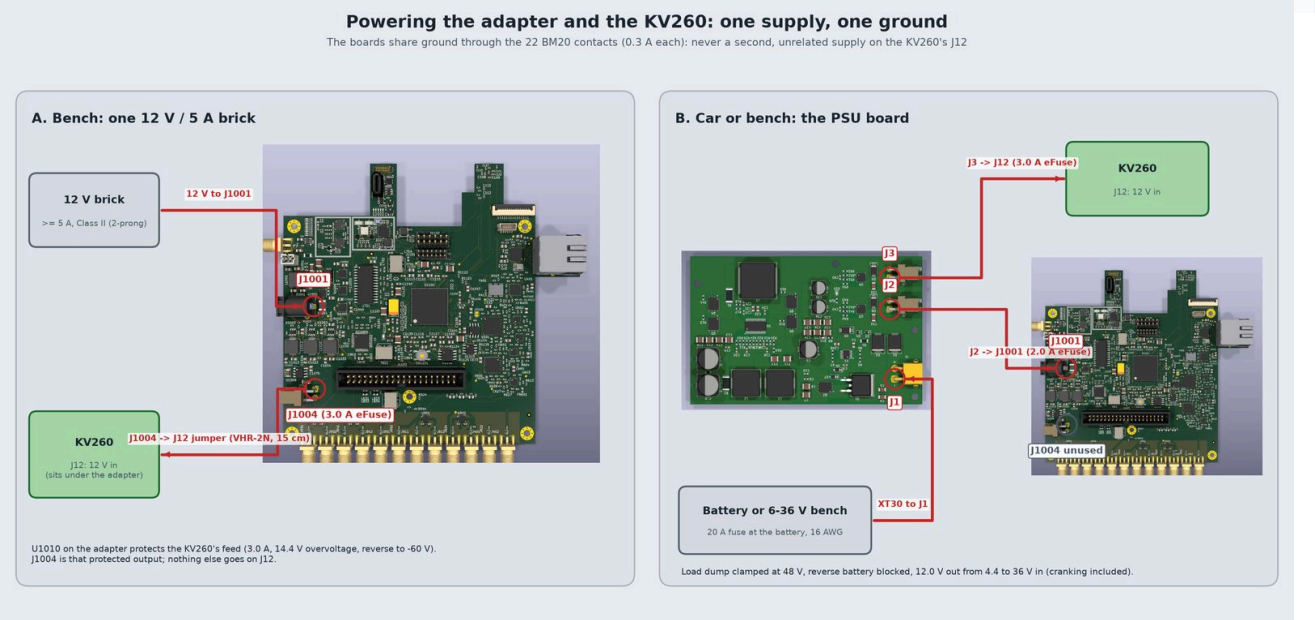
Closed	Exploded
	
PSU enclosure	*PSU enclosure, exploded*



PSU enclosure thermal

Powering the two boards

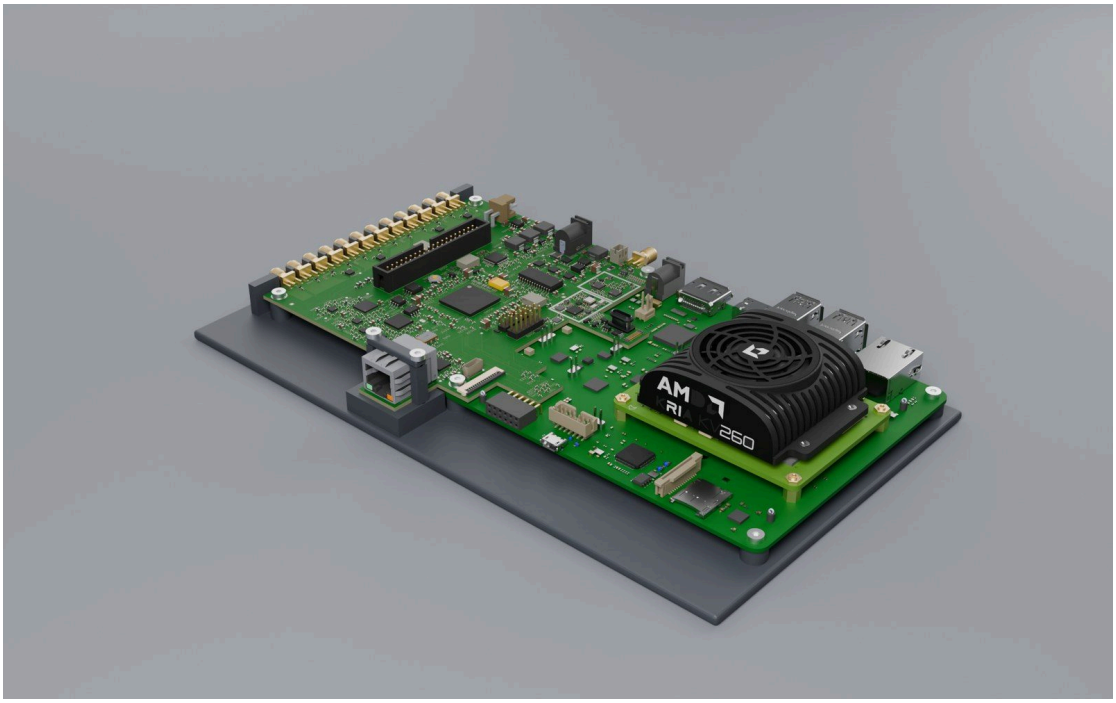
One supply and one ground for both boards: a 12 V brick on the adapter's `J1001` with the short jumper from `J1004` to the KV260's `J12`, or the PSU board with its own cable to each (**BOARD_MANUAL §6**).



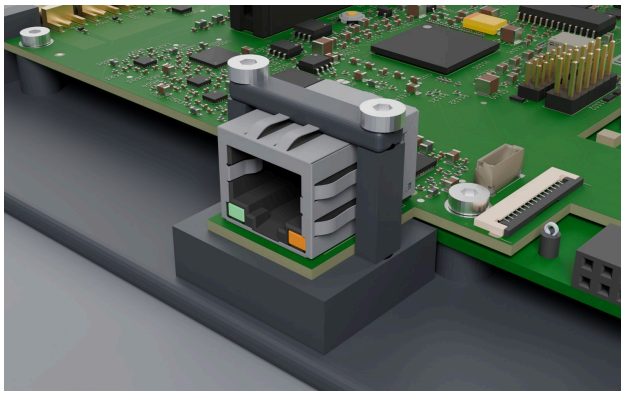
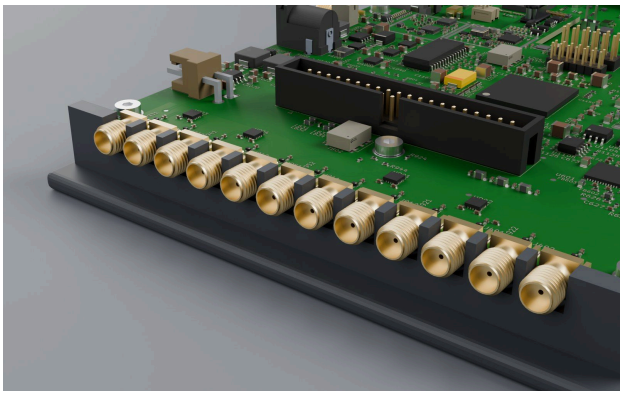
The two ways to power the adapter and the KV260

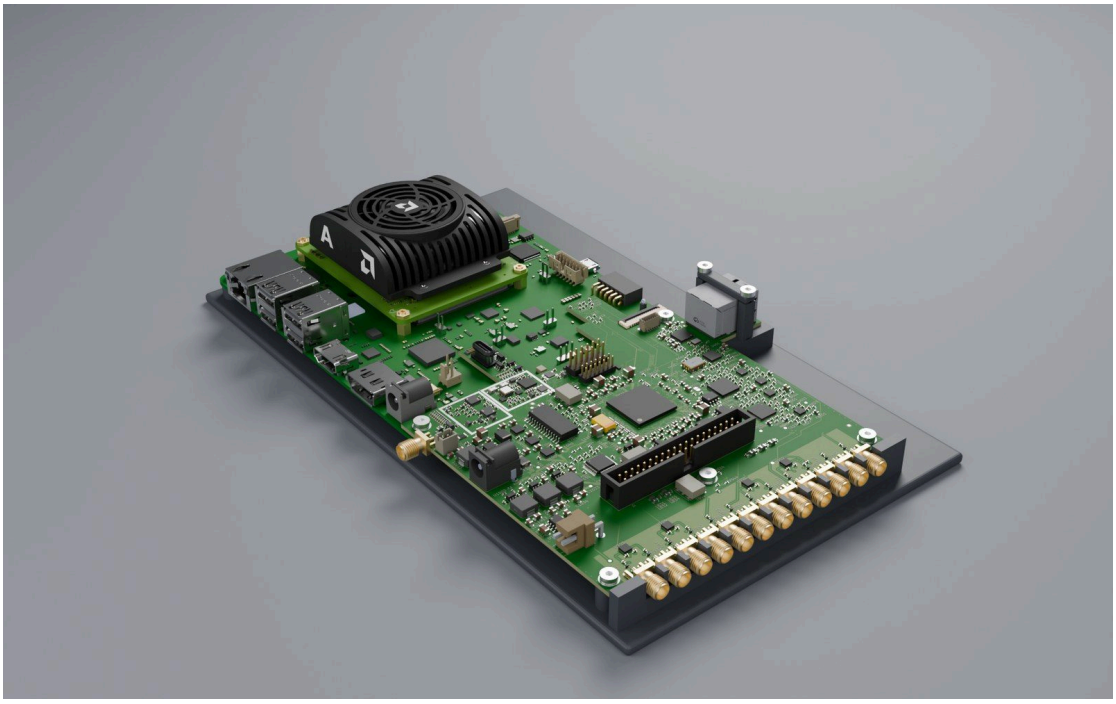
Mounted on the KV260

A printed base holds the KV260 and the adapter together: posts in place of the carrier's rubber feet, posts under the overhang, a wall that takes the SMA cables' torque, and a pedestal and strap that carry the Ethernet tab (**MECHANICAL**; STLs in `mech/`). Rendered in Blender (Cycles) with AMD's KV260 model.



The KV260 and the adapter on the printed base

The RJ45 tab, pedestal and strap	The SMA wall
	
RJ45	*SMA wall*



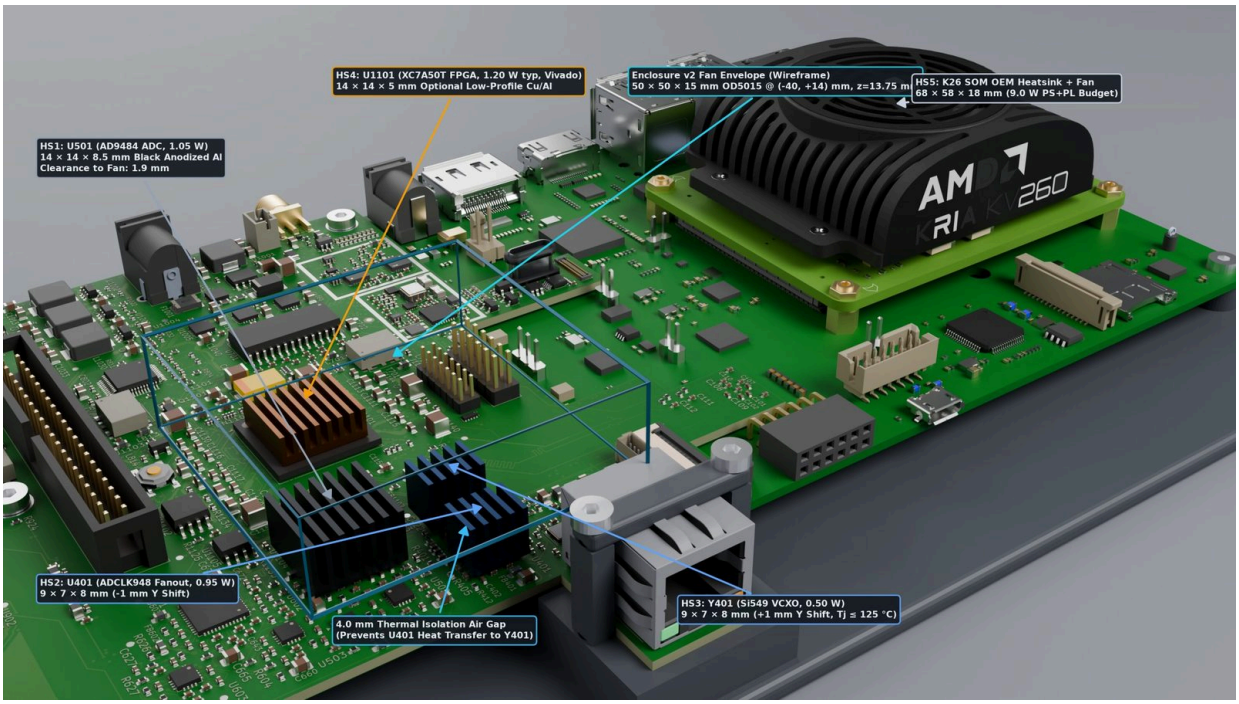
From the other side

Heatsink Placement, Mechanical Envelope & Thermal Cooling (`Enclosure v2`)

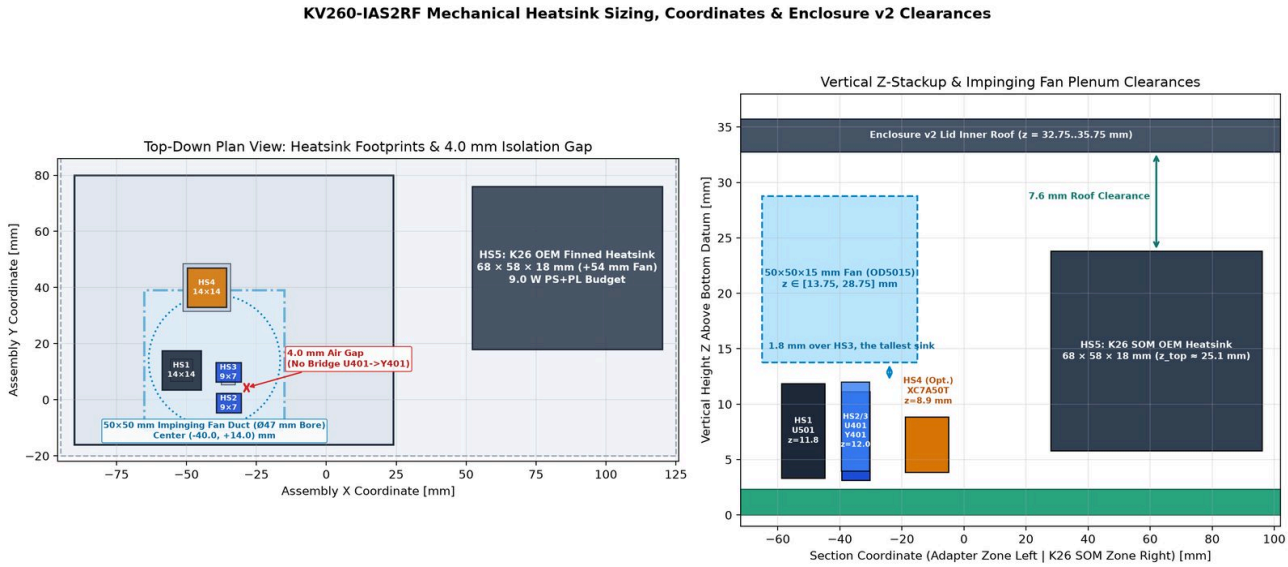
The closed field enclosure (**Enclosure v2**, PETG-CF / ASA / PAHT-CF with optional TPU 95A drop bumpers; **ENCLOSURE.md**, **ENCLOSURE_V2_THERMAL.md**) integrates a `50 × 50 × 15 mm` filtered intake fan (Orion OD5015-05HB, `0.13 A`) on `J1002` directly above the RF/clock hot strip and specifies five mechanically decoupled heatsinks (`HS1`–`HS5`) with verified structural clearances:

Heatsink	Target Component	Dimensions (`L × W × H`)	Assembly centre (`X, Y`, case frame)	Vertical Envelope & Clearance
`HS1`	`U501` (`AD9484` 400 MSPS ADC)	**`14 × 14 × 8.5 mm`** (black anodized Al, `0.18 mm` TIM)	`(-51.8, +10.55) mm`	Fin top `11.8 mm` (`1.9 mm` below the fan at `z = 13.75 mm`)
`HS2`	`U401` (`ADCLK948` LVPECL fan-out)	**`9 × 7 × 8 mm`** (blue anodized Al, `-1.0 mm` Y shift)	`(-34.9, -1.20) mm`	Fin top `11.2 mm` (`y_max = +2.3 mm`)
`HS3`	`Y401` (`Si549` Programmable XO)	**`9 × 7 × 8 mm`** (blue anodized Al, `+1.0 mm` Y shift)	`(-35.0, +9.80) mm`	Fin top `12.0 mm`, `1.8 mm` under the fan (`y_min = +6.3 mm` -> **`4.0 mm` thermal air gap** to `HS2`)

Heatsink	Target Component	Dimensions (L × W × H)	Assembly centre (X, Y, case frame)	Vertical Envelope & Clearance
HS4	U1101 (XC7A50T Artix-7, **fit it in a vehicle**)	**14 × 14 × 5 mm** (low-profile Cu/Al)	(-42.75, +40.0) mm	Fin top ~9.0 mm (with Vivado's FPGA power the CFD gives 102.1 °C at 70 °C ambient without it, 93.4 °C with it; limit 100 °C: AUDIT_Rev08 P6)
HS5	K26 SOM (XCK26 OEM cooler)	**68 × 58 × 18 mm + 54 mm fan**	(+86.1, +47.0) mm	Fin top ~25.1 mm (7.6 mm to Enclosure v2 roof honeycomb vent)



Annotated 4K heatsink placement over KV260 + IAS2RF assembly



Mechanical heatsink keep-out & clearance drawing

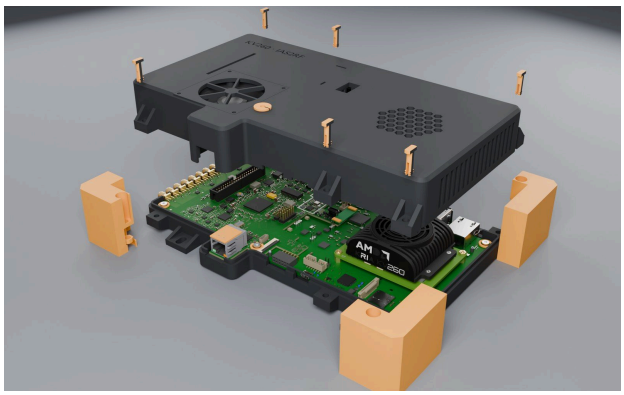
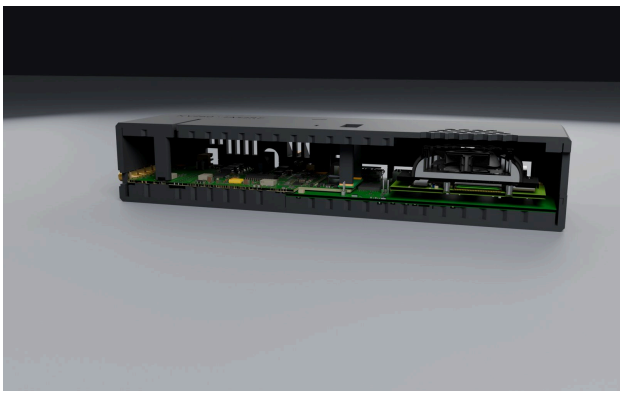
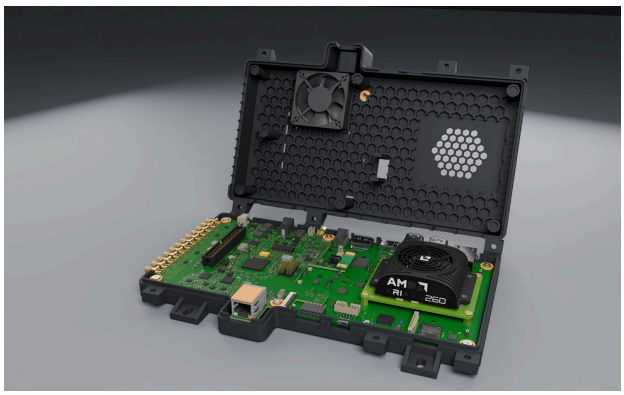
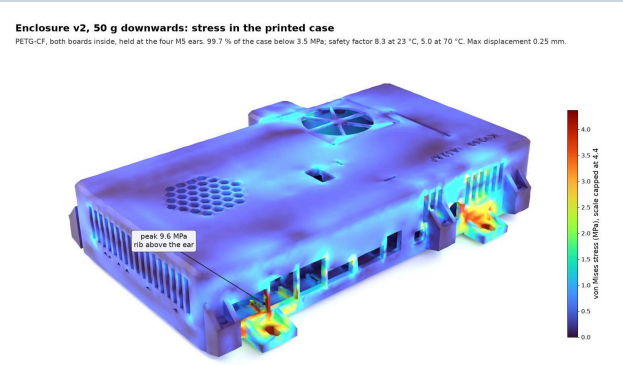
Enclosure v2: Filtered Active Cooling & 3-D FEA

With HS1–HS4 plus the 50 × 50 × 15 mm lid fan (J1002) pressurising the housing (7.5 CFM, +5.2 Pa) and exhausting through 17 right-wall and 9 back-wall slots, the fine-mesh 3-D CFD of the enclosure with the Rev08 board, Vivado FPGA power (1.25 / 1.60 W upper bound) and audited regulator losses rates it for **56.1 °C ambient with the stock KV260** (whose commercial K26 reaches its 85 °C junction limit there; UG1090), **63.3 °C by the adapter's own TA = 85 °C parts** (U401 board temperature), and **70.9 °C with an industrial K26I SOM when HS4 is fitted** (68.0 °C without HS4, because XC7A50T reaches 102.08 °C of 100 °C at 70 °C vs. **93.38 °C clean / 94.24 °C clogged with HS4**; K26I itself stays 99.21 °C). At 70 °C with HS4 fitted the adapter's hottest junctions are the LMR33630 at 117.71 °C (of 125 °C), U1006 (+1V8_D LDO) at 111.09 °C (of 125 °C),

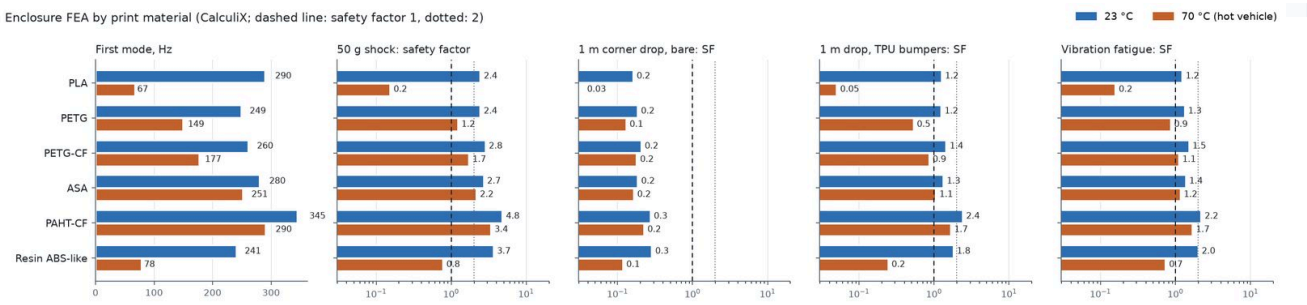
the `ADCLK948` at `98.13 °C` (`Tb = 91.87 °C`), the `XC7A50T` at `93.38 °C` (of `100 °C`), and the `RFFC5072` at `91.37 °C` (**ENCLOSURE §6**, **ENCLOSURE_V2_THERMAL.md §8**). A 197k-tetrahedra 3-D CalculiX FEA under a `50 g` shock keeps peak case stress at `9.6 MPa` (`1.8×` margin at `70 °C`) and BGA strain `<= 96 με` (vs. `500 με` limit; **ENCLOSURE §5.3**).



Enclosure v2 closed, with 50 mm filtered intake fan and TPU bumpers

Version 2 opened (`case_v2`)	Cross-section: fan duct, SMAs & Kria K26 heatsink
	
v2 open	*v2 section*
Version 2 lifted lid: `50 × 50 × 15 mm` fan in its duct	**3-D 50 g FEA: peak stress `9.3 MPa` / BGA strain `<= 162 με`**
	
v2 fan	*FEA stress*

*(4K `3840 × 2160` Cycles renders `board_iso_4k.png`, `board_heatsinks_closeup_4k.jpg`, `case_v2_closed_4k.jpg`, `case_v2_open_4k.jpg`, and `case_v2_section_4k.jpg` are in **`docs/img/highres/renders/`**.)*



FEA by material

Legal notice

This design transmits on regulated bands. Operating the SDR transmitter requires an amateur radio licence or equivalent authorisation, and emission in 10.4–10.6 GHz is subject to national allocations that are **not** free to use in every country. See the compliance section of **ARCHITECTURE.md**. Staying within the applicable law is the responsibility of whoever builds and operates the equipment.

Licence

Licensed under the **Apache License 2.0**; see `LICENSE`. Third-party MIT notices for the inherited Allied Vision CSI-2 adapter reference (`2023`) and verbatim `AERIS-10 / PLFM_RADAR` DSP modules (`fpga/third_party/aeris/`) are preserved in `LICENSE`.

Source: docs/BOARD_MANUAL.md

Board manual

What every connector, LED, switch and chip on the KV260-IAS2RF Rev08 board is for, so that the board can be used without the schematic. The drawings and the tables are generated together from the board file by `_work/manual/board_manual.py`, which also checks that every connector, LED and IC on the board is listed and that every listed part is on the board.



Top side



Bottom side

For orientation, the rendered board: **top**, **bottom**, **iso**. Vector drawings: **top**, **bottom**.

1. Connectors

The thirteen SMAs are on the front edge (`J401`-`J952`) and the back wall (`J961`). Every RF port is DC-blocked except `J961` when its bias tee is on.

No.	Ref	Side	Name	What it is for
1	`J101`	bottom	BM20B(0.8)-34DP	IAS1 to the KV260 (its `J8`), underneath: five LVDS pairs at up to 1 Gb/s each (three data lanes, two clocks), the housekeeping I2C (temperature sensor, ID EEPROM) and the FPGA's interrupt. The board's only data link to the Kria
2	`J102`	bottom	BM20B(0.8)-34DP	IAS0 to the KV260 (its `J7`), underneath. Every pin is passed through to `J103`; the board uses none
3	`J103`	top	BM20B(0.8)-34DS-0.4V(51)	IAS0 pass-through receptacle on the tongue's top face, pin for pin with `J102`: an IAS camera module plugs in here as it would on the carrier
4	`J401`	top	CLK_REF_IN	Reference clock input (SMA) to the ADCLK948, 0.4-3.4 V p-p differential range, 50 ohm on chip. Leave open to run from the on-board Si549
5	`J402`	top	CLK_OUT	Clock output (SMA), ADCLK948 Q3, LVPECL: to share the master clock with an instrument
6	`J911`	top	SDR_RX_A	SDR receive A (SMA): through SW1's default throw to the AD9253 channel A. Full scale about -2.4 dBm; DC-blocked
7	`J912`	top	AERIS_IF_A	Radar IF into the 14-bit AD9253 (SMA), through SW1's second throw
8	`J921`	top	AERIS_IF	Radar IF from AERIS-10 (SMA): through SW2's default throw to the AD9484 (400 or 500 MSPS with the master clock). Full scale about -17.6 dBm
9	`J922`	top	SDR_RX_WB	Wideband SDR receive (SMA), SW2's second throw. Not connected as built: `C926` is not fitted and the VHF/UHF front end takes the throw (`C927`); swap the two 0402s to use this port
10	`J931`	top	SDR_TX_A	SDR transmit A (SMA): AD9767 DAC1 through SW3's default throw, 10 mA full scale
11	`J932`	top	AERIS_TX_A	Radar chirp from the 14-bit AD9767 DAC1 (SMA), SW3's second throw
12	`J941`	top	AERIS_TX	Radar chirp to AERIS-10 (SMA): the AD9708 through SW4's default throw, 20 mA full scale into a 2:1 balun
13	`J942`	top	SDR_TX_WB	Wideband SDR transmit from the AD9708 (SMA), SW4's second throw
14	`J951`	top	SDR_RX_C	HF receive (SMA), no switch: a 30 MHz 7th-order elliptic low-pass, then the AD9253 channel B. Full scale about -3.0 dBm. The default HF input
15	`J952`	top	SDR_TX_C	HF transmit (SMA), no switch: AD9767 DAC2. The default HF output
16	`J961`	top	VU_ANT	VHF/UHF antenna (SMA, back wall): the Rev08 front end, direct 30-170 MHz and converted from 300 MHz to 3 GHz (170-300 MHz not covered: the converter's 300 MHz high-pass, AUDIT_Rev08 R1), into the AD9484 through SW2. Bias tee for an active antenna (off at power-up, 5 V or 3.3 V by `JP1301`, 125 mA limit; prefer 3.3 V where the antenna accepts it). Full scale -52 dBm at maximum gain, up to about +2 dBm with the attenuator and the LNA bypassed. No limiter: keep it away from a transmitter on the same vehicle (+25 dBm destroys the LNA)
17	`J1001`	top	12V IN	12 V input, barrel jack (CUI PJ-102AH, 5 A). Single power entry for both boards (`L1004` on both lines): feeds the adapter (11.7 W typical, 13.4 W / 1.12 A worst; `F1001` 2 A PTC, 18.3 V OVP) and the KV260 via `U1010`/`J1004` (3.0 A / 3.19 A max limit; 1.89 A typical, 4.12 A rated, 4.31 A worst combined). See POWER_SPEC section 1.4 and section 6
18	`J1002`	top	FAN 5V	Enclosure fan, JST PH 2-pin: pin 1 +5 V (0.5 A PTC `F1002`), pin 2 GND
19	`J1004`	top	B2PS-VH	12 V output to the KV260's `J12` (JST VH 2-pin right-angle, 10 A: pin 1 `+12V_KV`, pin 2 `GND`): protected by `U1010` (8.0 V UVLO, 14.4 V OVP, 3.0 A limit via `R1043` 6.04 kohm, -60 V reverse); see section 6
20	`J1101`	top	JTAG 2x7 2mm	Xilinx JTAG for the XC7A50T and its flash (Platform Cable or any 2 mm 14-pin JTAG adapter)
21	`J1102`	top	Pmod	Pmod from the KV260's `J2` (cable): SPI to the FPGA's register file, beam strobe, PPS and the debug UART. Pin by pin below
22	`J1103`	top	AERIS ADAR	AERIS-10 beam-steering ribbon (2x20 IDC): the ADAR1000 SPI and its control lines
23	`J1201`	top	HR911130C	Gigabit Ethernet (RJ45, magnetics and LEDs inside), from the RTL8211FS over SGMII to the FPGA: the board standalone
24	`J1501`	top	TYPE-C-31-E-17	Debug USB-C (vertical, on the tongue): the FPGA's console through a CH340X, 115,200 baud 8N1, powered from the cable. Lid off
25	`J1502`	top	FPC-1.0FX-15PWCR-H20	GPS PPS and the vehicle CAN to the KV260's `J9` (Raspberry Pi camera connector) by a 100 mm 15-way 1 mm FFC, either cable type: the pulse reaches `J9` pin 12, a PL pin (`kria_pps`); CAN TX leaves on `J9` pin 6 and RX comes back on pin 8 (PS `CAN1`, R5F core 1)

No.	Ref	Side	Name	What it is for
26	J1503	top	BM06B-SRSS-TB	GPS receiver and vehicle CAN, JST-SH 6-pin, vertical, the plug from above: 1 GND, 2 CANL, 3 CANH, 4 GND, 5 PPS in (3.3 V), 6 +3.3 V out (0.2 A PTC) (no termination: it taps the car's bus)

1.1 Pmod J1102

A Pmod cable from the KV260's J2. 3.3 V signals into the FPGA's bank 15, ESD-protected by U1108/U1109.

Pin	Net	Direction	Use
1	PMOD_CS	in	SPI chip select of the FPGA's register file
2	BEAM_STROBE	in	Applies the loaded beam on every ADAR1000 at once (R5F core 1 drives it in scan mode)
3	PMOD_MOSI	in	SPI data to the FPGA
4	PPS_SYNC	in	GPS PPS, to time-stamp detections
5	PMOD_MISO	out	SPI data from the FPGA
6	PMOD_SPARE1	in	Debug UART, Kria to FPGA (PS UART1 TX); the USB bridge also drives it through 1 kohm
7	PMOD_SCLK	in	SPI clock
8	PMOD_SPARE2	out	Debug UART, FPGA to Kria (PS UART1 RX); also lights the heartbeat LED
9, 10	GND		
11, 12	not connected		The board takes no power from the Pmod

1.2 Test points

Ref	Net	Ref	Net	Ref	Net
TP1	+5V0	TP2	+3V3_D	TP3	+3V3_A
TP4	+2V5	TP5	+1V8_D	TP6	+1V8_A
TP7	+1V2	TP8	+1V0	TP9	-3V3
TP10	+3V3_CLK	TP11	DONE	TP12	GND
TP13	GND	TP14	MDC	TP15	MDIO

2. Switches and jumpers

No.	Ref	Side	Name	What it does
27	SW1101	top	PROG	Pulls the FPGA's PROG_B: reloads the bitstream from the flash
28	JP1101	top	WC	Solder jumper, open as built: close it to allow writing the board-ID EEPROM U1105
29	JP1301	bottom	BIAS 5V0	3V3

Assembly options. C926/C927 choose what SW2's second throw reaches: as built C927 is fitted (the VHF/UHF front end) and C926 is not (J922). The Ethernet parts (U1201, J1201, Y1201) can be left off the BOM for a board that only runs with the Kria. The master clock mode (400 or 500 MHz) has no jumper: the FPGA programs the Si549 over I2C.

The RF switches, set by the FPGA's register file (SW_CTRL0-3); pulled to the default while the FPGA is unconfigured:

Switch	Default (RF1)	Second throw (RF2)
SW1 U901, AD9253 channel A	J911 SDR_RX_A	J912 AERIS_IF_A
SW2 U902, AD9484	J921 AERIS_IF	The VHF/UHF front end (J922 with C926 fitted)
SW3 U903, AD9767 DAC1	J931 SDR_TX_A	J932 AERIS_TX_A
SW4 U904, AD9708	J941 AERIS_TX	J942 SDR_TX_WB

3. LEDs

The nine status LEDs stand in a column beside J961, seen through a window in the lid. The rail LEDs are on the tongue: each one is lit by its rail, so a dead rail shows without a meter.

No.	Ref	Side	Colour	Meaning when lit
30	D1501	top	CFG green	FPGA configured and the clock sequencer finished

No.	Ref	Side	Colour	Meaning when lit
30	D1502	top	CLK yellow	Master clock mode: on 500 MHz, off 400 MHz
30	D1503	top	LINK green	IAS1 link to the Kria trained
30	D1504	top	ADCR red	The radar ADC (AD9484) clipped since the last read (sticky)
30	D1505	top	ADCS red	The SDR ADC (AD9253) clipped since the last read (sticky)
30	D1506	top	LO green	The RFFC5072 synthesiser is locked
30	D1507	top	TX red	A DAC is driving an SMA
30	D1508	top	ERR red	Any sticky error: CRC, FIFO overflow, I2C no-acknowledge, over-temperature
30	D1509	top	HB blue	Heartbeat: flickers with every line the FPGA prints on the debug UART, once a second
31	D1520	top	+12V green	+12V present (after the input protection)
31	D1521	top	+5V0 green	+5V0 present
31	D1522	top	+3V3_D green	+3V3_D present
31	D1523	top	+1V8_D green	+1V8_D present (switched from +3V3_D by Q1520)
31	D1524	top	+1V0 green	+1V0 (FPGA core) present (switched from +3V3_D by Q1521)
32	D1101	top	green	DONE: the FPGA has loaded a bitstream

At power-up, in order: the five rail LEDs; DONE when the FPGA has loaded its bitstream; CFG when the clocks are running; HB flickering once a second; LINK when the Kria has trained IAS1. The RJ45's own two LEDs show the Ethernet link and activity.

What you see	What it means, what to check
No LED at all	No 12 V, or the input protection is off: input below about 6 V, above 18.3 V, or reversed. Check J1001, F1001
+12V on, +5V0 off	U1001 or its load: measure TP1; a short on +5V0 holds the buck in hiccup
+5V0 on, +3V3_D off	U1002; every other rail after it stays off too
+1V8_D or +1V0 off, +3V3_D on	U1006 (+1V8_D) or U1004 (+1V0); TP5, TP8
Rails on, DONE off	No bitstream: the flash is empty or the load failed. Program it through J1101, or press SW1101
DONE on, CFG off	The clock sequencer did not finish: the Si549 did not answer on I2C, or J401's reference is out of range
CFG on, LINK off	The Kria has not trained IAS1: its bitstream or kria_pl_link is not running, or J101 is not seated
HB not flickering	The FPGA's status task has stopped, or the debug UART is held by the Kria (PMOD_SPARE2)
LO off	The RFFC5072 is unlocked: only the converted VHF/UHF modes are affected
ADCR or ADCS on	A converter clipped: lower the input (or the front end's gain); the LED clears when read
ERR on	Read the error register over the console (r command) to see which: CRC, FIFO, I2C or temperature

4. Chips

No.	Ref	Side	Part	Sheet	Function
33	U1101	top	XC7A50T-2FTG256I	CONTROL	The front-end FPGA: converters, RF switches, link to the Kria, Ethernet, housekeeping
34	U1102	top	MT25QL128ABA1ESE	CONTROL	128 Mbit SPI flash: the FPGA's bitstream
35	U1103	top	74LVC1G07	CONTROL	Open-drain buffer on the FPGA's PROG_B
36	U1104	top	TMP1075DR	CONTROL	Board temperature sensor, I2C 0x48
37	U1105	top	M24C02-FMN6TP	CONTROL	Board-ID EEPROM (revision, serial), I2C 0x50, write-protected unless JP1101 is closed
38	U1108	top	TPD4E05U06DQAR	CONTROL	ESD array on the Pmod lines
39	U1109	top	TPD4E05U06DQAR	CONTROL	ESD array on the Pmod lines
40	U1110	top	TPD4E05U06DQAR	CONTROL	ESD array on the JTAG lines
41	U1201	top	RTL8211FSI-CG	CONTROL	Gigabit Ethernet PHY, SGMII to the FPGA
42	U401	top	ADCLK948BCPZ	CLOCK	Clock fan-out: the converters' and the FPGA's clocks from the Si549 or J401
43	U501	top	AD9484BCPZ-500	ADC_RADAR	8-bit ADC at 400 or 500 MSPS with the master clock: the radar IF, the wideband SDR and the VHF/UHF front end
44	U502	top	AD8352ACPZ	ADC_RADAR	Differential driver for the AD9484, first stage
45	U503	top	AD8352ACPZ	ADC_RADAR	Differential driver for the AD9484, second stage

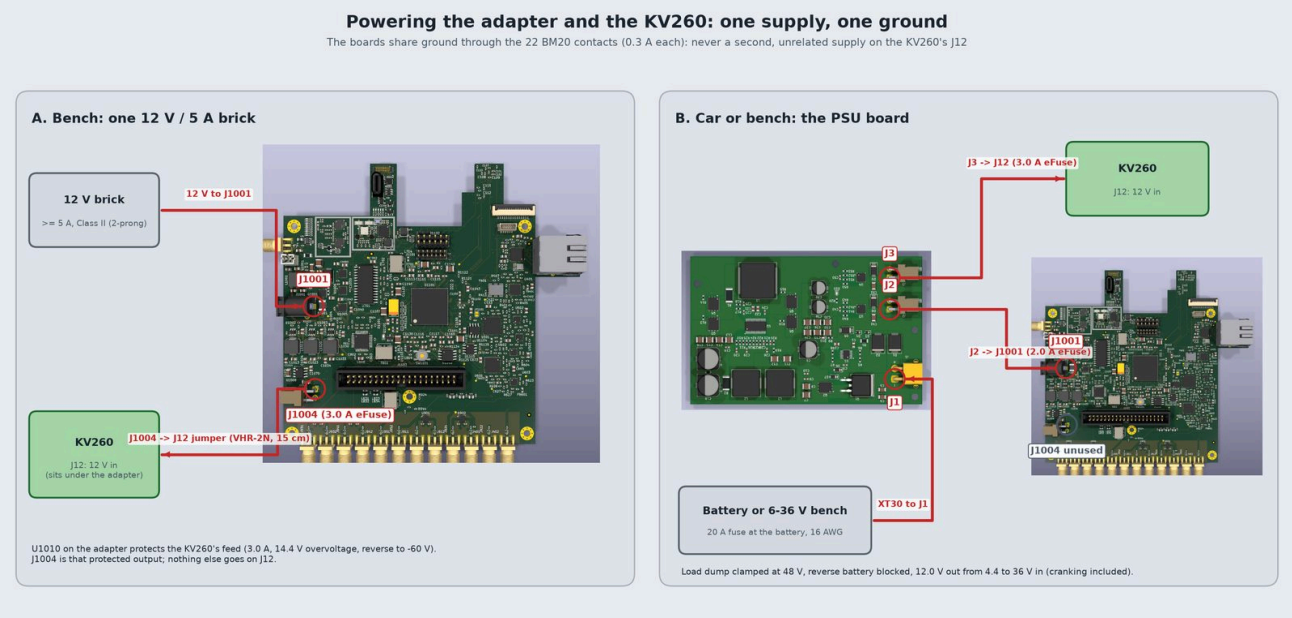
No.	Ref	Side	Part	Sheet	Function
46	U601	top	AD9253BCPZ-125	ADC_SDR	14-bit quad ADC, two channels used: SDR receive A and HF (C)
47	U602	top	AD8352ACPZ	ADC_SDR	Driver for the AD9253 channel A
48	U603	top	AD8352ACPZ	ADC_SDR	Driver for the AD9253 channel B (HF)
49	U701	top	AD9708AR	DAC_RADAR	8-bit 125 MSPS DAC: the radar chirp
50	U801	top	AD9767ASTZ	DAC_SDR	Dual 14-bit 125 MSPS DAC: SDR transmit A and HF
51	U901	top	M3SWA2-34DR+	ROUTING	SW1: SDR_RX_A or AERIS_IF_A to the AD9253 channel A
52	U902	top	M3SWA2-34DR+	ROUTING	SW2: AERIS_IF or the VHF/UHF front end to the AD9484
53	U903	top	M3SWA2-34DR+	ROUTING	SW3: the AD9767 DAC1 to SDR_TX_A or AERIS_TX_A
54	U904	top	M3SWA2-34DR+	ROUTING	SW4: the AD9708 to AERIS_TX or SDR_TX_WB
55	U1001	top	LMR33630ADDA	POWER	+12V to +5V0 buck, 3 A
56	U1002	top	TPS563201	POWER	+5V0 to +3V3_D buck, 3 A (Rev08 audit, P5)
57	U1003	top	TPS562201	POWER	+5V0 to +2V5 buck (FPGA LVDS banks, feeds +1V8_A)
58	U1004	top	TPS562201	POWER	+5V0 to +1V0 buck (FPGA core)
59	U1005	top	TPS7A8300RGR	POWER	+2V5 to +1V8_A LDO (the ADCs' analogue supply)
60	U1006	top	TPS7A8300RGR	POWER	+3V3_D to +1V8_D LDO (FPGA VCCAUX, the ADCs' outputs)
61	U1007	top	TPS7A8300RGR	POWER	+5V0 to +3V3_A LDO (the DACs' analogue supply)
62	U1008	top	LM2663M	POWER	-3V3 charge pump (the RF switches' negative supply)
63	U1009	bottom	LM74502-Q1	POWER	Input protection controller: reverse battery and over-voltage cut-off, with Q1001/Q1003
64	U1010	bottom	TPS26631PWPR	KVPWR	KV260 12 V output eFuse: 8.0 V UVLO, 14.4 V OVP, 3.0 A limit (R1043 6.04 kohm, 2.77 to 3.19 A), auto-retry, with Q1010/Q1011 reverse protection
65	U1301	top	SPF5043Z	RX_VU	VHF/UHF low-noise amplifier
66	U1302	top	PE4259	RX_VU	LNA bypass switch, input side
67	U1303	top	PE4259	RX_VU	LNA bypass switch, output side
68	U1304	top	PE42442	RX_VU	Preselector A: band selection, input side
69	U1305	top	PE42442	RX_VU	Preselector A: band selection, output side
70	U1306	top	SKY13418-485LF	RX_VU	Preselector B, input side (straight, UHF low-pass, ADS-B)
71	U1307	top	SKY13418-485LF	RX_VU	Preselector B, output side
72	U1308	top	PE4259	RX_VU	Direct or converted path
73	U1309	top	PE4259	RX_VU	Direct or converted path, after the converter
74	U1310	bottom	SPF5043Z	RX_VU	IF amplifier
75	U1311	bottom	PE4312	RX_VU	Digital attenuator, 0-31.5 dB
76	U1312	top	RFFC5072	RX_VU	Synthesiser and mixer: converts 300 MHz-3 GHz down to the IF (170-300 MHz not covered)
77	U1313	bottom	TCA6416ARTWR	RX_VU	I/O expander 0x20: the front end's switches, bias tee and converter control
78	U1314	top	AP22652W6-7	RX_VU	Bias-tee current limiter for J961 (125 mA)
79	U1315	bottom	LP5907MFX-2.8	RX_VU	+2V8_RF LDO for the front end (Rev08 audit, P8)
80	U1501	bottom	TCA6416ARTWR	STATUS	I/O expander 0x21: the status LEDs
81	U1502	top	CH340X	STATUS	USB to UART bridge for the debug console
82	U1503	top	USBLC6-2SC6	STATUS	ESD on the USB data lines
83	U1504	top	LP5907MFX-3.3	STATUS	3.3 V LDO for the USB bridge, from the cable
84	U1505	bottom	SN74LVC1G17DCKR	STATUS	GPS PPS Schmitt buffer, drives J1502 pins 12 and 4
85	U1506	bottom	TCAN3403DDFRQ1	STATUS	Vehicle CAN transceiver on J1503 pins 3 and 2, listen-only by default; TXD from the NOR pair Q1530/Q1531, RXD divided to 1.2 V for J9 pin 8
86	Y401	top	Si549 LVPECL 3V3 pinout C	CLOCK	Programmable master oscillator, 400 or 500 MHz
87	Y1201	top	25MHz	CONTROL	Crystal for the Ethernet PHY
88	Y1301	top	26MHz 1XXD26000MAA	RX_VU	TCXO, the RFFC5072's reference
89	FL1301	top	TA1090EC	RX_VU	1090 MHz SAW filter (ADS-B path)
90	FL1302	top	HFCN-1000+	RX_VU	High-pass after the mixer
91	FL1303	top	LFCN-1000+	RX_VU	Low-pass, UHF preselector
92	T701	top	ADT2-1T+	DAC_RADAR	AD9708 output balun

No.	Ref	Side	Part	Sheet	Function
93	`T801`	top	ADT2-1T+	DAC_SDR	AD9767 DAC1 output balun
94	`T802`	top	ADT2-1T+	DAC_SDR	AD9767 DAC2 output balun
95	`T1301`	top	TC1-1-13M+	RX_VU	Mixer input balun
96	`T1302`	top	TC4-1W+	RX_VU	Mixer output balun

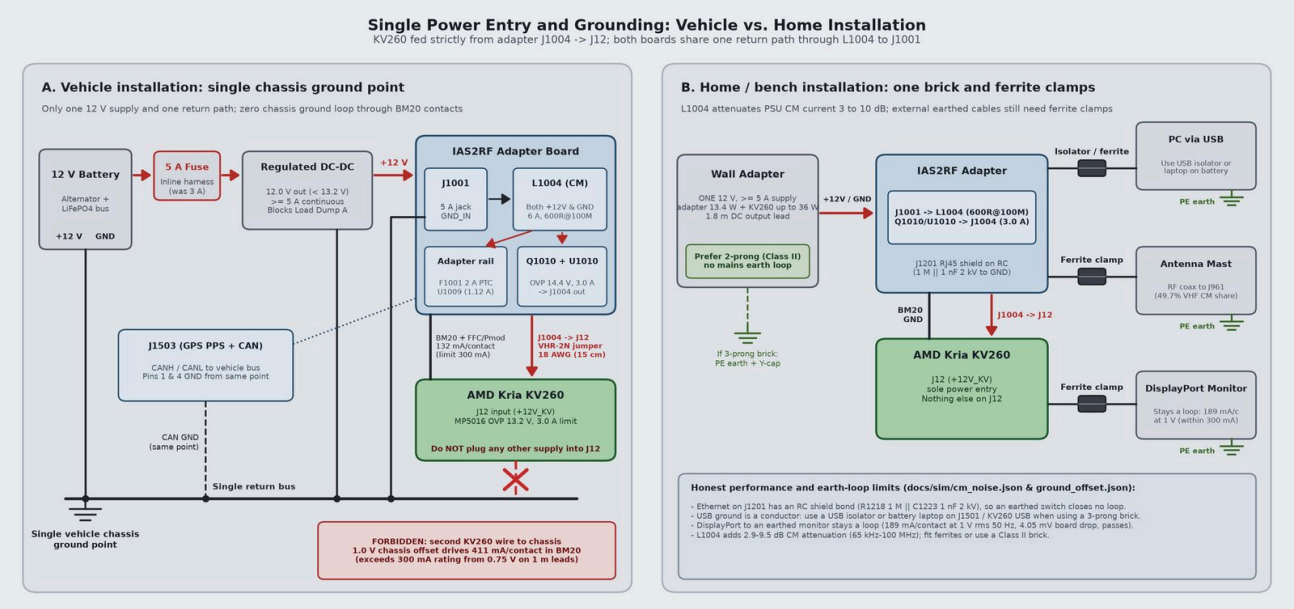
5. Typical uses

Use	Connect	Set
Radar with AERIS-10	Ribbon on `J1103`; chirp `J941` to AERIS's transmit input, AERIS's IF to `J921`; IAS1 on the KV260; 12 V on `J1001`	Default switch positions. The Kria runs the radar pipeline; R5F core 1 scans the beams
HF SDR	Antenna or HF front end on `J951`; transmit from `J952`	No switch in either path; 0-30 MHz, the 30 MHz low-pass on receive
VHF/UHF reception	Antenna on `J961` (active antenna: set `JP1301`, then the bias on in software)	SW2 to its second throw (the front end); band and gain from the Kria
SDR on the 14-bit converters	`J911` receive, `J931` transmit	Default positions of SW1 and SW3
Wideband SDR	`J942` transmit; `J922` receive only after swapping `C926`/`C927`	SW4 to its second throw
Camera on the KV260	IAS camera module on `J103`, as on the carrier's `J7`	Nothing on this board; the camera talks to the SOM as before
Standalone over Ethernet	RJ45 `J1201` to a PC; 12 V on `J1001`	The FPGA streams over UDP without the Kria
Debug	USB-C `J1501` (lid off), 115,200 8N1; JTAG `J1101`	Boot banner, one status line a second, `r`/`w` register commands
GPS time	GPS receiver on `J1503`; FFC from `J1502` to the KV260's `J9`	`kria_pps` timestamps the pulse; R5F core 0 disciplines the converters' clock to it

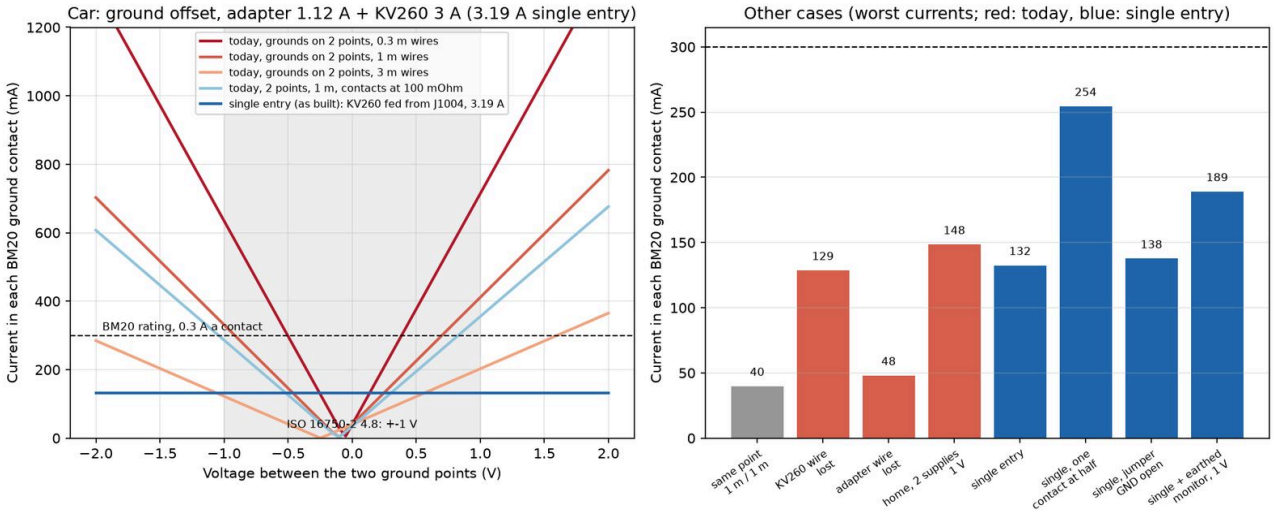
6. Powering the KV260 together with the board



The two ways to power the boards



Power and grounding wiring



Ground offset and earth loops

The two boards share their ground through the BM20 connectors (22 contacts rated 0.3 A each), so they must be fed from **one supply and one ground point**; two unrelated supplies (two earthed bricks, two car ground points) drive current through those contacts (AUDIT_Rev08 section 6). There are two ways to do it:

	Adapter's `J1001`	KV260's `J12`	Adapter's `J1004`
A. The PSU board (vehicle or bench; recommended)	from the PSU's `J2`	from the PSU's `J3`	unused (its branch can be left unfitted)
B. One 12 V / 5 A brick (bench)	the brick	jumper from `J1004`	to `J12`

Never plug a second brick into `J12`. Option B in detail: feed the entire two-board module through `J1001` alone. Connect `J1004` (right-angle JST VH at the back edge; pin 1 `+12V_KV`, pin 2 `GND`) to the KV260's barrel jack `J12` with the short 18 AWG jumper (VHR-2N, 15 cm to a 5.5 x 2.5 mm centre-positive plug) and **plug nothing else into `J12`**. Combined draw at `J1001` (5 A rating) and `L1004` (6 A rating) is 1.89 A typical, 4.12 A at the KV260's 3.0 A brick rating (1.12 A adapter plus 3.0 A KV260), and 4.31 A worst case at `U1010`'s +7 % limit (3.19 A from `R1043` 6.04 kohm).

With this single entry, **the KV260's own DC return runs through the BM20 ground contacts (`J101`/`J102`) by design**: the 22 parallel BM20 ground contacts plus the FFC and Pmod conductors present 1.3 mOhm (1.29 mOhm) against the jumper's 33 mOhm (33.1 mOhm), so 96 % of the KV260's return crosses the BM20 link. That is why `U1010` limits the KV260 to its brick's 3 A rating (2.98 A nominal, 2.77 to 3.19 A).

The recommended way, in a vehicle and on a bench: the PSU board (**PSU_SPEC**). It takes the battery (or a 6 to 36 V bench supply) and feeds the adapter's `J1001` through its `J2` and the KV260's `J12` through its `J3`, each by its own 18 AWG

cable from one ground. That carries the KV260's return in its own cable: 38 mA a BM20 contact at the worst load (66 mA with unequal cables, 178 mA with one contact at a third of the others' resistance), against 132 mA through the adapter's own single entry. With it, the adapter's KV260 branch (`U1010` to `J1004`) can stay unfitted. It runs through ISO 16750-2 Load Dump A and B, jump start and cranking Levels I, II and IV; only disconnecting the battery, a reverse battery and Level III cranking reset the module.

- In a vehicle:
- **The PSU board on the battery** (16 AWG, a 20 A fuse at the battery), or, without it, a 4.3 to 36 V buck-boost converter (12.0 V, under 13.2 V, 60 W) with a 36 V surge limiter ahead of it on `J1001`: never a 13.6 V stabiliser, which trips the KV260's `MP5016H` OVP (`POWER_SPEC` §1.4).
- **Never run a second chassis ground wire to the KV260** (by wire, mounting strap or shield): its only ground is its supply cable, from the PSU board's `J3` or the adapter's `J1004`. Return the CAN/GPS cable ground (`J1503` pins 1 and 4) from the same chassis ground point as the supply's negative lead.
- At home / on a bench:
- Use one 12 V / 5 A wall adapter on `J1001`, preferably a two-prong (Class II, double-insulated) brick with no mains earth pin.
- Ethernet on `J1201` to an earthed PC or switch no longer closes a DC or 50 Hz earth loop (`J1201`'s shield goes to ground through `R1218` 1 Mohm in parallel with `C1223` 1 nF 2 kV).
- **USB does close a ground loop** (its ground is a cable conductor): when connecting the debug USB-C `J1501` or the KV260's USB to an earthed PC while running an earthed supply, use a USB isolator or a laptop on battery.
- DisplayPort to an earthed monitor stays a loop (189 mA per BM20 contact with 1 V rms 50 Hz between earths, inside the 300 mA rating); fit clip-on ferrites on earthed cables.

Inter-board BM20 ground currents (`_work/power/ground_offset.py`, `docs/sim/ground_offset.json`, 0.30 A per-contact rating):

Installation / Fault case	Inter-board link current	Per BM20 contact	Against 0.30 A rating
Separate grounds, same point (1.0 m / 1.0 m)	-0.93 A	40 mA	Pass
Separate grounds, same point (0.3 m / 2.0 m)	-1.96 A	84 mA	Pass
Separate grounds, 1.0 V chassis offset (1 m typ)	10.2 A	411 mA	Fail (exceeds 0.30 A from 0.75 V)
Separate grounds, 1.0 V offset (1 m, max contact R)	9.9 A	355 mA	Fail (exceeds 0.30 A from 0.85 V)
Separate grounds, 1.0 V offset (0.3 m leads, typ)	17.7 A	714 mA	Fail (exceeds 0.30 A from 0.40 V)
Separate grounds, 1.0 V offset (3.0 m leads, typ)	5.0 A	203 mA	Pass (0.30 A at 1.60 V)
Separate grounds, KV260 ground wire lost	3.00 A	129 mA	Pass (surviving jack 4.12 A)
Single entry, typical KV260 load (0.92 A)	-0.89 A	38 mA	Pass
Single entry, at `U1010` limit (3.19 A)	-3.09 A	132 mA	Pass (independent of chassis offset)
Single entry, contacts at 100 mOhm max	-2.88 A	109 mA	Pass
Single entry, one contact at half resistance (3.19 A / 0.92 A)	-3.09 A / -0.89 A	254 mA / 73 mA	Pass
Single entry, one contact at a third of the others' resistance (2 A)		219 mA	Pass
Single entry, one contact at a third (3.19 A; the other 21 typical / at 100 mOhm max)	-3.09 A	352 mA / 306 mA	Over 0.30 A, pass on heat: 1.86 mW / 3.13 mW in that contact
Single entry, jumper ground contact open (typ / max R)	-3.21 A	138 mA / 122 mA	Pass
Home, single entry, earthed monitor 50 Hz (1.0 V / 0.1 V)	3.27 A / 0.33 A loop	189 mA / 133 mA	Pass (4.05 mV / 405 uV adapter drop)

The 0.30 A rating is a heating limit (Hirose derives it from the temperature rise under current). When one contact takes more than its share it is because its resistance is low, so its heat stays small: 3.13 mW at worst, against 9.0 mW for a contact at its 100 mOhm maximum at 0.30 A, and 25 mW in all 22 against 59 mW (docs/AUDIT_Rev08.md section 6.3).

Levels, bands and the register map: **ROUTING_SPEC**, **RX_VU_SPEC**, **SIGNAL_INTEGRITY**, **FPGA_GATEWARE**, **LINK_PROTOCOL**.

Part II: Dual-FPGA Gateware & XSim Verification

10 technical document(s)

Source: docs/FPGA_GATEWARE.md

FPGA gateware: Artix-7 front end and Kria KV260 Zynq UltraScale+ PL

Complete RTL, post-route Vivado 2026.1 implementation, and full-system XSim co-simulation documentation for the dual-FPGA **KV260-IAS2RF** platform (licensed under **Apache License 2.0**, with `fpga/third_party/aeris/` retained under MIT from `AERIS-10 / PLFM_RADAR`).

1. Dual-FPGA Hardware/Gateware Partition

```
+-------------------------------------------------+     IAS1 (J101 -> J8, 5 LVDS pairs + 4 SE 1.8V)     +-------------------------------------------------+
|     ADAPTER FRONT-END FPGA (U1101)              | ================================================> |        AMD KRIA KV260 SOM (XCK26-SFVC784-2LV-c)  |
|     Xilinx Artix-7 XC7A50T-FTG256-2             |  2x 1.0 Gb/s 64b/66b Uplink  (LINK_RX_D0/D1 + CLK)  |                                                  |
|                                                 | <================================================ |  PL (ia2rf_k26_bd):                              |
|  · AD9484 400 MSPS Radar ADC + AERIS-10 DDC (79DSP)|  1x 1.0 Gb/s 64b/66b Downlink (LINK_TX_D0 + CLK)    |   · kria_pl_link_0 (ISERDESE3+IDELAYE3+PCS+UART1)  |
|  · AD9253 2x 62.5/50 MSPS SDR ADC + Dual DDC (30DSP)|  + HK I2C (1.8V), FPGA_PROG_B, FPGA_IRQ             |   · axi_dma_0 (64-bit MM2S/S2MM -> HP0_FPD)        |
|  · AD9708 LFM Chirp TX + AD9767 Dual 14b SDR TX  |                                                  |   · axi_smc_hp0 + axi_smc_ctrl + EMIO SPI/I2C      |
|  · 8x ADAR1000 Beamformer + 4x M3SWA2-34DR+ SW   |     Dedicated 1000BASE-T Ethernet (U1201 -> J1201)  |                                                  |
|  · Dual-Path Mux + Debug UART (115.2k 8N1 Pmod)  | -------------------------------------------------> |  PS8 (Quad Cortex-A53 @ 1.33 GHz + 4 GB DDR4):   |
|                                                 |  192.168.10.2 UDP Port 0x4952 -> KV260 J10 (GEM3)   |   · Pulse compression, Doppler FFT, CFAR, Tracking |
| Post-route figures: section 2.4                 |  + Pmod J1102<->J2 EMIO UART1 (/dev/ttyPS1)         |   · SDR demodulation & Linux host IO             |
+-------------------------------------------------+     Failsafe Pmod J1102 <-> Carrier J2 (EMIO SPI0)   +-------------------------------------------------+
```

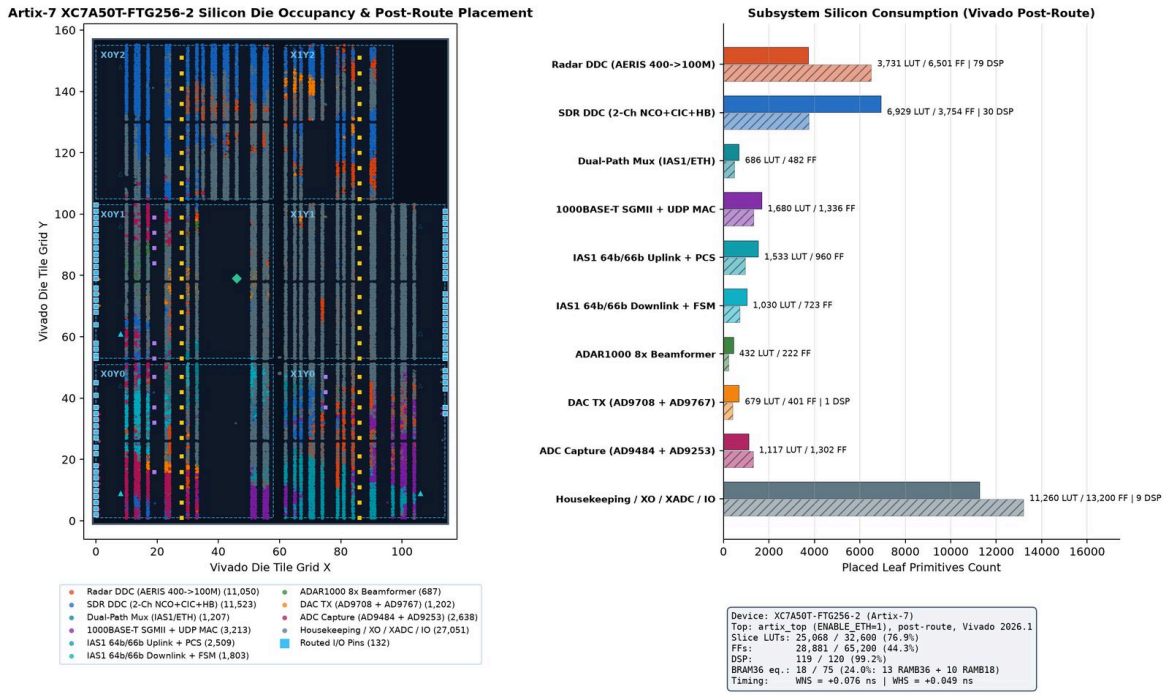
High-resolution vector schematics & silicon die renders (`SVG` / `PDF` / `4K PNG`) are in `fpga/` of the high-res archive, a release asset.

2. Artix-7 XC7A50T-FTG256-2 (`artix_top`)

Top-level file: **`fpga/artix/top.v`**, constrained by **`fpga/artix/xc7a50t.xdc`** and built with **`fpga/artix/build_rev06.tcl`** (`ENABLE_ETH = 1'b1`).

2.1 Vivado Post-Route Silicon Die Floorplan

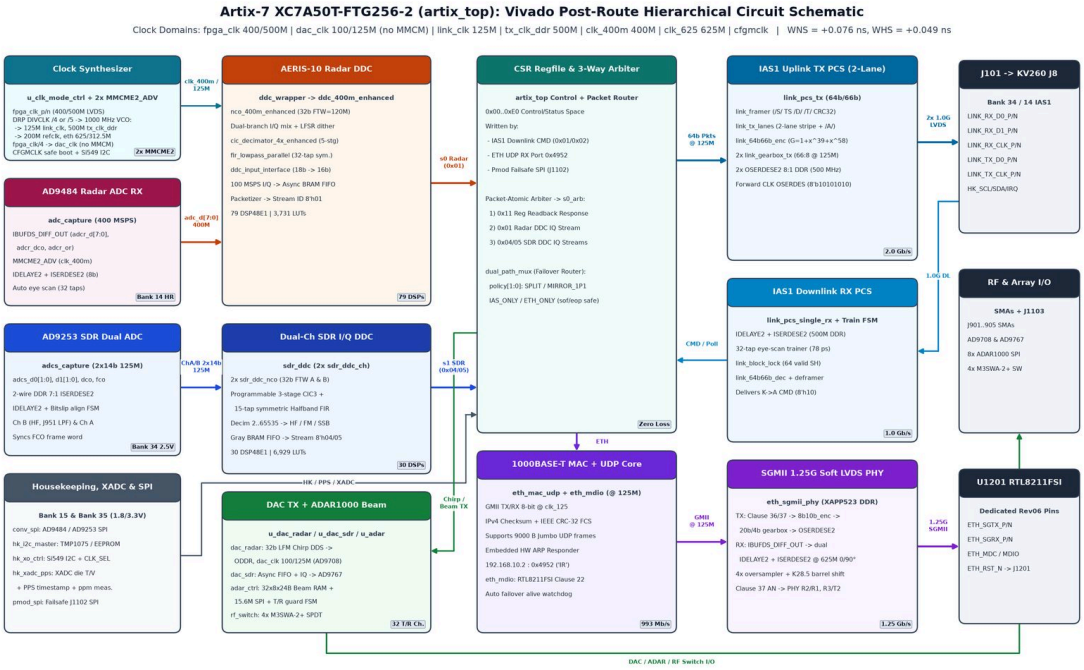
The post-route floorplan below is plotted directly from Vivado 2026.1 placed leaf cells across Clock Regions `X0Y0..X1Y2` (`_work/fpga_views/artix7_die_data.json`):



Artix-7 XC7A50T-FTG256-2 Silicon Die Floorplan

- **Vector / 4K Downloads:** `fpga/artix7_silicon_floorplan_4k.png`, `.svg` and `.pdf` in the high-res archive

2.2 Hierarchical Circuit Schematic



Artix-7 XC7A50T-FTG256-2 Vivado Hierarchical Circuit Schematic

- **Vector / 4K Downloads:** `fpga/artix7_vivado_schematic_4k.png`, `.svg` and `.pdf` in the high-res archive

2.3 Complete Module Inventory (`fpga/artix/` & `fpga/link/`)

Module	File(s)	Clock Domain(s)	Function & Key Implementation Details
Top, Clocks & Mode Ctrl	`fpga/artix/top.v` + `clk_mode_ctrl.v`	`cfgmclk`, `fpga_clk` (500M/400M), `dac_clk` (125M/100M), `link_clk` (125M)	`STARTUPE2` `CFGMCLK` safe-boot sequencer, `MMCME2_ADV` DRP (`DIVCLK_DIVIDE 5<->4` for `500<->400 MHz`), A-1 radar reset gate (`radar_dis_cfg` when `500 MHz`), non-MMCM 2-bit Johnson ÷4 `dac_clk`, Ethernet `MMCME2_ADV`, `0x00..0xFC` CSR regfile (4-master arbiter), 3-way uplink arbiter
Radar ADC Capture	`fpga/artix/adc_capture.v`	`adcr_dco` (200M) -> `clk_400m` (400M) / `clk_100m` (100M)	Private `MMCME2_ADV` (`1000 MHz` VCO), `DCO_INVERT=1` (`N14=DCO_N, P14=DCO_P`), `IBUFDS` + `IDELAYE2` + `IDDR` 8-bit DDR capture (`400 MSPS`, closed at 400 MSPS only; held in reset at 500 MHz per A-1) + 32-tap eye scanner
AERIS-10 Radar DDC	`fpga/artix/ddc_wrapper.v` + `fpga/third_party/aeris/`	`clk_400m` (400M), `clk_100m` (100M), `link_clk` (125M)	Verbatim `PLFM_RADAR` (`62d4c55`, MIT) 400 MSPS -> 100 MSPS I/Q DDC (`nco_400m_enhanced`, `cic_decimator_4x_enhanced`, `fir_lowpass_parallel`, `ddc_input_interface`), `POST_DECIM` (by 4: two multiplierless anti-alias half-bands, `ddc_hb4.v`), CPI mark from `dac_radar`'s chirp starts, 128-word async FIFO (10 µs at 25 MSPS), packetizer (`stream_id = 8'h01`, 512-byte packets); controlled via `RADAR_CTRL[0]` (`0xE4`)
SDR Dual ADC Capture	`fpga/artix/adcs_capture.v`	`adcs_dco` (`500 MHz` @ `500M` / `400 MHz` @ `400M` DDR) -> `adcs_clk_div` (125 / `100 MHz`)	AD9253 **one-lane 16-bit DDR wordwise** (`0x21=0x40`, `0x0B=0x07`, `DCO = 8*f_S`): `ISERDESE2 1:8` DDR `NETWORKING` + `IDELAYE2` + bitslip FSM locked to `FCO`, crosses via 16-entry Gray FIFO to `BUFG` `adcs_ddc_clk` (`83.333 MHz` MMCM `CLKOUT3`)
Dual-Ch SDR DDC	`fpga/artix/sdr_ddc.v`	`adcs_ddc_clk` (83.333M), `link_clk` (125M)	Two independent channels (`8'h04` Ch A on `J911`/`J912`, `8'h05` Ch B on `IF_RX_C J951` enabled at reset for switch-free HF) sampling at **`62.5 MSPS`** (`500M`) or **`50.0 MSPS`** (`400M`), each with 32-bit NCO + 3-stage CIC3 + 15-tap symmetric halfband FIR + programmable decimation `2..65535` + Gray async BRAM FIFO
Radar Chirp DAC TX	`fpga/artix/dac_radar.v`	`dac_clk` (125M/100M), `link_clk` (125M)	32-bit LFM up/down chirp DDS (`FTW(n) = f0 + n*df`) + programmable `pulse_len` & `pri_len` + `ODDR` clock forward from non-MMCM ÷4 `dac_clk` (`D1=0, D2=1` center-aligned) to `AD9708` (`U701`)
SDR Interleaved DAC TX	`fpga/artix/dac_sdr.v`	`dac_clk` (125M/100M), `link_clk` (125M)	Unpacks 64-bit downlink `8'h12` (or long `8'h10`) IQ frames across async FIFO -> 14-bit `IQWRT`/`IQSEL`/`IQCLK` interleaved bus on non-MMCM `dac_clk` to `AD9767` (`U801`); `hf_dac2_mode=1` default routes primary `I` to `DAC2 / IF_TX_C J952` (`dac1_mute` clamps `DAC1`)

Module	File(s)	Clock Domain(s)	Function & Key Implementation Details
8x ADAR1000 Beamformer	`fpga/artix/adar_ctrl.v`	`link_clk` (125M) -> `15.625 MHz` SPI	`32 beams x 8 chips x 24 bytes` BRAM table, broadcast/per-chip Mode-0 4-wire SPI (`J1103`), hardware `beam_strobe` loader, programmable `guard_pre` / `guard_post` T/R switching deadtime
RF Switch Matrix	`fpga/artix/rf_switch.v`	`link_clk` (125M)	Glitch-free control of the four `M3SWA2-34DR+` SPDT switches (`U901..U904`) with programmable `1 us` (`125 cyc`) settle lockout
1000BASE-T SGMII PHY	`fpga/artix/eth_sgmii_phy.v` + `fpga/artix/eth_8b10b.v`	`625M` (0°/90°), `312.5M` (0°/45°), `125M`	XAPP523-style 4x `ISERDESE2` oversampling RX (`IDELAYE2` + `K28.5` barrel shifter), `10:1` `OSERDESE2` TX, IEEE 802.3 Clause 37 SGMII AN, `eth_mdio.v` Clause 22 open-drain management to `RTL8211FSI` (`U1201`)
UDP/IPv4 MAC + Dual-Mux	`fpga/artix/eth_mac_udp.v` + `fpga/artix/dual_path_mux.v` + `fpga/artix/eth_sdr_pkt_gen.v`	`link_clk` (125M)	Full GMII MAC with HW ARP & ICMP echo responders, Jumbo UDP frames (`192.168.10.2:0x4952`), zero-loss packet-atomic `dual_path_mux` (`SPLIT`, `MIRROR_1P1`, `IAS_ONLY`, `ETH_ONLY`)
IAS1 64b/66b PCS	`fpga/link/` (`link_*.v`)	`link_clk` (125M), `tx_clk_ddr` (500M), `dl_rx_clk` (125M)	2-lane `2.0 Gb/s` uplink TX (`OSERDESE2` 8:1 DDR + `16:66` scrambler + `CRC-32`) and 1-lane `1.0 Gb/s` downlink RX (`IDELAYE2` 32-tap eye trainer + `64b/66b` descrambler + deframer)
Housekeeping & XADC/PPS	`fpga/artix/conv_spi.v`, `hk_i2c_master.v`, `hk_xo_ctrl.v`, `hk_xadc_pps.v`, `pmod_spi.v`	`cfgmclk`, `link_clk` (125M)	Auto-init 3-wire SPI for `AD9484`/`AD9253` (1-lane 16b DDR), open-drain `TMP1075`/`M24C02` I2C polling, `Si549` fractional N-delta I2C (`±50 ppm` `ENABLE_ETH` clamp) + `CLK_SEL`, 12-bit XADC temp/voltage monitor, 1-PPS period/ppm frequency counter & 64-bit ns timestamping, failsafe Pmod SPI slave
Debug UART Monitor (G-1)	`fpga/artix/dbg_uart.v`	`link_clk` (125M, constant in `400` & `500 MHz` modes)	`115,200` baud 8N1 (`div=1085` -> `115,207.4` baud, `+0.0064%` err) on `pmod_spare1` RX (`G15`, `PULLUP`) / `pmod_spare2` TX (`G11`): boot banner, 1 Hz `key=value` `STAT` line, interactive `r`/`w`/`s`/`h` CLI as 4th lossless CSR master

2.4 Artix-7 Post-Route Resource & Timing Closure (`reports_rev06/`)

<!-- fpga-figures:begin -->

Design (Vivado 2026.1)	Device	LUTs	FFs	BRAM36 eq.	DSPs	WNS / WHS	Failing endpoints	Reports
`artix_top`	XC7A50T-FTG256-2	25,279 (77.5 %)	28,970 (44.4 %)	18.0 (24.0 %)	119 (99.2 %)	+0.007 / +0.033 ns	0 of 83,391	`artix/reports_rev06/` from `build_rev06.tcl`
`ias2rf_k26_bd_wrapper`	XCK26-SFVC784-2LV-c	53,336 (45.5 %)	46,896 (20.0 %)	44.0 (30.6 %), 1 URAM	229 (18.3 %)	+1.043 / +0.010 ns	0 of 188,554	`kria/reports/` from `bd.tcl`

Post-route, generated from the Vivado reports by `_work/fpga_figures.py` (artix_top: Thu Nov 19 04:24:55 2026; ias2rf_k26_bd_wrapper: Thu Nov 19 09:53:51 2026). <!-- fpga-figures:end -->

<!-- fpga-artix-hier:begin -->

Hierarchy	Total LUTs	FFs	RAMB36	RAMB18	DSP48E1	Role
`artix_top` (total)	**25,279 (77.5 %)**	**28,970 (44.4 %)**	**13**	**10**	**119 (99.2 %)**	Everything below plus the top level's own logic
`u_sdr_ddc`	5,644	3,754	2	4	30	Dual-channel wideband SDR DDC (62.5 / 50.0 MSPS)
`u_ddc`	3,400	6,496	0	0	79	400 -> 100 -> 25 MSPS AERIS-10 radar DDC, tunable NCO (G-4), anti-alias half-bands and CPI mark (G-8)
`u_d2` + `u_d2_peak`	4,373	6,649	0	4	8	Rev08 G-7 D2: the 500 MSPS AD9484 path (four-lane NCO, mixer, pruned CIC5, `ddc_hb4`) and its AGC peak detector
`u_dbg_uart`	1,787	653	0	0	0	G-1 8N1 debug UART monitor, banner, 1 Hz `STAT` and the fourth CSR master
`u_ul_pcs_tx`	1,281	959	0	0	0	2-lane `64b/66b` IAS1 uplink PCS
`u_fe_agc` + `u_adcr_peak`	705	556	0	0	1	Rev08 G-2 to G-6: front-end AGC and its AD9484 peak detector (the expander and RFFC5072/PE4312 sequencer logic is flattened into the top level)
`gen_rev06_eth.*`	1,995	1,870	8	1	0	`1000BASE-T` SGMII + UDP MAC + dual-path failover
`u_dl_pcs_rx` + `u_dl_train_fsm`	787	723	0	0	0	1-lane 1.0 Gb/s IAS1 downlink + eye trainer
`u_xadc_pps` + `u_hk_i2c` + `u_clk_mode_ctrl` + `u_pmod_spi`	2,513	2,274	0	0	0	Safe-boot MMCM DRP / Si549, XADC, 1-PPS, I2C, Pmod SPI

Hierarchy	Total LUTs	FFs	RAMB36	RAMB18	DSP48E1	Role
`u_adc_cap` + `u_adcs_cap` + `u_conv_spi`	1,122	1,009	0	0	0	High-speed LVDS ADC capture and 3-wire converter init
`u_dac_radar` + `u_dac_sdr` + `u_adar_ctrl` + `u_rf_switch`	914	624	3	1	1	Non-MMCM DACs, `8x ADAR1000` beamformer, RF switches

<!-- fpga-artix-hier:end -->

- **Timing (`fpga/artix/reports_rev06/timing_summary.rpt` & `pulse_width.rpt`, with post-route `phys_opt_design`):** Overall design worst slacks are `WNS = +0.007 ns` (`0 / 83,391` failing setup endpoints), `WHS = +0.033 ns` (`0 / 82,906` failing hold endpoints), and `WPWS = +0.008 ns` (`0 / 29,834` failing pulse-width endpoints) (Rev08 final re-audit, 19 November; the per-clock figures below are from the build of 18 November). Two changes closed it after the audit's gates had pushed it to `-0.186 ns`:
- **`adc_capture`'s eye finder** rotates its pass mask instead of indexing it with `find_k`, which removes a 32:1 mux in front of `best_len`'s enable on `clk_trn_400`.
- **The IDDR pipe flops take the IDDR's own (falling) edge** when the DCO is inverted. The ILOGIC-to-fabric route gets a full cycle at 500 MSPS instead of half; the rising-edge users see the data in the same cycle as before.

The NCO reset `rst_n_400_nco` in the AERIS DDC is also capped at a fanout of 8 from `xc7a50t.xdc`. `tb_adc_ddc` gives the same eye (29) and taps; `tb_system` passes at 500 and 400 MHz. `build_rev06.tcl` uses `place_design -directive AltSpreadLogic_high` so the 119/120 DSP48E1s spread cleanly across clock regions, and runs post-route `phys_opt_design` passes while setup slack is below `50 ps`. Per-clock-group closure:

- **Build flow (`build_rev06.tcl`):** the post-place `phys_opt_design` runs an explicit pass list, `-fanout_opt -placement_opt -rewire -critical_cell_opt -critical_pin_opt -retime -shift_register_opt -bram_register_opt -hold_fix`, that is the default set without `-dsp_register_opt`. That pass pulled the AERIS mixer's `AREG` out of the DSP48 into a slice and left a fabric-to-multiplier path at `-0.146 ns` in the `2.5 ns` cycle. The post-route `phys_opt_design` runs with `-directive AggressiveExplore`: the AERIS CIC's combs sit within about `0.05 ns` of the `400 MHz` cycle and moved by that much between placements. `adc_peak`'s 128-bit window registers take power-up values and sit outside the reset branch (inside it, the reset still reached all 384 flip-flops as a hold condition). In the AERIS DDC the FIR output CDCs have their own reset copies. With G-7 the device is at 77 % of its LUTs and three more paths needed structure rather than placement luck: the AERIS CIC's comb stages 1 to 4 are whole 28-bit subtracts under a 4-cycle multicycle path (each loads once per output sample, 4 cycles after its source; bit-exact, 7 `clk_400m` cycles more latency), the AERIS DDC takes the ADC data through one more `clk_400m` register, and `fe_ctrl`'s step table has two cycles (`S_PREP2`, a 2-cycle multicycle path). The AERIS input register keeps the ADC MSB inverted, so the offset to two's complement inversion folds into it and the flop drives the mixers' 26 DSP48 A pins without a LUT, and the AD9484 IDDR pipe flops have no reset (the FIFO write is gated by `q_pipe_valid`), so each sits next to its ILOGIC for the half-cycle path at `500 MSPS`. The AERIS NCO's phase dither (17 Nov) adds its carry into the 8 address bits one stage later than the byte add that produces it: as one 16-bit carry chain in one stage it missed `400 MHz` by `0.66 ns`. The eye-scan trainer's clock comes through a `BUFGCTRL` from `clk_200m` (400 MHz mode) or `refclk_200m` (500 MHz, D2), declared as two generated clocks `clk_trn_400` and `clk_trn_500`, physically exclusive.
- **AD9484 Radar Domain (`clk_adcr_dco` `5.000 ns` = `400 MSPS` only, Rev08 A-1):** Held in hardware reset when master clock is `500 MHz` (`RADAR_STATUS[0]`), so it is closed at `400 MSPS` (`clk_400m_unbuf` `2.500 ns`: `WNS = +0.118 ns`, `WHS = +0.075 ns`, `WPWS = +0.396 ns`; the trainer's `clk_trn_400`: `WNS = +0.138 ns`; `clk_100m_unbuf`: `WNS = +0.157 ns`; `clk_adcr_dco`: `WNS = +0.356 ns`). At `500 MHz` the G-7 D2 path takes the AD9484 instead: `clk_adcr_dco_500` (`4.000 ns`) `WNS = +0.080 ns`, its trainer clock `clk_trn_500` `WNS = +0.132 ns`.
- **AD9253 SDR Bit-Clock Domain (`clk_adcs_dco_500` `2.000 ns` & `clk_adcs_dco_400` `2.500 ns`, Rev08 A-2):** Constrained for both master modes as physically exclusive `500 MHz` (`62.5 MSPS`) and `400 MHz` (`50.0 MSPS`) DDR bit clocks: `clk_adcs_dco_500` `WPWS = +0.529 ns` (`adcs_clk_div_1` `8.000 ns`: `WNS = +2.635 ns`, `WHS = +0.085 ns`, `WPWS = +2.870 ns`); `clk_adcs_dco_400` `WPWS = +1.029 ns` (`adcs_clk_div` `10.000 ns`: `WNS = +4.635 ns`, `WHS = +0.085 ns`, `WPWS = +3.870 ns`).
- **Master / Ethernet / IAS1 Domains:** `clk_fpga_500` (`WNS = +1.409 ns`), `link_clk_unbuf` (`125 MHz`, which also runs D2: `WNS = +0.193 ns`), `adcs_ddc_clk_unbuf` (`83.333 MHz`: `WNS = +1.033 ns`), `clk_dac_500` (`125 MHz`: `WNS = +0.484 ns`), `gen_rev06_eth.clk_312p5_u` (`WNS = +0.076 ns`), `gen_rev06_eth.clk_625_0_u/625_90_u` (`WPWS = +0.008 ns`), `clk_fpga_400` (`WNS = +1.909 ns`, `clk_dac_400` `WNS = +2.484 ns`), `dl_rx_clk` (`WNS = +0.392 ns`, `clk_link_tx` `WPWS = +0.529 ns`), `clk_cfgmclk` (`WNS = +0.668 ns`; constrained at the `100 MHz` worst case of `CFGMCLK`, where `fe_ctrl` sits). (`build.tcl`, the same design with the default placement and no power reports, closed at `WNS = +0.035 ns`, `WHS = +0.054 ns` on 19 November; its reports are not kept, `build_rev06.tcl` is the build of record.)
- **Non-MMCM ÷4 DAC Clock Jitter Reduction:** Driving `dac_clk` (`125 MHz @ 500M` / `100 MHz @ 400M`) from a glitch-free 2-bit Johnson divider on `fpga_clk_bufg -> BUFG` instead of an MMCM `CLKOUT` cuts Vivado `Clock Uncertainty` from `0.165 ns`

down to **`0.035 ns`** (`4.7x` improvement) and eliminates MMCM `Discrete Jitter` (`0.124 ns -> 0.000 ns`) and `Phase Error` (`0.099 ns -> 0.000 ns`).

- **Safe-Boot & Live `400 <-> 500 MHz` Mode Switch (`clk_mode_ctrl`):** On POR, `STARTUPE2 CFGMCLK` holds `mmcm_rst = 1` while `Y401` (`Si549`) programs and settles (`>= 30.7 ms` FCAL wait), configures both MMCMs via DRP (`DIVCLK_DIVIDE = 5` for `500 MHz`, `4` for `400 MHz`), and releases `mmcm_rst` (`XO_CTRL[14] xo_boot_done`, `[12] xo_boot_err`). `clk_mode_ctrl` also drives `radar_dis_cfg` high whenever switching or operating at `500 MHz`, holding `u_adc_cap` and `u_ddc` safely in reset and automatically retraining AD9484 when returning to `400 MHz`; at `500 MHz` the G-7 path D2 (§4.3) takes the AD9484 instead. Writing `XO_CTRL[2] prog_start` switches live between `500 MHz` and `400 MHz`; during the switch, `mmcm_rst` drops `link_clk`, so IAS1 link training and SGMII MAC/PHY reset and retrain cleanly, and `dac_rst` applies a glitchless reset to `dac_radar`/`dac_sdr`. `ADPLL_DELTA_M` writes to `XO_DELTA_M` are clamped to `±50.0 ppm` (`±429553`, latched in `XO_CTRL[13] xo_delta_clamped`) when `ENABLE_ETH=1`. While the uplink retrains (`ul_tx_gate` low), `dual_path_mux` drops whole bulk packets meant for IAS1 (`ias_drain`: not written, or popped unsent if the PCS has not taken their first word) and keeps `0x11` read-backs, so the first register read after a switch returns in about `3.7 us` instead of waiting about `40 us` behind a full `1024`-word FIFO of stale data; the ETH FIFO, and so `MIRROR_1P1` and `SPLIT` failover traffic, is not affected (`tb_dual_path_drain`, `tb_clk_mode_switch rd_max`). The mux counts IAS1 healthy only while that uplink may send (`ul_tx_allow`: the downlink up and the Kria's receiver up, its `link_up` bit in the downlink's status word), so if the Kria's receiver alone drops, `SPLIT` moves IAS1 traffic onto ETH instead of draining it; before the uplink first opens after a reset, IAS1 counts as healthy (`tb_rev06` Phase 2b).
- **DRC & CDC (`drc.rpt` & `cdc.rpt`):** `0` DRC errors (`0` Critical/Error timing or methodology failures). `cdc.rpt` (`reports_rev06/`) reports `192 CDC-1`, `12 CDC-2`, `65 CDC-3`, `2 CDC-4`, `12 CDC-5`, `40 CDC-6`, `1 CDC-7`, `2 CDC-8`, `2 CDC-9`, `61 CDC-10`, `2 CDC-11`, `156 CDC-13`, `1 CDC-14`, `759 CDC-15` (covered by asynchronous clock groups & 2/3-stage Gray/toggle synchronizers across `link_clk`, `clk_cfgmclk`, `clk_adcr_dco`, `clk_adcs_dco_*`, and `clk_link_tx`). *(Top-level slice counts in `utilization.rpt` reflect Vivado cross-hierarchy LUT combining and `phys_opt_design` post-route optimization in `build.tcl` and `build_rev06.tcl`.)*
- **Vivado `report_power` (`reports_rev06/power_25c_typ.rpt` & `power_70c_max.rpt`, 8-11 layers, no airflow).** The reports are for the fitted part's grade, industrial (`-2FTG256I`, Tj 100 °C), since the final re-audit. Before that they took the commercial grade's static power and 85 °C limit, hence their "junction temperature exceeded" at 70 °C. The power budget (`_work/power_budget.py`) and the enclosure CFD keep the commercial figures of 18 November (1.25 / 1.60 W, VCCINT 0.468 / 0.776 A, VCCAUX 0.313 / 0.367 A) as an upper bound.

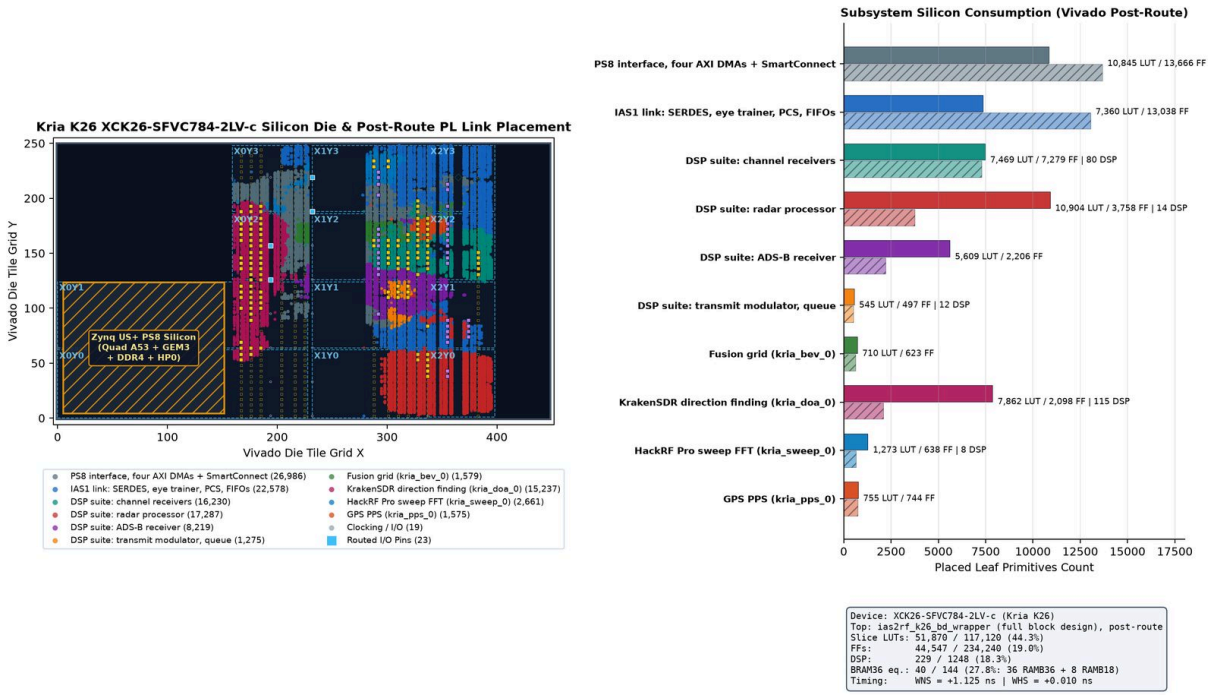
Operating Condition	Total On-Chip Power	Junction Temp (Tj)	VCCINT (1.0 V)	VCCAUX (1.8 V)
25 °C typical, industrial	**`1.223 W`**	`42.6 °C`	`0.442 A` (`0.424 A` dyn / `0.019 A` static)	`0.313 A` (`0.299 A` dyn / `0.013 A` static)
70 °C maximum process, industrial	**`1.446 W`**	`90.8 °C`	`0.632 A` (`0.425 A` dyn / `0.208 A` static)	`0.342 A` (`0.299 A` dyn / `0.042 A` static)

- **Rev08 Audit Inter-Board & RF Safety Gates (Power-Domain Rule: no FPGA sources current into an unpowered board):**
- `FPGA_IRQ` (`fpga/artix/top.v`): gated by `dl_up_sync[1]` (`link_trained`), so an unpowered K26 never receives clamp current when an alert is asserted (`tb_artix_top`, mutation `irq_ungated`).
- `PMOD_MISO` (`fpga/artix/pmod_spi.v`): `pmod_miso_oe = cs_active & kria_present`; `kria_present` sets only after `PMOD_CS` stays continuously high for `>= 1 ms` (`125,000` cycles) and clears if `PMOD_CS` stays low `> 100 ms` (`12,500,000` cycles) with no SCLK edge (`tb_pmod_spi`, mutation `miso_always_oe`). `xc7a50t.xdc` puts a `PULLDOWN` on `pmod_cs_n`, so a line left floating by an unpowered K26 (or one still holding its outputs high-Z) reads low and can never set `kria_present`; a pull-down sinks, so it never sources current into the other board.
- `PMOD_SPARE2` (`fpga/artix/top.v`): debug UART TX (`115,200 baud`) is open-drain (`dbg_uart_tx ? 1'bz : 1'b0`), relying on the Kria's `PULLUP TRUE` on `pmod_spare2` (`fpga/kria/xck26_bd.xdc`) and the CH340X's internal pull-up (`tb_dbg_uart`, mutation `spare2_pushpull`). With `10–20 kOhm` pull-up and `~15–35 pF` bus capacitance, rise time (`~0.33–1.54 us`) stays well below the `8.68 us` bit time.
- K26 Pmod outputs (`fpga/kria/top.v`): `PMOD_CS`, `MOSI`, `SCLK`, `BEAM_STROBE`, `PPS_SYNC`, and `PMOD_SPARE1` stay high-Z until `adapter_alive` (`link_up_tx_sync[1]` OR a falling edge on `PMOD_SPARE2` within the last `3 s`, `PMOD_ALIVE_CYC = 375,000,000`), returning to high-Z when both lapse (`tb_system`, mutation `kria_pmod_always_oe`).
- `VU_LNA_ON` on `LFCN-1000+` (`fpga/artix/fe_ctrl.v`): whenever `OP_EXP` sets `VU_CONV_ON = 1` (`bit 6`), `V2V1 = 2'b11` (`bits 1:0`), and `V1V2V3 = 3'b011` (`bits 4:2`), `fe_ctrl` forces `VU_LNA_ON = 1` (`bit 5`) regardless of software request and reports it in `FE_STAT[27]` (`tb_fe_ctrl`, mutation `no_lna_force`).

3. Kria KV260 Zynq UltraScale+ PL & Block Design (`XCK26-SFVC784-2LV-c`)

Sources: `fpga/kria/top.v`, `fpga/kria/kria_pl_link.v`, `fpga/kria/kria_pps.v`, `fpga/kria/link_axis.v`, `fpga/kria/bd.tcl`, `fpga/kria/xck26.xdc`.

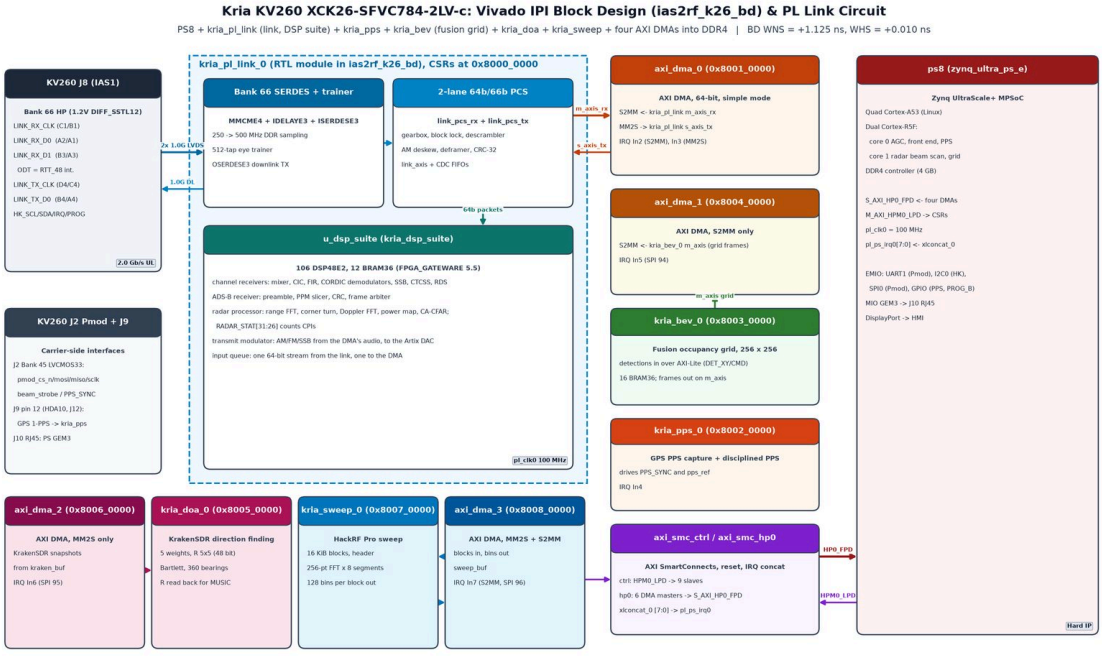
3.1 Kria K26 Silicon Die Floorplan & Occupancy



Kria K26 XCK26-SFVC784-2LV-c Silicon Die Floorplan

- **Vector / 4K Downloads:** `fpga/kria_k26_silicon_floorplan_4k.png`, `.svg` and `.pdf` in the high-res archive

3.2 Vivado IPI Block Design (`ias2rf_k26_bd`) & PL Link Circuit



Kria K26 Vivado IPI Block Design Circuit Schematic

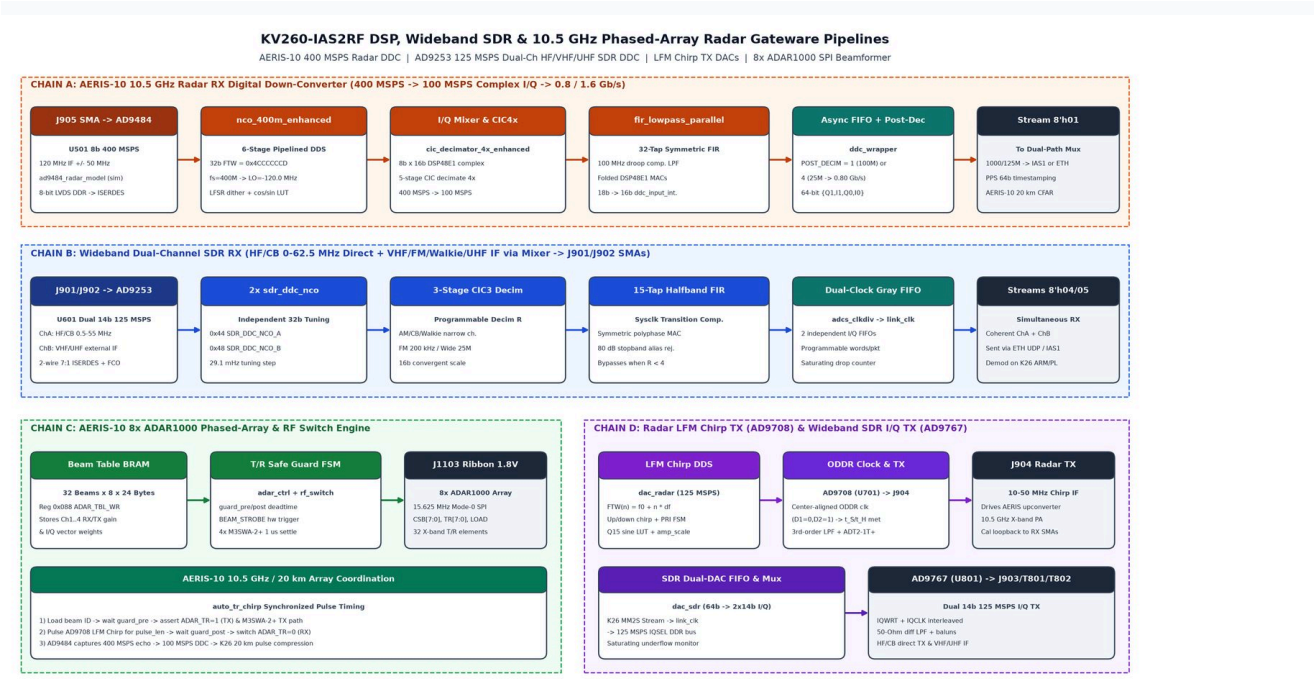
- **Vector / 4K Downloads (combined PS + PL `ias2rf_k26_bd` & `kria_pl_link` schematic):** `fpga/kria_k26_vivado_bd_schematic_4k.png`, `.svg` and `.pdf` in the high-res archive

3.3 K26 Block Design & Post-Route Resources (`fpga/kria/reports/`)

Instance / Subsystem	Module	Slice LUTs	FFs	BRAM36	BRAM18	URAM	DSP48E2	Purpose
ias2rf_k26_bd_wrapper (Full BD)	**ias2rf_k26_bd**	**53,336 (45.5%)**	**46,896 (20.0%)**	**40**	**8 (44.0 eq, 30.6%)**	**1 (1.6%)**	**229 (18.3%)**	Full PS8 + four DMAs + SmartConnect + PL link + DSP suite + PS framer + GPS PPS + fusion grid + KrakenSDR and HackRF blocks + EMIO UART1 + EMIO CAN1
kria_pl_link_0 (link only)	kria_pl_link	6,755	12,516	0	0	0	0	Bank 66 HP SERDES + 512-tap eye trainer + 64b/66b PCS + link_axis + TX_KEY
u_dsp_suite (in kria_pl_link)	kria_dsp_suite	23,188	16,009	16	0	0	106	Input queue (361 LUT, 1 BRAM36), channel receiver (6,697 LUT, 80 DSP), ADS-B (4,497 LUT), radar (10,674 LUT, 11 BRAM36, 14 DSP), transmit modulator (497 LUT, 12 DSP), u_dsp_out (458 LUT, 732 FF, 4 BRAM36)
kria_ps_framer_0	kria_ps_framer	431	598	0	0	1	0	Packet framer into axi_dma_0 with a 4,096-word URAM FIFO (104 LUTRAM)
kria_pps_0	kria_pps	568	744	0	0	0	0	GPS PPS capture, disciplined PPS generator, PPS_SYNC source (section 5.6)
kria_bev_0	kria_bev_axi	782	623	16	0	0	0	Fusion occupancy grid behind its AXI-Lite wrapper at 0x8003_0000 (INTEGRATIONS.md §6.1)
axi_dma_1	Xilinx IP	1,044	1,590	1	1	0	0	S2MM DMA at 0x8004_0000: the grid's frames into DDR4, IRQ In5 (SPI 94)
kria_doa_0	kria_doa_axi	10,117	2,089	0	1	0	115	KrakenSDR direction finding at 0x8005_0000 (section 5.8): weights, covariance, Bartlett scan. 3,200 of the LUTs are LUTRAM: Vivado keeps the ten steering-table memories (512 x 32 each) in distributed RAM
axi_dma_2	Xilinx IP	563	841	1	1	0	0	MM2S DMA at 0x8006_0000: the KrakenSDR's snapshots, IRQ In6 (SPI 95)
kria_sweep_0	kria_sweep_axi	1,586	638	2	1	0	8	HackRF Pro sweep FFT at 0x8007_0000 (section 5.9): block tail and FFT memory in block RAM (480 LUTRAM)
axi_dma_3	Xilinx IP	1,667	2,415	2	2	0	0	MM2S + S2MM DMA at 0x8008_0000: sweep blocks in, bins out, IRQ In7 (SPI 96)
axi_dma_0 + axi_smc_* + rst + xlslice + can1_tx_inv	Xilinx IP	6,635	8,833	2	2	0	0	64-bit MM2S/S2MM DMA (axi_dma_0: 2,199 LUT, 2,853 FF) into PS8 HP0_FPD DDR4, interconnect for all DMAs (axi_smc_ctrl + axi_smc_hp0), reset sync, UART slices and CAN1 TX inverter (before cross-hierarchy LUT combining across the 53,294 total)
Free K26 PL Silicon	-	**63,784 (54.5%)**	**187,344 (80.0%)**	**100.0 eq (69.4%)**	-	**63 (98.4%)**	**1,019 (81.7%)**	Available for on-SOM pulse compression, tracking and more channels

- **Timing (fpga/kria/reports/timing_summary.rpt & cdc.rpt):** Full BD WNS = +1.043 ns, TNS = 0.000 ns (0 / 188,554 failing setup endpoints; the worst path is an ADS-B divider stage, u_adsb_rx/g_ph[2].u_ph/u_div, on clk_pl_0). Intra-clock setup / hold: clk_pl_0 (100 MHz, 152,657 endpoints) +1.043 ns / +0.010 ns, rx_clkdiv (125 MHz, 34,540 endpoints) +2.664 ns / +0.014 ns, tx_clk_div (125 MHz, 1,186 endpoints) +1.960 ns / +0.016 ns, clk_300_u (300 MHz, 2 endpoints) +2.748 ns / +0.144 ns. Overall WHS = +0.010 ns, THS = 0.000 ns (0 / 188,554 failing hold; worst path is a delay-line register in the channel receiver, u_ch_rx/ssb_q_dly_reg, on clk_pl_0), WPWS = +0.000 ns, TPWS = 0.000 ns (0 / 54,270 failing pulse-width endpoints). drc.rpt reports 0 errors (252 warnings: 87 DPIP-2, 57 DPOP-3, 95 DPOP-4 DSP pipelining advisories, 1 PLCK-58 clock placer advisory, and 6 REQP-1934 + 6 REQP-1935 DMA FIFO block-RAM collision advisories). methodology.rpt reports the same 6 existing checks (LUTAR-1: 1, TIMING-9: 1, TIMING-18: 2, CLKC-30: 1, CLKC-56: 1) and 0 new warnings. cdc.rpt reports 253 CDC-1, 8 CDC-3, 6 CDC-6, 1 CDC-10, 439 CDC-13, 1 CDC-14 and 300 CDC-15 (1,008 entries; the new CDC-3 is the PMOD_SPARE2 synchroniser spare2_sync, and the CDC-14 entry is three bits of the link's receive FIFO read, u_fifo_rx2pl/mem_reg[9][12:10], that the 18 November report listed as three CDC-13: the same crossings, grouped; 0 new CDC paths from can1_txn / can1_rx). Build of 19 November with the Rev08 audit changes (FPGA_IRQ gated by link-up, PMOD_MISO gated by kria_present, the PMOD_SPARE2 input); the 18 November build (53,294 LUT, WNS = +0.991 ns) added u_dsp_out, kria_ps_framer, TX_KEY (0x38) and PS CAN1 EMIO. Earlier snapshots: 51,870 LUT (WNS = +1.125 ns) before kria_ps_framer and TX_KEY; 36,393 LUT (WNS = +0.874 ns) before the KrakenSDR and HackRF Pro blocks; 33,876 LUT (WNS = +1.121 ns) before the grid and its DMA; without the pipelining described in section 5.5 the DSP build missed clk_pl_0 by 13.8 ns.
- **UltraScale+ Bank 66 Training, PS UART1 EMIO & PS CAN1 EMIO:** Uses component-mode IDELAYE3 (VAR_LOAD, 512 taps @ ~4 ps, BISC EN_VTC handshaking) + ISERDESE3 at 125 MHz CLKDIV / 500 MHz CLK (MMCME4_ADV from 250 MHz forwarded LINK_RX_CLK) and ODT = RTT_48 internal DIFF_SSTL12 termination at 1.2 V. bd.tcl enables PS UART1 on EMIO so Linux exposes /dev/ttyPS1 @ 115,200 baud directly across KV260 Pmod J2 (D11 -> pmod_spare1, B11 <- pmod_spare2 with PULLUP TRUE), and PS CAN1 on EMIO across KV260 J9 (G6 -> can1_txn on pin 6, D6 <- can1_rx on pin 8, section 5.11).

4. Wideband SDR & AERIS-10 10.5 GHz Radar DSP Pipelines



DSP Wideband SDR & 10.5 GHz Radar Pipelines

- **Vector / 4K Downloads:** `fpga/dsp_radar_sdr_pipeline_schematic_4k.png`, `.svg` and `.pdf` in the high-res archive

4.1 Wideband SDR Architecture (`AD9253` + `AD9767` + `sdr_ddc.v`)

The adapter supports dual-channel receive and transmit SDR operation through the dual `14`-bit `AD9253` ADC (`U601`, clocked at **`62.5 MSPS`** in `500 MHz` master mode or **`50.0 MSPS`** in `400 MHz` master mode via one-lane `16`-bit DDR wordwise LVDS, `0x21=0x40`, `0x0B=0x07`) and dual `14`-bit `AD9767` TX DAC (`U801`, `125 MSPS @ 500M` / `100 MSPS @ 400M`):

1. **Direct-Sampled HF Receive (`0–31.25 MHz` @ `62.5 MSPS` or `0–25.0 MHz` @ `50.0 MSPS` Nyquist Zone 1):**
2. **Filtered HF Input (`J951` `SDR_RX_C` / `IF_RX_C`, Ch B direct):** Feeds `AD9253` Ch B directly (no RF switch) through the Rev07 `30 MHz` 7th-order elliptic anti-alias low-pass filter (`>= 60 dB` stopband from `50 MHz`), covering **AM broadcast (`0.53–1.7 MHz`), SW/HF amateur bands (`160m–10m`), and Citizen Band (`27 MHz CB`)** cleanly without aliasing (note at `50.0 MSPS` (`400 MHz` master), `25–30 MHz` folds onto `20–25 MHz`).
3. **Unfiltered Channel A (`J911` `SDR_RX_A` -> `SW1` RF1 -> `IF_RX_A`, Ch A):** Unfiltered path into `AD9253` Ch A (`SW1` RF2 connects `J912` `AERIS_IF_A`); **6m (`50 MHz`)** lies in **Nyquist Zone 2** and can only be sampled on this unfiltered Ch A path (`J911`).
4. `sdr_ddc_ch` tunes any carrier via a `32`-bit NCO with LSB step **`f_S / 2^32 = 0.01455 Hz`** at `62.5 MSPS` (**`0.01164 Hz`** at `50.0 MSPS`; **an FTW computed assuming `125 MHz` tunes to half the intended frequency**), and decimates by `R = 2..65535` through a 3-stage `CIC3` + 15-tap symmetric halfband `FIR` (`80 dB` stopband alias rejection, automatically bypassed for `R < 4`).
5. **VHF/UHF receive: the Rev08 front end on `J961`, and external converters:**
6. Because `AD9253` Zone 1 ends at `31.25 MHz` (`25.0 MHz` at `400M`), **FM Broadcast (`88–108 MHz`), Airband AM (`118–137 MHz`), Walkie-Talkie / PMR446 (`446 MHz`), 70 cm (`433 MHz`) and ADS-B (`1090 MHz`)** do not reach this ADC. They come from the Rev08 front end on `J961` (direct `30–170 MHz` and RFFC5072 converter `300 MHz` to `3 GHz` behind the `300 MHz` high-pass; `170–300 MHz` is not covered), which `SW2` RF2 connects to the `AD9484` (§4.3, **RX_VU_SPEC**). As built, `C927` is fitted and `C926` is not, so `J922` `SDR_RX_WB` is unconnected; swapping the two 0402s restores the bare `J922` (Zone 1 `0–200 MHz` at 8 bits, NF about 27 dB). An external converter into `J911`/`J951` remains possible.
7. Independent `NCO_B` (`0x48`) tunes Ch B simultaneously with Ch A, emitting dual coherent 64-bit I/Q packet streams (`8'h04` Ch A, `8'h05` Ch B) over `IAS1` / `1000BASE-T` to K26 `ps8` for FM/AM/SSB/NFM demodulation and spectrum waterfalling.
8. **Interleaved Dual-Channel SDR TX (`AD9767` via `J931` `SDR_TX_A` / `J932` `AERIS_TX_A` / `J952` `SDR_TX_C`):**
9. Downlink packets (`8'h12` or long `8'h10`) carry complex baseband IQ samples from K26 DDR4 to `dac_sdr.v`, driving `dacs_d[13:0]` interleaved (`IQWRT`/`IQSEL`) on the non-MMCM `÷4` `dac_clk` (`125 MSPS` at `500 MHz` mode, `100 MSPS` at `400 MHz` mode) into `ADT2-1T+` transformers (`T801`/`T802`) and low-pass filters (`DAC1` via `SW3` `J931`/`J932`, `DAC2` direct to `J952`).
10. **Switch-free HF defaults:** On power-on reset, `ADCS_CTRL` initializes to `0x0000_0009` (`Ch B / IF_RX_C J951` enabled) and `DACS_CTRL[1] = 0` enables `hf_dac2_mode = 1` so primary `I` routes directly to `DAC2 / IF_TX_C J952` (with optional

DACS_CTRL[2] dac1_mute clamping DAC1 to midscale 14'h2000). Set DACS_CTRL[1] = 1 (hf_dac2_mode = 0) for standard DAC1/DAC2 quadrature I/Q TX.

4.2 AERIS-10 10.5 GHz / 20 km Phased-Array Radar Chain

All X-band front-end modules are sized and pin-mapped to drive the external AERIS-10 antenna array (8x ADAR1000 = 32 T/R elements for 20 km instrumented range in Extended configuration), enabled when the master clock is **400 MHz** (held in hardware reset at 500 MHz per Rev08 A-1 until G-7 adds a dedicated 500 MSPS path):

- **TX Pulse Synthesis (dac_radar.v):** Generates 32-bit Linear Frequency Modulated (LFM) up/down chirps centered in the 120 MHz IF window via AD9708 (J941 AERIS_TX / J942 SDR_TX_WB -> external AERIS-10 upconverter & 10.5 GHz PA). When ADAR_CTRL[12] (auto_tr_chirp) is set, adar_ctrl.v sequences guard_pre deadtime -> T/R switch TX -> chirp transmission -> guard_post ring-down -> RX echo window.
- **Beamforming Control (adar_ctrl.v & rf_switch.v):** Stores 32 beam tables × 8 chips × 24 bytes in Artix BRAM (0x88) and blasts phase/gain weights over 15.625 MHz 4-wire SPI across J1103 (1.8 V IDC ribbon) with synchronous LOAD and hardware beam_strobe pulses while guarding the four M3SWA2-34DR+ SPDT switches (J911/J912, J921/J922, J931/J932, J941/J942).
- **RX 400 MSPS Capture & DDC (adc_capture.v + ddc_wrapper.v):** Captures 8-bit 400 MSPS LVDS samples from AD9484 (J921 AERIS_IF, or through SW2 RF2 the J961 VHF/UHF front end), digitally down-converts the 120 MHz IF to 100 MSPS complex I/Q using PLFM_RADAR (62d4c55, MIT) DSP48E1 slices (79 DSPs), decimates by 4 through the ddc_hb4 anti-alias half-bands (0.80 Gb/s sustained), and streams stamped 512-byte 8'h01 packets to the Kria. The NCO defaults to PHASE_INC_120MHZ = 32'h4CCCCCCD (0.3 * f_S) in **fpga/third_party/aeris/ddc_400m.v**; since G-4, RADAR_CTRL[2] and [31:8] override it. Two NCO fixes (17 Nov) set the image of the input around the LO: the quarter-wave table is sampled half a step off zero (sin(2 pi (k + 0.5) / 256)), because its fold reads cos as LUT[63 - k], which with the upstream table put cos one step (1/256 cycle) away from sin; and a random byte from a 23-bit LFSR (eight steps per clock) is added to the accumulator just below its 8 address bits. Upstream added its dither to the FTW's low byte, where it never reached the address. At 0.3 f_S the accumulator visits 10 phases, so the plain truncation error repeats every 5 samples and has a component at the conjugate LO. Before the fixes the image sat at -46 to -61 dB, depending on where the accumulator happened to be, which is why tb_system's S3 read 48 to 61 dB from one RTL change to the next. It is now -81 dB or lower in every window of tb_nco_image. The only side effect is a constant pi/256 on the LO phase. The path is held in reset in the 500 MHz mode (A-1).

4.3 D2: the 500 MSPS AD9484 path (Rev08 G-7)

At 500 MHz the AD9484 runs at 500 MSPS and its DCO at 250 MHz. The AERIS DDC stays as it is and keeps running only at 400 MSPS (A-1). D2 is a second path, selected by D2_CTRL[0], that runs whenever the master clock has settled at 500 MHz. HF on the AD9253 (62.5 MSPS) and VHF/UHF on the AD9484 then run at the same time. D2 takes 4,124 LUT, 6,241 FF, 4 RAMB18 and 8 DSP48 (119 of 120 used), plus 259 LUT for its AGC peak detector; the Artix goes from 20,254 to 25,000 LUT (77 %).

Capture (adc_capture, mode_500)

- The DCO MMCM stays in reset, because its 400 MHz output would run at 500 MHz.
- The IDDRs keep their BUFIO, and the BUFR capture registers keep their BUFR, now at 250 MHz.
- The IDELAYs and the eye-scan trainer move to refclk_200m. They are fed through the BUFGCTRL that otherwise carries the MMCM's clk_200m. The select changes only while the capture is in reset, so both inputs are set to IGNORE.
- The trainer is unchanged. Because the training pattern is static, it samples the IDDR pairs through two flip-flops instead of the 400 MSPS FIFO.
- Each pair of DCO cycles makes one word of four samples, 4 x {OR, D[7:0]} with the earliest sample in [8:0]. The words cross into link_clk through an 8-word Gray FIFO.
- link_clk is 500 MHz / 4. It is frequency-locked to the DCO because both come from the master clock. Once the reader starts at a fill of 4, the fill stays put. A drift trips D2_STAT[3] and the reader restarts at a fill of 4.
- In top.v, a change of mode holds the capture in reset for 16 refclk_200m cycles. mode_500 changes in the middle of that window.
- Training starts about 65 us after D2 does (ADC_AUTO_TRAIN). It can be restarted with D2_CTRL[2] or the Pmod retrain.

DDC (ddc_500.v, link_clk, four lanes per clock)

Stage	What it does	Result
NCO	32-bit phase. Lane `i` runs at `acc + i * FTW`, and `acc` advances by `4 * FTW`. A 12-bit phase addresses a 1024 x 12-bit quarter-wave table (`ddc500_rom.v`, generated by `gen_ddc500_rom.py`): one dual-port RAMB18 per lane, one port for the sine's index and one for the cosine's	Worst phase-truncation spur -72 dBc
Mixer	The code as an odd 9-bit number, `2 * (code - 128) + 1`, so mid-scale carries no DC, times `e^-j theta`, in one DSP48 per product, rounded to 15 bits. `D2_CTRL[1]` conjugates the output; the AERIS DDC's output is the conjugate spectrum	
CIC	5 stages, decimation by 5, 500 to 100 MSPS. Integrators in four-lane prefix form, with one adder in each accumulator loop, pruned (Hogenauer) from 28 bits to 27, 25, 23, 22 and 21 bits, and the combs to 21, 20, 19, 18 and 18. The truncations are plain shifts: a constant error entering after the first integrator leaves no DC, and the one before it is the mixer's rounding. Of every five words it keeps lanes 0, 1, 2, 3 and none (samples 0, 5, 10, 15 of 20). Gain 3125 / 4096	What folds onto +/-10 MHz (100 MHz multiples +/- 10 MHz) at least 94 dB down, onto +/-12.5 MHz at least 83 dB; droop 0.69 dB at 10 MHz
`ddc_hb4`	The radar path's two half-bands, unchanged, 100 to 25 MSPS. Their input is valid 4 cycles in 5	Flat to 0.07 dB up to 10 MHz; -49.6 dB from 15 to 25 MHz
Packets	512-byte packets on stream `0x01`, as from `ddc_wrapper`, so the Kria sees the same stream in both clock modes. There is no CPI mark, because the X-band front end is off at 500 MHz. While D2 runs, `top.v` routes stream `0x01` from D2, and switches back only after D2's last packet has gone (`pkt_busy`), so the uplink arbiter never waits on a stopped source	
Gain	A real tone of `A` codes at `f_NCO + d` gives `	bb
AGC	The four lanes' largest-magnitude code goes to a second `adc_peak` (2^14 words, 131 us), which feeds `fe_agc` in place of the 400 MSPS peak. Over-range is a code of 0 or 255: the OR pin's IDDR is not timed at 250 MHz	

Constraints (`xc7a50t.xdc`)

- `clk_adcr_dco_500` (4.000 ns, `-add`) is stopped at the DCO MMCM's `CLKIN1`. It is physically exclusive with `clk_adcr_dco` and with the 400 MHz clocks.
- Its crossings into `link_clk` and `refclk_200m` take `set_max_delay -datapath_only 4.000`.
- The `BUFGCTRL` select is a false path, and so is the OR pin's IDDR at 250 MHz.
- The trainer's results reach `link_clk` under an 8 ns datapath limit, and the D2 run condition reaches `refclk_200m` under 4 ns.

Uplink (`top.v`, `ddc_wrapper.v`)

- The radar DDC and D2 never offer a stream `0x01` packet at the same time, so `valid` and `eop` are ORed and both see `ready`.
- In both DDCs, `pkt_valid` comes from registers: `pkt_active`, or a registered `a packet is ready`. With store and forward the FIFO cannot run empty during a packet, and the pointer arithmetic leaves the uplink arbiter's path to the SDR FIFOs.

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5. Complete Control, Stream & Register Map

5.1 Packet Stream IDs (64-bit Header Format in `fpga/link/LINK_PROTOCOL.md`)

`stream_id`	Direction	Generator / Consumer	Payload Content
`8'h01`	Artix -> Kria	`ddc_wrapper` (`u_ddc`)	AERIS-10 400->100 MSPS Radar DDC Complex `I/Q` `{Q1, I1, Q0, I0}` + 64-bit PPS timestamp
`8'h02`	Artix -> Kria/ ETH	`eth_sdr_pkt_gen` (`u_sdr_gen`)	Diagnostic / telemetry packet generator on SGMII UDP path
`8'h04`	Artix -> Kria	`sdr_ddc` Ch A (`u_ch_a`)	AD9253 Ch A (`J911`/`J912` unfiltered, `62.5`/`50.0 MSPS`) decimated `16`-bit `I/Q` stream
`8'h05`	Artix -> Kria	`sdr_ddc` Ch B (`u_ch_b`)	AD9253 Ch B (`IF_RX_C J951 30 MHz` LPF, `62.5`/`50.0 MSPS`, default on) decimated `16`-bit `I/Q` stream
`8'h10`	Kria -> Artix	`kria_pl_link` -> `artix_top`	Short CMD packet (`len = 8B`, `{opcode[63:56], flags, addr[47:32], wdata[31:0]}`) or legacy IQ TX (`len >= 24B`)
`8'h11`	Artix -> Kria	`artix_top` Readback Engine	Register read response `{16'h0002, addr[47:32], rdata[31:0]}`
`8'h12`	Kria -> Artix	`kria_pl_link` -> `dac_sdr`	AD9767 dual `14`-bit `I/Q` TX sample stream
`8'h20`	Kria PL -> PS	`kria_dsp_out` -> `kria_ps_framer`	Audio, 64 words a packet: `{flags, mono, right, left}`, flags pilot, CTCSS, RDS bit present, RDS bit (§5.10)

stream_id	Direction	Generator / Consumer	Payload Content
8'h21	Kria PL -> PS	kria_dsp_out -> kria_ps_framer	ADS-B, one CRC-good frame a packet, 2 words
8'h22	Kria PL -> PS	kria_dsp_out -> kria_ps_framer	Radar detections of one CPI (at most 64) and a summary word {0xFF, cpi, detections, dropped}
8'h23	Kria PL -> PS	kria_dsp_out -> kria_ps_framer	Radar range-Doppler map, 512 words, two cells a word {det, dbin, rbin, exponent, mantissa}
8'h00	Kria PL -> PS	kria_ps_framer	Flush packet (0 words): ends a DMA block after 1 ms without data

5.2 Artix-7 Full CSR Space (0x00..0xFC and, since Rev08, 0x100..0x124 via IAS1 CMD 8'h10, UDP Port 0x4952 or Debug UART; the Pmod SPI port reaches 0x00..0x7F only)

Offset	Register	Access	Fields & Function
0x00–0x30	IAS1 Link Control & Telemetry	R/W	Link reset, PRBS-7 TX/RX test, manual IDELAY tap control, block/deskew lock, SH/CRC/PRBS error counters, eye window edges (LINK_PROTOCOL.md §7.1)
0x34	ADCS_CTRL	R/W	[0] AD9253 capture enable, [1] start_init (W1P), [3:2] SDR DDC Ch A/B enable (0x0000_0009 reset: Ch B / IF_RX_C J951 enabled for switch-free HF)
0x38	ADCS_STAT	R	[31:24] AD9253 Chip ID, [17:16] conv SPI init err/done, [11:0] aligned, idelay_done/err, bitslip_err, best_tap
0x3C–0x40	CONV_SPI_CMD / STAT	R/W	Raw 3-wire SPI access to AD9484 & AD9253 ([22] target, [21] rw, [20:8] addr, [7:0] wdata)
0x44–0x50	SDR_DDC_NCO_A/B, DECIM, STAT	R/W	Independent 32-bit NCO FTWs for Ch A (0x44) & Ch B (0x48), [15:0] CIC3 decim ratio & [25:16] words/pkt (0x4C), dropped sample counter (0x50)
0x54–0x6C	DACR_* (Radar LFM Chirp TX)	R/W	Enable/trigger & amp_scale (0x54), start FTW f0 (0x58), chirp slope df (0x5C), pulse_len (0x60), pri_len (0x64), chirp_active (0x68), pulse_cnt (0x6C)
0x70–0x78	DACS_* (SDR IQ DAC TX)	R/W	tx_enable ([0]), ~hf_dac2_mode ([1], default 0 = primary I on DAC2 / IF_TX_C J952), dac1_mute ([2]) (0x70); underflow counter (0x74); async TX FIFO level (0x78)
0x7C–0x90	ADAR_* & RF Switches	R/W	active_beam_id[4:0], soft T/R, sw_req[11:8], auto_tr_chirp[12], soft_load, scan mode [13] with its last beam [20:16] (each BEAM_STROBE loads the next of beams 0..scan_last, from 0; Rev08) (0x7C); guard_pre/post (0x80); sw_settle (0x84); 32-beam RAM write (0x88); raw ADAR SPI (0x8C); status (0x90)
0x94–0xA4	HK_I2C_* & HK_TEMP_ERR	R/W	Open-drain I2C controller for TMP1075 (0x48) & CAT24C02 (0x50) temperature & EEPROM polling
0xA8–0xB4	XO_CTRL, XO_DELTA_M, XO_RAW	R/W	Si549 fractional N-delta (±50 ppm ENABLE_ETH clamp, 0xAC), raw I2C (0xB0/0xB4; 0xB0[23:17] device address, 0 = the Si549, Rev08), CLK_SEL + safe-boot/400<->500 MHz DRP switch (xo_boot_err[12], xo_delta_clamped[13], xo_boot_done[14])
0xB8–0xBC	XADC_TEMP_VCCINT / VCCAUX	R	On-die Artix-7 XADC 12-bit temperature, VCCINT, VCCAUX, and overtemp flag
0xC0–0xE0	PPS_* & TS_SYS / PPS_LATCH	R/W	1-PPS loop gain/nom period/ppm frequency error & locked 64-bit nanosecond wall-clock timestamp registers
0xE4	RADAR_CTRL	R/W	[0] rad_ddc_en (reset 1, replaces legacy ~pmod_spare1), [1] W1P clear sticky clip/ovf flags & 0xEC counters, [2] radar NCO override, [3] CPI mark in I[0] of the stream (G-8), [7:4] the mark's delay in 25 MSPS samples, [31:8] the NCO's frequency word (Rev08 G-4)
0xE8	RADAR_STATUS	RO	[0] radar_dis_by_clk_mode (1 at 500 MHz), [1] adcr_mmcm_locked, [2] adc_trained, [3] dco_phase_err, [4] dl_link_up, [5] dl_up & adc_trained (replaces legacy pmod_spare2), [6..9] sticky adcr_or/adcs_clip/ddc_sat/ddc_ovf, [10] reg_rad_ddc_en, [21:16] adc_eye_width_min, [23:22] ddc_status
0xEC	CLIP_OVF_CNT	RO	[15:0] saturating adcr_clip_cnt (AD9484), [31:16] saturating adcs_clip_cnt (AD9253)
0xF0	DBG_UART_CTRL	R/W	[15:0] baud_div (default 1085 = 115,207.4 baud on 125 MHz link_clk), [16] stat_periodic_dis, [17] W1P force_stat_p, [24] rx_idle_high, [25] tx_busy, [26] banner_done, [31:27] rx_ferr_cnt
0xF4	DBG_UART_STAT_DIV	R/W	[31:0] periodic STAT interval in link_clk cycles (default 125,000,000 = 1.000 s)
0xF8–0xFC	BUILD_GIT_HASH / BUILD_TIMESTAMP	RO	Injected synth_design -generic 8-hex git commit prefix (0xF8) and {BUILD_DATE[15:0], BUILD_TIME[23:8]} (0xFC)
0x100	D2_CTRL	R/W	Rev08 G-7 500 MSPS path. [0] enable: D2 runs while the master clock is settled at 500 MHz. [1] conjugate the output. [2] restart AD9484 training (write 1; reads 0). [3] clear D2_STAT[3] (write 1; reads 0). Put the AD9484 in its 0xAA/0x55 test pattern before training, as at 400 MSPS

Offset	Register	Access	Fields & Function
0x104	D2_FTW	R/W	D2's NCO: f = FTW * 500 MHz / 2^32
0x108	D2_STAT	R	[0] running, [1] trained, [2] training failed (eye under 4 taps or wrong pattern), [3] FIFO slip (sticky), [4] master clock at 500 MHz, [13:8] narrowest eye in IDELAY taps
0x10C	D2_DROP	R	[23:0] stream 0x01 words dropped at the packet FIFO (D2's while it runs, else the radar DDC's)
0x110	FE_CMD	R/W	Rev08 front-end command (fe_ctrl.v), [31:28] op: 1 INIT, 2 EXP_OUT [15:0] = {port 1, port 0} of U1313 (software owns port 0, RESETX and ENBL; written on change), 3 POLL inputs, 4 RFFC5072 write [22:16] register [15:0] data, 5 RFFC5072 read, 6 PE4312 [5:0] in 0.5 dB steps, 7 LEDs [7:0] (written on change). Wait for FE_STAT[28] = 0 before the next write
0x114	FE_STAT	RO	[31] I2C error, [30] expanders initialised, [29] overrun (a command written while busy, dropped), [28] busy, [27] LNA forced on (VU_CONV_ON=1, V2V1=11, V1V2V3=011), [23:16] I2C transactions of the last command, [15:0] U1313 inputs at the last POLL ([12] = VU_LD lock detect, [8] = VU_BIAS_FLT_N)
0x118	FE_RFFC	RO	[15:0] the last RFFC5072 register read
0x11C	FE_LED_CTRL	R/W	[0] LED auto-map on (reset 1), [1] show [15:8] instead, [31:24] RO what was last written to U1501
0x120	FE_AGC_CTRL	R/W	Rev08 G-5 AGC (fe_agc.v), off at reset: [0] enable, [1] LNA bypass allowed, [14:8] high threshold (default 96 of 128), [22:16] low threshold (default 24), [31:24] hold-off in ms (default 50)
0x124	FE_AGC_STAT	RO	[31] LNA in, [29:24] attenuation code, [22:16] last peak of the AD9484 codes, [15:0] changes made
others from 0x100	(reserved)	n/a	Any address from 0x100 not listed reads 0 and ignores writes; page 0 no longer aliases into 0x1xx
UDP 0x0000 / 0x0004	ETH_MUX_CTRL / ETH_MDIO	R/W	Dual-path policy ([1:0]), SDR UDP gen enable ([2]), fault injection ([4:3]), AN restart ([5]), Clause 22 MDIO access to RTL8211FSI

5.2a Front-end control (Rev08 G-2 to G-6)

The two TCA6416A expanders (U1313 at 0x20 on RX_VU, U1501 at 0x21 on STATUS) share the XO_SCL/XO_SDA bus with the Si549. hk_xo_ctrl (cfgmclk) gained a device address on its raw port and a second client port, and fe_ctrl drives the expanders through it; the Si549 presets, its delta-M and raw accesses keep priority. The expanders' INT pins are not connected, so inputs are read on request (POLL). Nothing goes on the bus unless a command asks.

- **INIT** runs before the first command and after any I2C error: output registers first, then configuration, so no pin glitches when it turns into an output. It drives VU_ATT_LE low, which latches the PE4312 at its power-up 31.5 dB. LE must stay low whenever SCLK moves: with LE high the attenuator's latch is transparent, and SCLK/SDATA are shared with the RFFC5072.
- **RFFC5072** register write and read-back with HackRF's three-wire framing (**RFFC5072_PROGRAMMING.md** §2): every SCLK or SDATA edge is one write of U1313's port 1, so a register write is 59 I2C transactions (about 26 ms at the nominal 65 kHz bus, 17 to 52 ms over CFGMCLK's ±50 % spread) and a read 82 (about 37 ms). A gateware three-wire master would be the upgrade for fast hopping.
- **PE4312**: six bits MSB first (C16 first), then an LE pulse; about 5 ms.
- **LEDs (G-6)**: D1501..D1508 = CFG (boot done), CLK (500 MHz), LINK (link up and ADC trained), ADC-R over-range, ADC-S clip (both sticky until 0xE4[1]), LO lock (from the last POLL), TX (SDR DAC or radar chirp), ERR (I2C or ADC phase error). Written on change, at most once every 100 ms; FE_LED_CTRL[0] = 0 stops them and the bus stays quiet.
- **AGC (G-5)**: adc_peak takes the largest |code − 128| of the AD9484 per 65,536-sample window (over-range counts as full scale); fe_agc adds 3 dB above the high threshold, removes 0.5 dB after each quiet hold-off period, bypasses the LNA only at 31.5 dB, and puts it back 18 dB under the low threshold. Command priority: software, then AGC, then LEDs. With the AGC on, software must not send ATT. The AD9484 path runs in the 400 MHz mode only (A-1), so the AGC does too.
- **G-4** (tunable DDC): the AERIS NCO is a register through RADAR_CTRL[2] and [31:8], default unchanged; the second decimation stage down to channel bandwidths is in the Kria PL (kria_channel_rx, section 4), where DSP slices are plentiful, instead of in the Artix (one DSP48 left free since G-7).

Bus errors: a NACK on fe_ctrl's transactions sets FE_STAT[31] (and so the ERR LED) and makes the next command start with INIT. It does not set XO_CTRL[11] xo_ack_err or count in XO_CTRL[31:16], which stay for the Si549 and raw accesses, so a missing or unpowered RX_VU board never marks the clock XO as faulty.

Benches: tb_fe_ctrl (models of the TCA6416A, the RFFC5072 port and the PE4312, plus a second hk_xo_ctrl and fe_ctrl on a bus with no devices; 28 checks; mutations le_high, no_shadow, lsb_first, gen_nack_to_xo), tb_fe_agc (closed loop with a

tone; mutation `no_holdoff`), and `tb_artix_top` (CSR page 1, no aliasing).

5.3 Kria `kria_pl_link` AXI4-Lite Slave (`s_axi` at `0x8000_0000`)

Offset	Register	Function
`0x00`	`CTRL`	Soft reset, loopback enable, retrain trigger, manual IDELAY override, PRBS-7 TX/RX check
`0x04`	`STATUS`	`l0_lock`, `l1_lock`, `deskew_lock`, `link_up`, `idelayctrl_rdy`, `train_state`, `st_remote_status`
`0x08` / `0x0C`	`TAP_L0` / `TAP_L1`	Active & manual `512`-tap `IDELAYE3` tap values (`~4 ps/tap`) for `LINK_RX_D0/D1`
`0x10`–`0x28`	Error & Packet Telemetry	`sh_err_l0`, `sh_err_l1`, `crc_err_cnt`, `pkt_rx_cnt`, `{rx_drop, tx_drop}`, `{am_seq, skew_blocks}`, `prbs_err_cnt`
`0x2C` / `0x30`	`EYE_L0` / `EYE_L1`	Measured opening left/right tap boundaries from `link_rx_train_fsm` eye scan
`0x38`	`TX_KEY`	Transmit enable owned by R5F core 0 (`pl_clk_100m`): writes take effect only with full byte strobes (`wstrb == 4'hF`) and `24'h4B4559` (`"KEY"`) in `[31:8]`; `[0]` sets `tx_key` (`0x4B45_5901` on, `0x4B45_5900` off, reset `0`). Reads return `{24'h4B4559, 7'd0, tx_key}`. Clocked on `pl_clk_100m`, so core 0 can always read or clear it even when the IAS1 receive clock is absent

5.4 Debug UART Console (`dbg_uart` / Kria PS `UART1` EMIO, Rev08 G-1)

- **Physical & Clocking:** Runs on `link_clk` (`125.000 MHz` constant in both `400 MHz` and `500 MHz` master modes via MMCM DRP), with `DBG_UART_CTRL[15:0] = 1085` -> `115,207.4` baud 8N1 (`+0.0064%` error). Artix RX is `pmod_spare1` (`G15`, `PULLUP TRUE`); Artix TX is `pmod_spare2` (`G11`). On Kria (`bd.tcl/kria_pl_link.v/top.v`), PS `UART1` connects over EMIO (`D11` -> `pmod_spare1`, `B11` <- `pmod_spare2`, exposing `/dev/ttyPS1`).
- **Boot Banner & 1 Hz `STAT`:** Prints `KV260-IAS2RF build=<YYYYMMDD>-<HHMMSS> git=<8h> clk=<500M|400M> eth=<yes|no>` after reset, followed every `1.0 s` (`DBG_UART_STAT_DIV`, disable with `DBG_UART_CTRL[16]`) by `STAT xo=<0|1> clk=<500|400> mmcm=<sys><eth><adcr> dl=<st><l0><up> eth=<up><cu> adc=<tr_r><al_s> clip=<adcr4h><adcs4h> xadc=<3h> tmp=<4h> err=<2h> rdis=<0|1>`.
- **CLI & 4-Master CSR Arbitration:** Supports `r <addr>` -> `<8h>`, `w <addr> <val>` -> `ok`, `s` -> immediate `STAT`, `h` -> help (hex, case-insensitive, optional `0x`, backspace, echo, invalid/overflow -> `err`). Artix CSR writes/reads arbitrate atomically across all four masters (`dl_pend > eth_pend > spi_pend > uart_csr`) with single-slot registered pending latches for link/ETH/SPI and held `uart_csr_req` until `uart_csr_ack_r` so no concurrent write is lost or torn on collision.

5.5 Kria PL DSP suite (`kria_dsp_suite`, AXI-Lite `0x40..0x7C` of `kria_pl_link`, Rev08 G-8)

The suite sits in `kria_pl_link` on `pl_clk_100m` and takes the stream selected by `DSP_CTRL[3:2]` (`8'h01` AD9484 radar/VHF DDC, `8'h05` and `8'h04` the two AD9253 channels). Everything is off at reset (`DSP_CTRL[0] = 0`, `TX_KEY[0] = 0`).

Offset	Register	Fields
`0x40`	`DSP_CTRL`	`[0]` receive enable, `[1]` transmit enable (read-only mirror of `TX_KEY[0]` at `0x38`; writes to bit 1 are ignored so whole-register writes from Linux cannot key or clear the transmitter), `[3:2]` source stream, `[6:4]` channel mode (`0` AM, `1` USB, `2` LSB, `3` NBFM, `4` WBFM), `[7]` ADS-B, `[8]` radar, `[9]` radar window, `[12:10]` TX mode (`0` CW, `1` AM, `2` NBFM, `3` USB, `4` LSB), `[13]` `radar_sync`: CPIs start at the Artix's mark, `[14]` the result streams of `kria_dsp_out` on, `[18:15]` a radar map every `2^n` CPIs (§5.10)
`0x44`	`CH_NCO`	Channel NCO frequency word, `2^32 · f / f_stream`; `0` bypasses the mixer
`0x48`	`CH_DECIM`	`[15:0]` CIC decimation `R`, `[21:16]` CIC shift (gain `R^N`), `[22]` five CIC stages instead of three, `[31:24]` FIR decimation
`0x4C`	`CH_DEMOD`	`[15:0]` de-emphasis coefficient, `[31:16]` CTCSS Goertzel coefficient (Q14 `2 cos ω`)
`0x50`	`CH_PILOT`	19 kHz pilot frequency word at the channel rate
`0x54`	`CH_CTCSS`	`[15:0]` Goertzel block length, `[31:16]` RDS samples per bit, **Q8.8** (`250 kS/s`: `210.53` = `0xD287`)
`0x58`	`CH_CTCSS_THR`	CTCSS detection threshold (Goertzel power)
`0x5C`, `0x60`	status (RO)	Last audio pair; `{audio count [31:16], RDS bit count [15:8], result stream lost data [3] (sticky), input queue overflow [2] (sticky), CTCSS detect [1], pilot lock [0]}`
`0x64`	`ADSB_CFG`	`[7:0]` samples per 0.5 µs chip (`[7]` adds one on every other chip: `0x8C` = 12.5 at 25 MSPS), `[23:8]` floor on the four preamble pulses' summed chip averages
`0x68`, `0x6C`	ADS-B status (RO)	`{CRC errors, CRC good}` frame counters; low word of the last good frame

Offset	Register	Fields
`0x70`–`0x78`	`TX_CAR`, `TX_TONE`, `TX_CFG`	Carrier and test-tone frequency words; `[15:0]` modulation parameter, `[31:16]` amplitude
`0x7C`	`RADAR_ALPHA` (W) / `RADAR_STAT` (R)	Write: `[15:0]` CFAR factor, Q8 (`1536` = 6.0), `[31:16]` absolute power floor in units of 16 (`0` keeps the former fixed `20000`); read: `[31:26]` CPIs completed modulo 64 (Rev08, for R5F core 1's scan), `[25:10]` detections in the last CPI, `[9:6]` peak Doppler bin, `[5:0]` peak range bin

What G-8 changed, and why:

- **Input queue (`kria_dsp_suite`).** The suite taps the link's AXI-Stream, where a whole packet (up to 512 beats of two samples) arrives on consecutive clocks, and turns each 64-bit beat into two samples, one per clock. The old unpacker dropped any beat that arrived while the second sample of the previous one went out. The paced sweeps never showed it, but in the full chain it corrupted every radar CPI and every ADS-B frame. A 512-beat FIFO (one BRAM36) now sits in front of it; overflow is sticky in `0x60[2]`. Mutation `unpack_no_queue`.
- **RDS bit clock (`kria_channel_rx`).** The 57 kHz product is low-passed by two first-order sections and integrated over the four quarters of each bit. The bit clock is a Q8.8 accumulator against `CH_CTCSS[31:16]`, so a non-integer number of samples per bit (210.53 at 250 kS/s) does not slip. An early-late gate on the bi-phase mid-bit transition pulls it with a gear shift: 8 samples per bit for the first 16 bits, then 2, then half a sample, and from bit 112 a quarter sample. The loop starts anywhere in the bit (up to half a bit from lock), so a fixed one-sample pull could not converge in time, and a large step left jitter. Mutation `rds_no_timing` removes the loop.
- **Channel mixer NCO (`kria_channel_rx`).** The mixer's sine is the 512-point table linearly interpolated on the next 8 phase bits, as in `kria_tx_mod`. With the bare table (9 bits of phase), a small offset (the few hertz the Artix's 24-bit NCO leaves) made the table index step every few thousand samples. The resulting phase sawtooth put sidebands about 50 dB down on every strong signal in the stream, which cost 7 to 9 dB of SINAD next to a strong airband neighbour. The LO is registered one step ahead (`lo_c`, `lo_s`), so the interpolation's multiply is not in series with the mixer's. Mutation `mix_nco_9bit` restores the bare table.
- **Mixer rounding (`kria_channel_rx`).** The mixer's products were cut to 16 bits with a plain shift, a bias of -0.5 LSB on every input sample. The CIC's gain (`R^3 / 2^shift`, about 8 for NBFM) turned it into a DC offset as large as the channel's noise, and that offset, added to an FM carrier near 0 Hz, cost NBFM 6.5 dB of sensitivity whenever the channel NCO was on. The products are now rounded; the RTL's output then matches a bit-level model sample for sample. Mutation `mix_truncate`.
- **CIC with five stages (`kria_channel_rx`, `CH_DECIM[22]`).** A three-stage CIC barely attenuates the bands that fold next to each multiple of its output rate. An airband AM neighbour 25 kHz away, at a 24.04 kS/s CIC output, has sidebands within 3 kHz of the first null, where three stages give only -59 dB: a neighbour 35 dB up cost 5 dB of SINAD. Five stages give -98 dB there, for 0.4 dB more droop at the channel edge. The integrators are shared and 72 bits wide (`R^5 = 2^50` at `R = 1040`); the three-stage combs work modulo `2^48` on the third integrator, so the default is bit-identical to the former CIC. The shift for five stages is `5 log2 R` minus the wanted gain.
- **CORDIC guard bits (`kria_cordic`).** `FRAC = 8` fractional bits through the 1/K pre-scale and the shifts. Without them small vectors lost their low bits: a weak AM carrier lost 5 dB of SINAD against a floating-point demodulator, now 0.6 dB at most.
- **ADS-B (`kria_adsb_rx`).** The chip grid was free-running against the received frame, so half a chip off every chip average mixed two chips. Four decoders now run on grids a quarter chip apart, so one is always within an eighth of a chip. The first CRC-good copy is reported and the others (within 2 µs) are dropped. A frame no phase decodes is reported once, flagged bad. Mutation `one_phase` keeps a single grid. The preamble test was a set of per-chip ratios (each pulse twice its neighbouring gaps, every other gap under half the pulses' mean), which suit an envelope sampled a few times per chip. At 12.5 samples per chip a chip average of noise varies little, and a joint test is about 4 dB more sensitive: the weakest of the four pulses above the strongest of the twelve gaps, the pulses' mean at least 1.5 times the gaps' mean (`2 · hi4 > lo12`), and the summed pulses above `ADSB_CFG[23:8]`. Software sets that floor at twice the noise envelope's mean per pulse (`8 · 0.886 σ`). Mutation `strict_preamble` restores the old rules.
- **Radar CPI framing (`kria_radar_proc`, Artix `ddc_wrapper`).** The suite used to tie the CPI start to 0, so CPIs began wherever the stream was. The Artix now counts `dac_radar`'s chirp starts and, with `RADAR_CTRL[3]`, sets `I[0]` on the first sample of every 16th chirp, delayed by `RADAR_CTRL[7:4]` samples to cover the DDC's latency. With `DSP_CTRL[13]` the Kria captures only from the mark, keeps the marked sample as sample 0 and waits for the next mark after each CPI. Note that the AERIS DDC delivers the conjugate spectrum (`tb_e2e` checks it: a tone 1.5625 MHz above the IF lands at -1.5625 MHz), so a beat tone above the IF at range bin `r` and Doppler bin `d` appears in the map at `(64 - r, 16 - d)`. Software reads the map that way, or the RF chain puts the beat below the IF.
- **Radar stream packets (Artix `ddc_wrapper`, `top.v`).** The radar stream went out in 64-byte packets, so 3 of every 11 blocks on the uplink were header and CRC. With channel B of the AD9253 streaming as well, the two-lane uplink was

full and the 32-word FIFO dropped a word every 8 µs, which cut ADS-B frames and radar CPIs. The stream now uses 512-byte packets (the size `LINK_PROTOCOL.md` already gave) and a 128-word FIFO.

- **Transmit SSB (`kria_tx_mod`).** The 31-tap Hilbert transformer ran at the 25 MSPS tick rate, where it is flat down to DC for any audio tone, so USB and LSB came out double-sideband (opposite sideband 0 dB down). The internal test tone now uses its own sine as the quadrature (opposite sideband 49.9 dB down). External audio keeps the Hilbert, which is correct at audio rates. The quarter-wave table is linearly interpolated on the next 8 phase bits: CW SFDR 59.9 to 66.7 dBc.

Timing on the K26. The G-8 suite was written as single-clock arithmetic and verified in simulation only; the first K26 build with it in place missed `clk_pl_0` (`100 MHz`) by 13.8 ns on about 15,700 endpoints, and the radar took 84,000 LUTs because its corner-turn memory, written from two places in the reset branch, was built from flip-flops and multiplexers. Every block is now pipelined as a pure time shift: each stage carries its own valid bit, the arithmetic is unchanged, and the outputs are the same values in the same order, a few clocks later. Each new module was checked against the former one from `main` in a two-instance bench fed with the G-8 input files plus random bursts, gaps and output backpressure, comparing every output event (ADS-B 48 frames; channel 8 configurations, AM, USB, LSB, air, NBFM with CTCSS and WBFM with RDS; transmit modes 0 to 4; radar with and without the window and with `radar_sync`, 96 CPIs, 98,304 cells, 2,142 detections): no difference. The G-8 campaign on the pipelined suite gives the same results in all eight cases and the same figures (the transmit case's fitted carrier moves in the eleventh digit).

- **ADS-B.** The envelope and the chip sums are registered, and the chip average (a 24/7-bit divide) is a 4-stage restoring divider, one result per clock. The frame arbiter sees each sample 5 clocks later.
- **Channel receiver.** The mixer (phase, table, interpolation, products and rounding), the CIC combs, the FIR (16 products, 4 partial sums, sum, saturation) and the SSB Hilbert are pipelined. The demodulator (CORDIC, discriminator, de-emphasis, pilot PLL, CTCSS Goertzel, RDS) runs as a 6-step sequence per channel sample and changes state only in the last step, so it needs at least 6 clocks between channel samples: `CH_DECIM` must give `R · FIR decimation ≥ 6` (the shipped settings decimate by 50 or more). A simulation-only counter (`demod_overrun`) reports any violation.
- **Transmit modulator.** Nine stages from the phase accumulators to the DAC word, with an 8-word output FIFO; a new sample is started only while fewer than 14 words are in flight, so backpressure on `m_axis` loses nothing. With the internal tone every mode is bit-exact against the former module, with or without backpressure. With external audio (`ext_aud`, tied to 0 in the system) and backpressure the two versions drop different audio samples.
- **Radar.** Loads, butterflies, the corner turn, the power map and CA-CFAR are pipelines issued one cell per clock; the state machine waits in `ST_WAIT` until a pipeline has drained before the next phase reads what it wrote. The corner-turn memory has one write port (the capture, else the range-FFT store) and one registered read port, outside the reset branch, so it maps to block RAM; the power map is nine block-RAM copies, one per CFAR read. The radar now takes about 10,700 LUTs and 11 RAMB36. A CPI takes about 1,500 clocks more, and `cpi_done_pulse` still comes on the clock the processor returns to loading.

5.6 Kria GPS PPS (`kria_pps`, AXI-Lite at `0x8002_0000`, Rev08)

`fpga/kria/kria_pps.v` takes a GPS receiver's 1-PPS on `gps_pps`, which is KV260 `J9` (Raspberry Pi camera connector) pin 12, `HDA10`, ball `J12`, LVCMOS33 with a pull-down. It runs on `clk_pl_0`, the same 100 MHz as the AXI port.

What it does:

- Timestamps each GPS edge on a free-running 64-bit counter, after a 1 µs high-time qualification.
- Generates a disciplined second from a fractional period.
- Chooses what drives `PPS_SYNC` on the Pmod and the seconds of the link time stamps (`kria_pl_link` input `pps_ref`).
- Raises `pl_ps_irq0[4]` (GIC SPI 93).

R5F core 0 owns it (**`sw/kria/r5f`**); the loop is described in **INTEGRATIONS.md §2.1**. At reset it is in mode 0, so `PPS_SYNC` is the software GPIO (`EMIO GPIO[2]`) exactly as before the block existed.

Offset	Register	Fields
`0x00`	`CTRL`	`[1:0]` source of `PPS_SYNC` (`0` software GPIO, `1` GPS pulse after qualification, `2` generated), `[2]` IRQ enable, `[3]` generator on, `[4]` restart (W1, self-clearing: next generated edge at `NOW + PERIOD`)
`0x04`	`STATUS`	`[0]` capture pending (W1C), `[1]` GPS missing (no edge for 1.25 s), `[2]` glitch seen (W1C), `[3]` generated edge pending (W1C), `[31:16]` GPS edge count. Clear only the bits that were read
`0x08`, `0x0C`	`CAP_LO`, `CAP_HI`	Tick count of the last accepted GPS edge
`0x10`	`CAP_PERIOD`	Ticks between the last two accepted edges

Offset	Register	Fields
0x14, 0x18	GEN_PERIOD_INT, GEN_PERIOD_FRAC	Generator period: whole ticks and a 32-bit fraction
0x1C	GEN_ADJUST	Signed ticks added once to the next generated period
0x20, 0x24	GEN_LO, GEN_HI	Tick count of the last generated edge
0x28	WIDTH	Output pulse width in ticks (reset 100 ms)
0x2C, 0x30	NOW_LO, NOW_HI	Free-running counter; reading NOW_LO latches NOW_HI. Linux and the R5F stamp the shared mailbox with it
0x34	ID	0x50505331 ("PPS1")

Bench: tb_kria_pps (section 6), with the mutation pps_no_filter. Cost and timing: section 3.3.

5.7 Kria fusion grid (kria_bev_axi, AXI-Lite at 0x8003_0000, and axi_dma_1 at 0x8004_0000, Rev08)

kria_bev_axi puts the bird's-eye-view grid core (fpga/kria/integrations/kria_bev_grid.v, **INTEGRATIONS.md §6**) on the K26's buses. It has three ports:

- **Registers** (below), including a command port. R5F core 1 is its only writer: a command is two writes, so two writers could pair one's position with the other's command.
- **s_axis_det:** a stream input, one 36-bit command in the low bits of each 64-bit beat, for a LiDAR DMA. It is unconnected for now, so Vivado ties its tvalid to 0. The register queue has priority over it.
- **m_axis:** the dump, eight cells per beat with tlast on the 8,192nd, into axi_dma_1. That DMA is S2MM only, its interrupt is on pl_ps_irq0[5] (GIC SPI 94), and it writes the 64 KiB frame into one of two buffers at 0x3EE1_0000.

Offset	Register	Fields
0x00	ID	0x42455631 ("BEV1")
0x04	STATUS	[0] core busy (ray, decay or dump), [1] queue full, [2] overflow (W1C: a DET_CMD write found the queue full and was dropped), [3] queue empty, [25:16] queue level (512 entries)
0x08, 0x0C	ORIGIN_X, ORIGIN_Y	[8k+7:8k]: sensor k's origin cell, 128 the centre (reset 0x80808080)
0x10, 0x14	HIT, MISS	[7k+6:7k]: sensor k's detection increment and ray decrement (reset 0)
0x18	RAY	[3:0]: ray casting for sensor k (reset 0)
0x1C	DET_XY	[15:0] x, [31:16] y, signed Q8.8 cells from the centre; staged, read back
0x20	DET_CMD	Write: [1:0] sensor, [3:2] command (0 detection, 1 decay pass, 2 dump); pushes {DET_CMD[3:0], DET_XY}
0x24	COUNT	Commands the core has accepted from both inputs (wraps)

Change the configuration only while STATUS shows the queue empty and the core idle.

Bench: tb_kria_bev_axi (section 6), with the mutation bev_axi_no_stage. Cost and timing: section 3.3.

5.8 Kria KrakenSDR direction finding (kria_doa, AXI-Lite at 0x8005_0000, and axi_dma_2 at 0x8006_0000, 18 Nov)

fpga/kria/integrations/kria_doa.v takes a KrakenSDR's five aligned channels from the A53s (**INTEGRATIONS.md §9**) through axi_dma_2 (MM2S only, 64-bit), one snapshot of five signed 8-bit I/Q pairs per two beats, and:

- multiplies each channel by its calibration weight (complex Q2.14), y = (w x) >>> 10;
- accumulates the covariance $R = \Sigma\, y\, y^{H}$ over 2^N_LOG2 snapshots (15 entries, 48 bits each);
- scans 360 bearings, one per clock, $P(\theta) = \Sigma\, R_{ii} + 2\, \Sigma\, \mathrm{Re}(b_{ij}(\theta)\, R_{ij})$, from a table of steering cross-products in ten 512 × 32 block RAMs that the A53s write for the array and the frequency.

The A53s read R back for MUSIC. kria-sdrd reads R's diagonal after the CPI, sets SHIFT so the largest entry fits 25 bits, and asks for a scan of the held R (CTRL[2]). Registers: **INTEGRATIONS.md §9.1**. axi_dma_2's mm2s_introut is pl_ps_irq0[6] (GIC SPI 95).

Bench: tb_kria_doa (section 6) against the A53's bit-exact model, with the mutation doa_no_conj. Cost and timing: section 3.3.

5.9 Kria HackRF Pro sweep (`kria_sweep`, AXI-Lite at `0x8007_0000`, and `axi_dma_3` at `0x8008_0000`, 18 Nov)

`fpga/kria/integrations/kria_sweep.v` takes a HackRF Pro's sweep transfers as libhackrf delivers them (**INTEGRATIONS.md §10**) through `axi_dma_3`'s MM2S, 2,048 beats per 16 KiB block, and per block:

- checks the header (`0x7F 0x7F`) and keeps the 64-bit frequency; a bad block is dropped and counted (`BAD`);
- keeps the block's last 1,024 beats in block RAM and transforms the last `2^NSEG_LOG2` segments of 256 samples (default 8): Hann window from a table, radix-2 FFT with 1/2 per stage (22-bit data, Q1.15 twiddles from a table), power summed bin by bin;
- sends the frequency and 128 powers (bins 161 to 224 and 33 to 96, the two quarter bands) back through `axi_dma_3`'s S2MM, 65 beats with `tlast`.

Offset	Register
`0x000`	ID `SWP1`
`0x004`	STATUS: `[0]` busy
`0x008`, `0x00C`	BLOCKS, BAD
`0x010`, `0x014`	PSHIFT (output = sum >> PSHIFT, saturated to 32 bits), NSEG_LOG2 (0 to 4)
`0x400` + 4i	window, 256 entries, Q1.15
`0x800` + 4k	twiddles `exp(-j 2π k / 256)`, 128 entries: `[15:0]` cos, `[31:16]` −sin

One block takes about 54,500 clocks with 8 segments (1,024 butterflies of six clocks per segment, in one block RAM with one write and one read port), 0.545 ms at 100 MHz, against 0.82 ms between blocks of a sweep; `tready` is low while a block is processed. `axi_dma_3`'s `s2mm_introut` is `pl_ps_irq0[7]` (GIC SPI 96); its MM2S completion is polled, as the eight interrupt lines of `pl_ps_irq0` are all used.

Bench: `tb_kria_sweep` (section 6) against the A53's bit-exact model, with the mutation `sweep_twiddle_conj`. Cost and timing: section 3.3.

5.10 The PL's results to the A53s (`kria_dsp_out`, `kria_ps_framer`, 18 Nov)

Until 18 November the DSP suite's results reached the PS only as status registers (the last audio pair, the last ADS-B word, the radar's peak), and `axi_dma_0`'s S2MM channel received the link's packets one by one: a transfer of at most 512 bytes each, about 200,000 re-arms a second at the AD9484 stream's rate, with each packet's stream id lost (the DMA writes only `tdata`). Two blocks close that gap for the in-car software (**HMI.md §4**).

`fpga/kria/kria_dsp_out.v`, inside `kria_dsp_suite`, packs the results as the streams `8'h20` to `8'h23` of §5.1. Each source has its own FIFO, and the arbiter sends whole packets round robin. An audio packet that waits 2 ms for its next sample ends early. A map starts only when its FIFO has room for all of it, otherwise that CPI's map is skipped. Samples or frames that meet a full FIFO, detections beyond 64 and skipped maps set `0x60[3]` (sticky). `DSP_CTRL[14]` turns the streams on; `DSP_CTRL[18:15]` sets how often a map is sent.

`fpga/kria/kria_ps_framer.v` sits between `kria_pl_link` and `axi_dma_0`. It takes the link's uplink packets (input A, with the stream id and the CRC flag) and the results (input B), stores each packet whole in a 4,096-word FIFO (32 KiB, which also covers the DMA's re-arm time), and sends it behind two header words:

Word	Content
0	`{0xA5, tid[7:0], flags[7:0], 0x00, words[15:0], seq[15:0]}`; flags `[0]` CRC error, `[1]` from input B; `seq` counts every packet, so a gap shows a loss
1	The 64-bit `pl_clk_100m` tick count when the packet's last word arrived (10 ns)

`tlast` goes on the last word of the first packet that brings the block to 8,192 words (64 KiB) or more, so a transfer is at most 8,706 words: Linux arms S2MM with 69,648 bytes and reads `S2MM_LENGTH` for what came. When nothing is pending for 1 ms and the block holds data, a flush packet (`tid 0`, 0 words) ends it. The inputs alternate when both have a packet waiting. `tb_kria_ps_framer` drives both inputs with every stream type, random gaps and output backpressure: 798 of 798 packets in order with correct headers, 136 blocks, 1 flush, 3,000 audio samples, 133 of 133 ADS-B frames, 12 CPI summaries and 6 maps. Its two mutations fail as they should (`MUTATE_FRAMER_LAST_EVERY_PACKET`, `MUTATE_MAP_NO_NORMALISE`). `kria-hmi-core::frame` is the software side and is tested on the same format.

5.11 PS CAN1 through EMIO (18 Nov)

`fpga/kria/bd.tcl` enables the Zynq PS controller `CAN1` (`0xFF07_0000`, `PSU__CAN1__PERIPHERAL__IO {EMIO}`) with a `100 MHz` reference clock (`PSU__CRL_APB__CAN1_REF_CTRL__SRCSEL {IOPLL}`, `DIVISOR0 {15}`, `DIVISOR1 {1}`).

- **`can1_txn` (TX):** `ps8/emio_can1_phy_tx` is inverted by `can1_tx_inv` (`util_vector_logic`, `C_OPERATION {not}`, `C_SIZE {1}`) to top-level port `can1_txn[0:0]` on ball `G6` (`KV260 J9` pin 6, `DATA1_P`, `SOM240_1 A9`, `LVCMOS12`, `DRIVE 4`, `SLEW SLOW`, Bank 66).
- **`can1_rx` (RX):** Top-level input `can1_rx` on ball `D6` (`KV260 J9` pin 8, `CLK_N`, `SOM240_1 C13`, `LVCMOS12`, `PULLUP TRUE`, Bank 66) feeds `ps8/emio_can1_phy_rx`.
- **Bank 66 voltage and level shift:** Bank 66 on the K26 SOM is powered at `PL_1V2` (`1.2 V`), so **`fpga/kria/xck26_bd.xdc`** constrains both pins as `LVCMOS12`. On the Rev08 adapter (`STATUS` sheet), `can1_txn` drives a pair of `MMBT3904` NPN transistors (`Q1530`, `Q1531`) wired as a `3.3 V` NOR stage into `U1506` (`TCAN3403DDFRQ1`, `3.3 V`, pin 5 `VIO` on `+3V3_D`, `STB` low, `±58 V` bus), and `CAN_RXD` is stepped down from `3.3 V` to `1.18 V` by a `1.8 kΩ / 1 kΩ` divider (`R1556` / `R1557`); see **INTEGRATIONS.md §2.2**.

6. XSim & Full-System Verification Suite (`fpga/sim/`)

Every module and top-level integration is verified in AMD/Xilinx `xsim` (`Vivado 2026.1`) with unified primitive models (`unisims_ver`, `secureip`, `glbl`) and behavioral hardware board/IC models (`fpga/sim/models/`):

```
# Run full dual-FPGA + PCB board + analog converter co-simulation (500 MHz & 400 MHz):
.\fpga\sim\run.ps1 tb_system
.\fpga\sim\run.ps1 tb_system -Define FPGA_CLK_400M

# Run SGMII, Clock Mode Switch, & Mutation Benches:
.\fpga\sim\run.ps1 tb_clk_mode_switch
.\fpga\sim\run.ps1 tb_clk_mode_switch -Mutate no_delta_clamp
.\fpga\sim\run.ps1 tb_rev06
.\fpga\sim\run.ps1 tb_rev06 -Mutate no_phase_select
.\fpga\sim\run.ps1 tb_rev06 -Define FPGA_CLK_400M
.\fpga\sim\run.ps1 tb_rev06 -Define FPGA_CLK_400M -Mutate ias_ok_dl_only
.\fpga\sim\run.ps1 tb_e2e
```

Bench	Scope Verified
`tb_system.v`	Full end-to-end co-simulation (S1..S7) at both `500 MHz` and `400 MHz`, including A-1 `500 MHz` reset gating, `500->400 MHz` unlock & retrain, PS `UART1` EMIO `0xE8` readback, and S7 `TX_KEY` (`0x38`) key-word & read-only `DSP_CTRL[1]` checks (`-Mutate tx_key_from_dsp_ctrl` fails at S7)
`tb_kria_bev_axi.v`	`kria_bev_axi` against the bit-exact grid model: ID, reset values, configuration read-back; the fog run's 974 commands (or, with `+BEV_DIR=../radar_grid`, the 2,705 that R5F core 1's code produced in `examples/radar_grid.rs`) sent in blocks of 64 alternating between `DET_XY`/`DET_CMD` and `s_axis_det` with random gaps, the dump compared cell by cell under random backpressure; `COUNT`; with the sink stalled during a second dump, 513 pushes leave the queue full at 512 with `STATUS.overflow` set, cleared by W1C; mutation `bev_axi_no_stage` (exit `1`)
`tb_kria_pps.v`	`kria_pps` over AXI-Lite with 10,000-tick seconds: ID, mode 0 forwarding, captures and IRQ, capture period, mode 1 after qualification, a 5-tick glitch (flagged, not captured or forwarded), missing GPS, the fractional generator (8 s of 10,000.25 ticks = 80,002), one-shot adjust, a closed loop holding the generator within 1 tick of a 10,000.37-tick GPS second, and holdover; mutation `pps_no_filter` (exit `1`)
`tb_kria_doa.v`	`kria_doa_axi` from the A53's own files (`kria-sdrd kraken-pre`, `+DOA_DIR`): ID, the driver's 3,606 register writes (weights, steering table, `N_LOG2`), a CPI of 32,768 snapshots with gaps in `tvalid`, R's diagonal read back and `SHIFT` chosen from it as the driver does, the rescan; all 15 entries of R and all 360 bearings of P equal the bit-exact model; `DROPPED` = 0; writes `doa_rtl.txt` for `kraken-post`; mutation `doa_no_conj` (exit `1`)
`tb_kria_sweep.v`	`kria_sweep_axi` from the A53's own files (`kria-sdrd hackrf-pre`, `+SWEEP_DIR`): ID, window, twiddles, `PSHIFT` and `NSEG_LOG2`; one 720-block sweep from 0 to 7.2 GHz (1.47 M beats, random gaps in `tvalid`) with one corrupted header; every one of the 46,735 output beats and its `tlast` equals the bit-exact model under random back-pressure; `BLOCKS` = 719, `BAD` = 1; writes `sweep_rtl.hex` for `hackrf-post`; mutation `sweep_twiddle_conj` (exit `1`)
`tb_kria_ps_framer.v`	`kria_dsp_out` and `kria_ps_framer` together: the link's packets of every stream type on input A and the DSP suite's audio, ADS-B, CPI and map events on input B, random gaps and output back-pressure; every packet comes out whole, in order, with its header, sequence number and stream id (798 of 798), blocks end at 64 KiB or on the 1 ms flush (136 blocks, 1 flush), 3,000 audio samples, 133 of 133 ADS-B frames, 12 CPI summaries, 6 maps; mutations `MUTATE_FRAMER_LAST_EVERY_PACKET` and `MUTATE_MAP_NO_NORMALISE` (exit `1`)
`tb_dbg_uart.v`	G-1 `dbg_uart` boot banner, periodic `STAT`, `r`/`w`/`s`/`h` CLI, 4-master CSR collision arbitration, `BREAK` recovery (`500 MHz` & `400 MHz`) + mutations `wrong_divisor` & `drop_monitor_write` (exit `1`)
`tb_clk_mode_switch.v`	Safe-boot Si549 `500 MHz` init, A-1 radar path reset/retrain on `500<->400 MHz` switch, and `±50 ppm` `ADPLL_DELTA_M` Ethernet clamp (`500 MHz` & `400 MHz`, + `-Mutate no_delta_clamp`)
`tb_dual_path_drain.v`	`dual_path_sf_fifo` drain while the IAS1 uplink is closed: bulk dropped whole on both sides, `0x11` kept and sent first, a started packet never cut, a started discard runs to its `eop` (`-Mutate drain_started_pkt`, `drain_all_sid`, `drain_release`, `drain_no_wskip`)

Bench	Scope Verified
`tb_rev06.v`	`1.25 Gb/s` SGMII `XAPP523` oversampler across `+100/-100 ppm` crystal drift, UDP CSR write, ARP/ICMP, failover `SPLIT`/`MIRROR`/`IAS_ONLY`/`ETH_ONLY` with `0` lost packets (`500 MHz` & `400 MHz`); at `400 MHz`, Phase 2b drops the Kria's receiver with the downlink up and `0x01` must move onto ETH and back. Only what the IAS1 drain discards is excused: the `0x01` packets made before the uplink first opens, and those queued for IAS1 when it closes (at most the FIFO's 32 packet slots; `-Mutate ias_ok_dl_only` fails)
`tb_e2e.v`, `tb_artix_top.v`	End-to-end AD9484 400 MSPS -> AERIS DDC (`500 MHz` A-1 isolation & `400 MHz` CW FFT), `64b/66b` IAS1 -> `kria_pl_link` (`0` CRC/seq/proto errors; verified at both `500 MHz` and `400 MHz`)
`tb_ddc_500`	Gain within 0.25 dB of the model at +1, +5, +9 and -7 MHz (measured within 0.04 dB); image at least 60 dB down (79 to 93 measured); `CONJ`; alias rejection at +103 MHz (-88 dB) and +21 MHz (-59 dB); lane-order image at NCO 187.5 MHz (-96 dB); SNR at least 50 dB (55.2 measured for 0.4 LSB ADC noise); one output per 5 clocks; packet payload, sequence, no drops; mutations `d2_nco_lane0` (gain -12.5 dB), `d2_lane_swap` (lane-order image at -1.4 dB)
`tb_nco_image`	AERIS NCO alone: the conjugate-LO component of `cos + j sin` at least 70 dB below the wanted one in each of 12 windows of 40,000 samples (4 at the default FTW, 8 with the FTW 64 LSB higher, so the accumulator's position in its truncation cell drifts across the run); `-81.3 dB` worst measured. Mutations `nco_int_lut` (upstream table, `-52 dB`) and `nco_no_phase_dither` (`-52` to `-62 dB`) each fail
`tb_adc_cap500`	`adc_capture` in `mode_500` with a 250 MHz DCO (skew -90..+5 ps, +/-80 ps edges): training on `refclk_200m` with the MMCM in reset (eye 22 taps); a 4000-word ramp arrives in order with no gap or slip; then 400 MSPS training still works (eye 29 taps); mutations `d2_word_order`
`tb_artix_top` (500 MHz boot)	D2 CSR readback; D2 on at 250 MHz with the AD9484 model on the master clock: trained, stream `0x01` packets, first sample `I` = 8322 (8299 expected), `Q` = -6; D2 off mid-stream releases the uplink
`tb_adcs_capture.v`, `tb_adc_ddc.v`	AD9253 1-lane 16-bit DDR FCO bitslip alignment (`500`/`400 MHz` DCO -> `62.5`/`50.0 MSPS`) + Dual-Ch SDR DDC & AD9484 IDELAY auto-training (`500 MHz` & `400 MHz`)
`tb_dac_tx.v`, `tb_adar_ctrl.v`, `tb_hk.v`, `tb_pmod_spi.v`, `tb_link_*`, `tb_pcs_*`, `tb_serdes*`	Non-MMCM `÷4` `dac_clk` LFM chirp & `hf_dac2_mode` TX, 8-chip ADAR1000 SPI & guard bands, the Rev08 scan mode (five strobes load beams 0, 1, 2, 0, 1 with their own weights; mutation `scan_ignored`), TMP1075/Si549 I2C, XADC/PPS, Pmod SPI, 2-lane PCS deskew & `IDELAYE3` eye centering (all 19 benches pass at `500 MHz` & `400 MHz`)

*(See **`SYSTEM_SIM.md`** for the complete recorded output logs of every testbench.)*

6.1 Signal-level verification (Rev08 G-8)

`fpga/sim/signals/g8_suite.py` (shared code in `g8_lib.py`) puts realistic signals for every use of the board through the real RTL and compares what comes out with a floating-point reference. Run it with `python fpga/sim/signals/g8_suite.py [case ...]`, cases `hf_am hf_ssb fm air nbfm adsb tx radar`. It writes `results.json` next to the script and the figures to `docs/img/sim/g8_*.png`. Parallel runs set `G8_SUFFIX` so that their snapshots, work files and results stay apart.

Each receive case runs in three steps, all on the RTL:

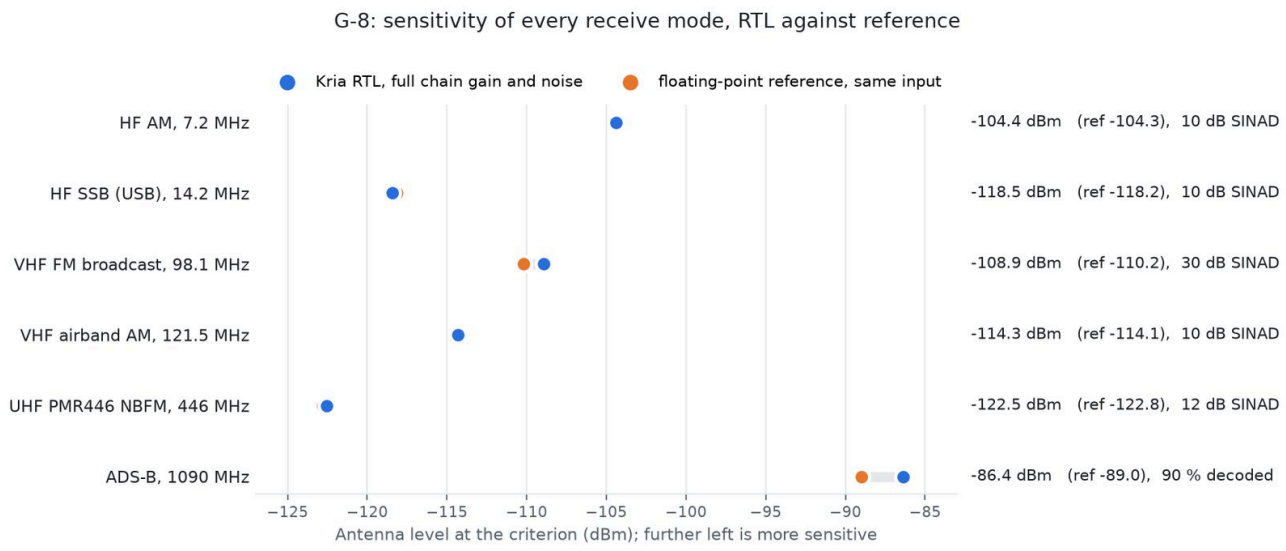
1. **Calibration, full chain.** A CW at a known antenna level, with the cascade's thermal noise for that input (noise figure from the RF budget), goes through the ADC model, the Artix DDC, the board's LVDS channel model, the IAS1 link and into the Kria (`tb_system_signals`). The stream the Kria receives gives the chain's gain (output code amplitude per antenna volt), the noise density at the Kria's input, the tuning error and, for the AD9484 path, the DDC's image rejection (tone and mirror fitted together by least squares).
2. **Scene, full chain.** The case's realistic scene (modulation, fading, adjacent channels, blockers, colliding replies, radar targets) goes the same way. Its spectra, waterfall and decoded output make the figures and check that the chain demodulates what was sent.
3. **Sweep, Kria RTL alone.** A full-chain run of a few milliseconds yields only a few audio samples, so the level sweeps feed the Kria blocks directly (`tb_dsp_sweeps`, paced at the stream's real sample rate on the 100 MHz clock) with the CSR values the scene used. The input is the baseband the Artix would deliver: the signal scaled by the measured gain, plus complex noise at the measured density. A floating-point reference demodulator gets the same input, and the RTL must stay within a stated margin of it.

Each case also runs at least one **mutation** (`run.ps1 -Mutate`): a deliberate fault in the RTL that its checks must catch. No result has a fallback value; an empty or missing output stops the run.

Results on the RTL of this revision (`fpga/sim/signals/results.json`, re-run on 18 November 2026 on the final Rev08 RTL; against the run of 17 November the figures moved by 0.9 dB at most (the PMR446 reference), all within their criteria). Levels are at the antenna connector; "reference" is the floating-point demodulator on the same input. In every receive case the noise density at the Kria's input is within 1.3 dB of the cascade's prediction and the tuning error is under 20 Hz; on the AD9484 path the DDC's mirror is 52 to 69 dB down. The AD9484 cases (FM, airband, VHF/UHF NBFM, ADS-B, radar) were run again on the NCO fix of 17 November (`results_nco.json`, figures regenerated), and all pass. That mirror figure is the capture's noise, not the NCO: in 300 us of capture, the least-squares fit of the mirror bottoms out at 56 to 60 dB below

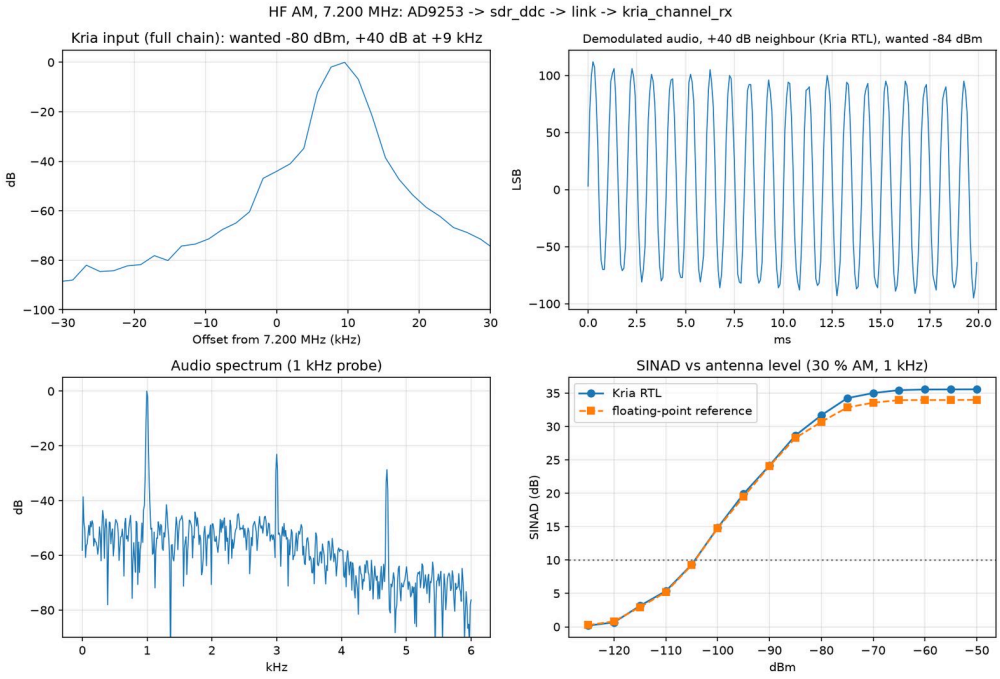
the tone for these carrier-to-noise ratios, and its spread is that of noise. The NCO's own image is `-81 dB` or lower (`tb_nco_image`).

Case	Path	Result (RTL vs reference)	Scene, full chain	Mutations caught	Checks
HF AM, 7.2 MHz	AD9253 B, `sdr_ddc`, AM	10 dB SINAD at -104.4 dBm (-104.3); a +40 dB signal 9 kHz away costs 2.0 dB	Fading AM with impulses demodulated	`cordic_no_frac` (10.0 to 5.5 dB)	6 / 6
HF SSB, 14.2 MHz USB	AD9253 B, `sdr_ddc`, USB	10 dB SINAD at -118.5 dBm (-118.2); opposite sideband 56.4 dB down	Fading USB speech with QRN	`swap_usb_lsb`	6 / 6
FM broadcast, 98.1 MHz	AD9484, AERIS DDC, WBFM	30 dB SINAD at -108.9 dBm (-110.2); stereo separation 32.6 dB; RDS BER 0 from -105 dBm up	Pilot locked with a +60 dB blocker 2.2 MHz away	`rds_no_timing`	9 / 9
Airband AM, 121.5 MHz	AD9484, AERIS DDC, AM, five-stage CIC	10 dB SINAD at -114.3 dBm (-114.1); neighbours +25 dB at 8.33 kHz and +35 dB at 25 kHz cost 0.0 and 0.1 dB	8.33 kHz channel plan	`mix_nco_9bit` (29.2 to 22.7 dB)	7 / 7
PMR446 NBFM, 446.00625 MHz	Converter, AD9484, AERIS DDC, NBFM	12 dB SINAD at -122.5 dBm (-122.8); CTCSS detected there, no false detection 20 dB higher; EN 300 296 neighbour +40 dB at 12.5 kHz costs 0.1 dB (reference 0.0)	NBFM, CTCSS and a +40 dB neighbour	`mix_truncate` (11.3 to 2.1 dB), `wrong_atan_lut`	9 / 9
ADS-B, 1090 MHz	Converter, AD9484, AERIS DDC, `kria_adsb_rx`	90 % decode at -86.4 dBm (timing-aware reference -89.0)	3 of 3 overlapping replies CRC-good	`unpack_no_queue` (0 of 3), `one_phase`, `strict_preamble`	8 / 8
Radar, FMCW at 120 MHz IF	AD9484, AERIS DDC, CPI mark, `kria_radar_proc`	Pd 0.5 at -18.83 dB per sample (model -18.74); Pfa 1.99e-2 (model 2.00e-2)	Targets at 0, -10 and -30 dB all detected, none elsewhere; beam scan peaks at the target's -15 degrees	`wrong_twiddle_sign`	7 / 7
Transmit	`kria_tx_mod`, link, `dac_sdr` / `dac_radar`	AM and NBFM SINAD 83 and 58 dB, adjacent channel -80 and -66 dBc; USB opposite sideband 49.9 dB, carrier 81 dB down; CW SFDR 66.7 dBc	AM at the AD9767 pins on a 3.125 MHz carrier, depth 0.80; 24 radar chirps at the programmed start and slope	`flip_usb_q`	10 / 10

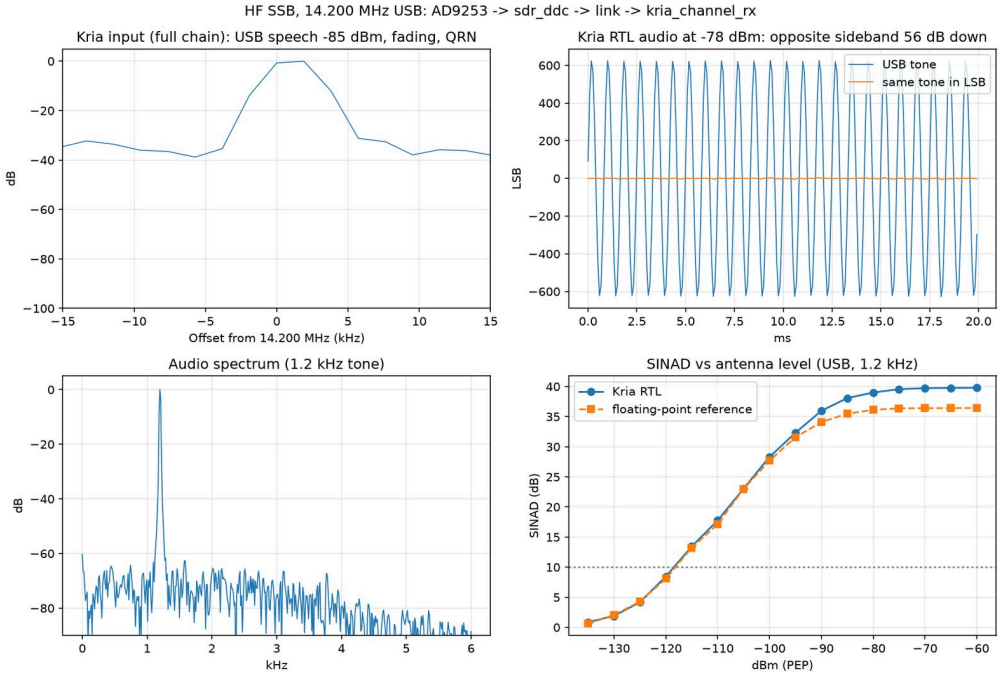


G-8 sensitivity of every receive mode

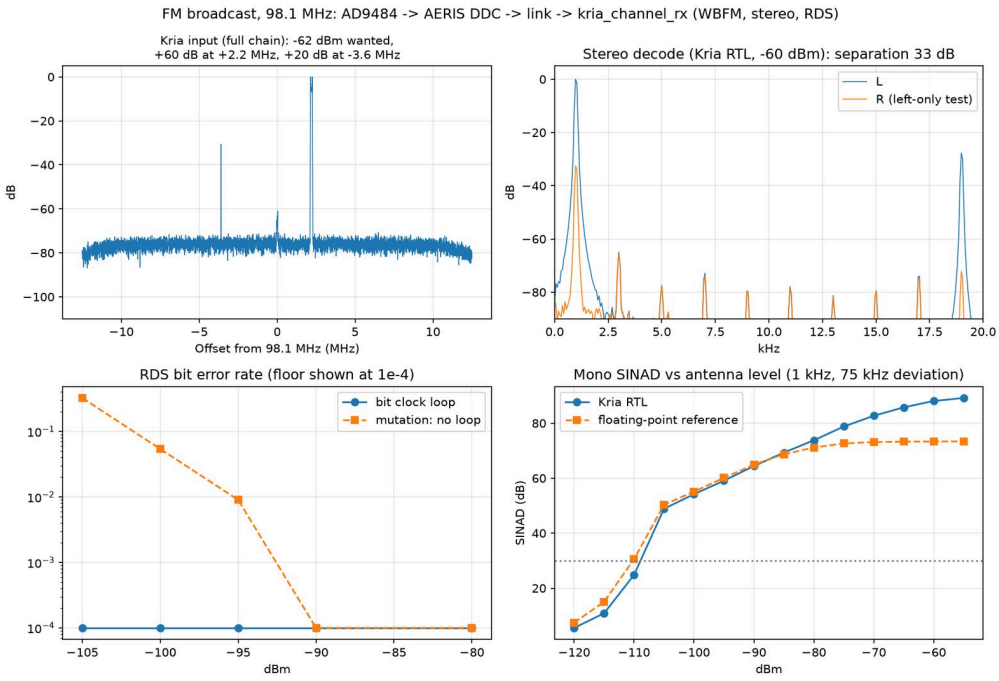
`python fpga/sim/signals/g8_overview.py` draws this summary from `results.json`. The figures of each case follow: the Kria's input from the full chain, the decoded output, and the sweep of the RTL against the reference.



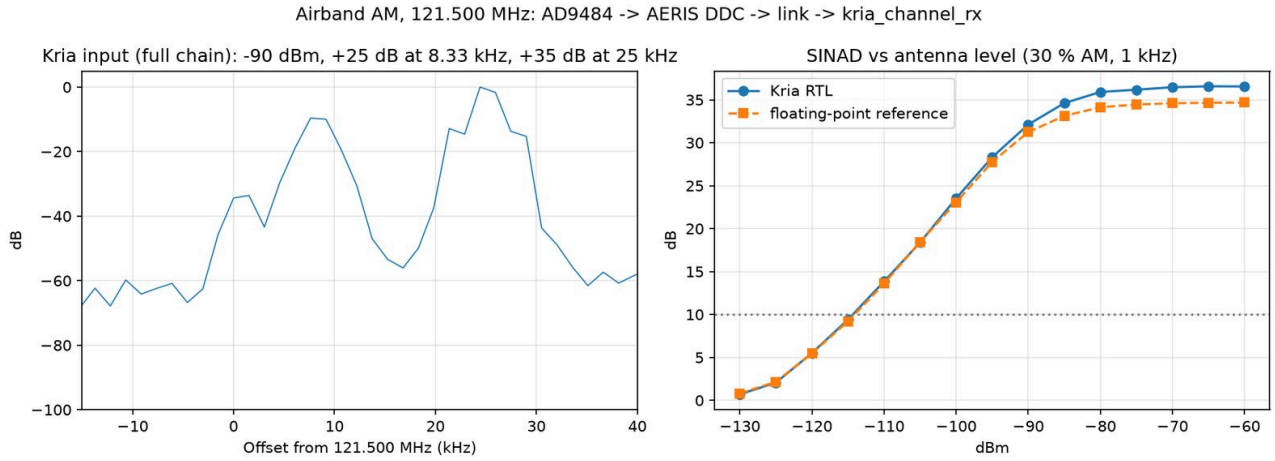
HF AM, 7.2 MHz



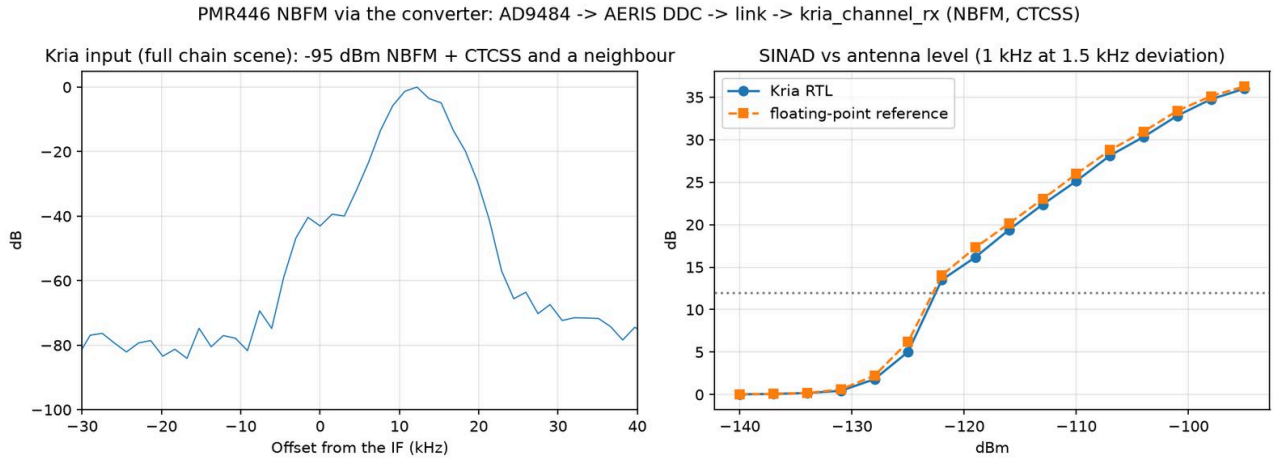
HF SSB, 14.2 MHz USB



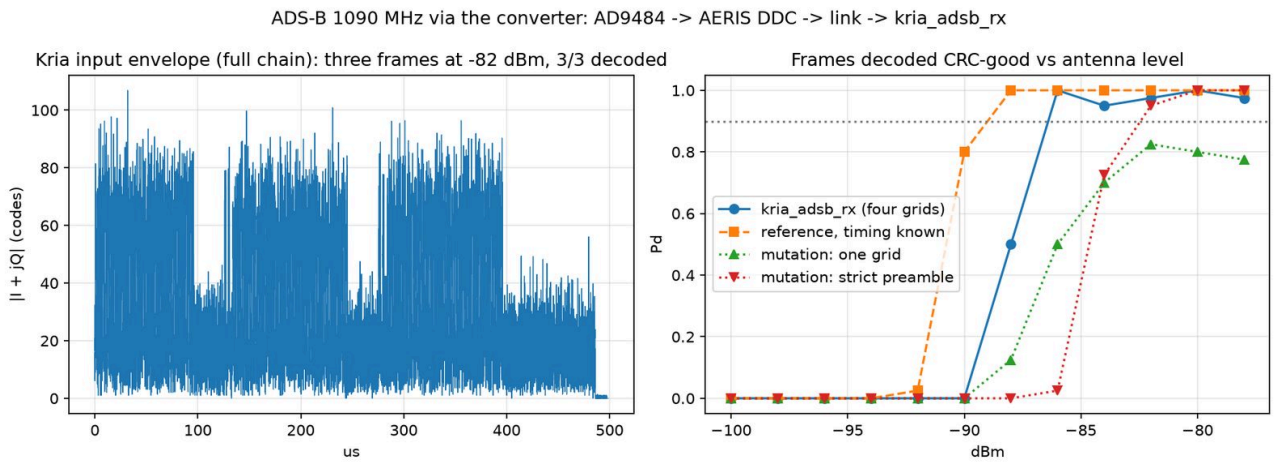
FM broadcast, 98.1 MHz



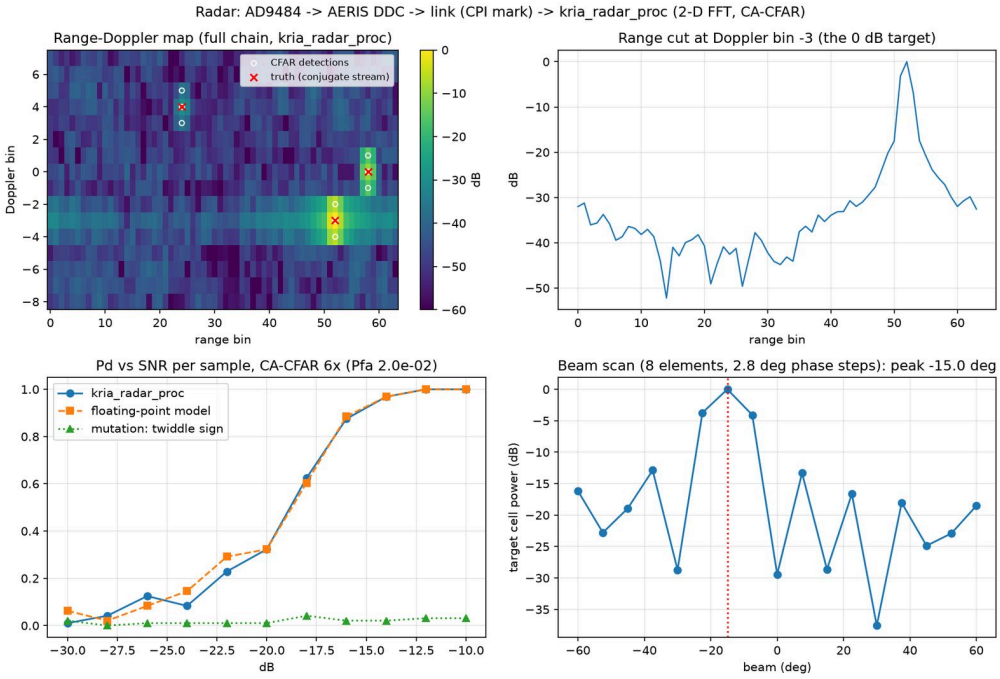
Airband AM, 121.5 MHz



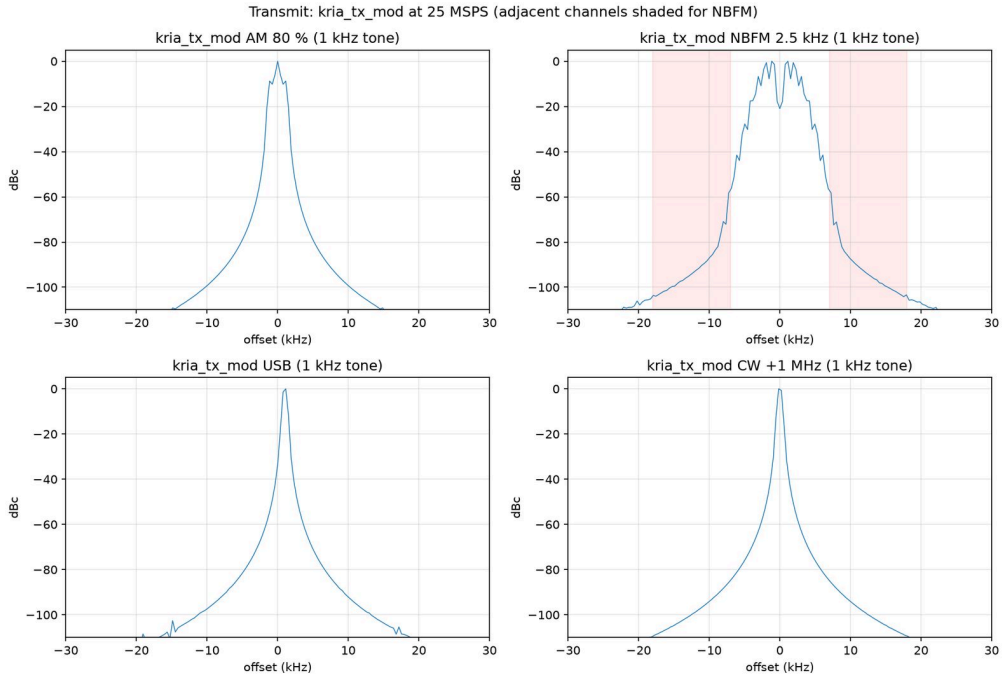
PMR446 NBFM, 446 MHz



ADS-B, 1090 MHz



Radar, range-Doppler map and CA-CFAR



Transmit, spectra against their masks

Two properties of the chain show up in these numbers and matter to software. The AERIS DDC delivers the conjugate spectrum, so on the AD9484 path the channel NCO is set to minus the offset and the radar map is read at `(64 - r, 16 - d)`. The first radar CPI after the stimulus starts holds the DDC filters' start-up transient (Doppler sidelobes near -30 dBc even in floating point), so the first map after enabling the radar should be discarded.

Source: fpga/README.md

FPGA Gateware: Dual-FPGA RTL, Vivado Builds & XSim Verification

This folder contains the complete synthesizable Verilog gateware, Vivado 2026.1 constraints/build scripts, and full-system XSim co-simulation testbenches for both FPGAs in the **KV260-IAS2RF** platform (**Apache License 2.0**, with `third_party/aeris/` under MIT).

> **Comprehensive Documentation & Vivado Silicon Renders:** See **`docs/FPGA_GATEWARE.md`** for complete post-route Vivado silicon die floorplans (`XC7A50T` & `XCK26`), hierarchical circuit schematics, complete SDR (direct HF `0–31.25/25 MHz` & external-converter VHF/UHF) & `AERIS-10` (`10.5 GHz` / `20 km` / `8x ADAR1000`) signal chains, the `dbg_uart` monitor, and the full `0x00..0xFC` register map.

Layout

Folder / File	Purpose
`artix/`	Front-end `XC7A50T-FTG256-2` RTL (`top.v` with integrated Radar DDC, Dual-Ch SDR DDC, `dac_radar`, `dac_sdr`, `adar_ctrl`, `rf_switch`, `eth_sgmii_phy`, `eth_mac_udp`, `dual_path_mux`, `dbg_uart`, `hk_*`, `pmod_spi`; Rev08: `fe_ctrl` on `hk_xo_ctrl`'s I2C client port for the two TCA6416A expanders, and through them the VHF/UHF front end's switches, bias tee, RFFC5072 and PE4312 and the status LEDs, `fe_agc`, the 500 MSPS AD9484 path D2 `ddc_500`/`ddc500_rom`, and the beam-scan mode of `adar_ctrl`), `xc7a50t.xdc`, `build_rev06.tcl`, and routed reports (`reports_rev06/`)
`kria/`	Kria KV260 `XCK26-SFVC784-2LV-c` PL core (`top.v`, `kria_pl_link.v`, `link_axis.v`, PS `UART1` EMIO, PS `CAN1` EMIO with `can1_txn`/`can1_rx` on `J9` pins 6 and 8; Rev08: `TX_KEY` at `0x38`, the DSP suite `kria_dsp_suite` with `kria_channel_rx`, `kria_adsb_rx`, `kria_radar_proc`, `kria_tx_mod`, `kria_cordic` and `kria_dsp_out`; `kria_ps_framer`; `kria_pps`; the fusion grid `kria_bev_axi` with `integrations/kria_bev_grid.v`; the KrakenSDR and HackRF Pro blocks `integrations/kria_doa.v` and `integrations/kria_sweep.v`), Vivado IPI block design (`bd.tcl`), `xck26.xdc`, `build.tcl`, and routed reports (`reports/`)
`link/`	Shared bidirectional `64b/66b` IAS1 PCS (`link_crc32`, `link_scrambler`, `link_gearbox`, `link_framer`, `link_lanes`, `link_rx_train_fsm`, `link_top`) + **`LINK_PROTOCOL.md`** & **`PINMAP.md`**
`third_party/aeris/`	Verbatim `PLFM_RADAR` (`62d4c55`, MIT) 400 -> 100 MSPS radar DDC modules (`ddc_400m.v`, `nco_400m_enhanced.v`, `cic_decimator_4x_enhanced.v`, `fir_lowpass.v`, `ddc_input_interface.v`, `cdc_modules.v`)
`eth/`	`1000BASE-T` SGMII feasibility, pin-dedicated implementation notes (**`REV06.md`**), failover architecture (**`REDUNDANCY.md`**), and standalone SGMII XSim bench
`sim/`	Vivado `xsim` runner (`run.ps1`), behavioral RF/IC/PCB board models (`sim/models/`), unit benches (`tb_*`), and full-system dual-FPGA co-simulation (`tb_system.v`)
`export_vivado_views.tcl`	Batch TCL extractor dumping placed cells, clock regions, architectural columns, and module statistics from post-route Artix-7 and Kria K26 checkpoints

Vivado 2026.1 Post-Route Implementation Status

<!-- fpga-figures:begin -->

Design (Vivado 2026.1)	Device	LUTs	FFs	BRAM36 eq.	DSPs	WNS / WHS	Failing endpoints	Reports
`artix_top`	XC7A50T-FTG256-2	25,279 (77.5 %)	28,970 (44.4 %)	18.0 (24.0 %)	119 (99.2 %)	+0.007 / +0.033 ns	0 of 83,391	**`artix/reports_rev06/`** from **`build_rev06.tcl`**
`ias2rf_k26_bd_wrapper`	XCK26-SFVC784-2LV-c	53,336 (45.5 %)	46,896 (20.0 %)	44.0 (30.6 %), 1 URAM	229 (18.3 %)	+1.043 / +0.010 ns	0 of 188,554	**`kria/reports/`** from **`bd.tcl`**

Post-route, generated from the Vivado reports by `_work/fpga_figures.py` (artix_top: Thu Nov 19 04:24:55 2026; ias2rf_k26_bd_wrapper: Thu Nov 19 09:53:51 2026). <!-- fpga-figures:end -->

Batch Build & Simulation Commands (Vivado 2026.1)

```
# Build Artix-7 bitstream & post-route reports
```

```
<Vivado 2026.1 install>\bin\vivado.bat -mode batch -nojournal -nolog -source fpga/artix/build_rev06.tcl

# Build Kria K26 Vivado Block Design + XSA + bitstream
<Vivado 2026.1 install>\bin\vivado.bat -mode batch -nojournal -nolog -source fpga/kria/bd.tcl

# Run XSim unit, E2E, SGMII & full-system dual-FPGA co-simulations
.\fpga\sim\run.ps1 tb_system
.\fpga\sim\run.ps1 tb_system -Define FPGA_CLK_400M
.\fpga\sim\run.ps1 tb_dbg_uart
.\fpga\sim\run.ps1 tb_rev06
.\fpga\sim\run.ps1 tb_e2e
```

For detailed simulation results across every testbench, see **`SYSTEM_SIM.md`**. For PetaLinux / user-space software bring-up on the K26 PS, see **`sw/README.md`**.

Source: fpga/SYSTEM_SIM.md

Full-System Co-Simulation (`tb_system`)

End-to-end mixed-signal/digital XSim co-simulation connecting the real front-end Artix-7 RTL (**`artix_top`**, `ENABLE_ETH = 1`) and the real Kria K26 PL wrapper (**`kria_pl_link`**) across 8-layer LVDS IAS1 and dedicated-pin 1000BASE-T SGMII (`ETH_SGTX 404/402 ps`, `ETH_SGRX 464/468 ps`) channel models, behavioral converter/RF/housekeeping peripherals, and a behavioral RTL8211FSI + PS GEM3 SGMII/UDP peer. Both eye-scan FSMs (`u_kria.u_train_fsm`, `u_artix.u_dl_train_fsm`) run at their hardware-default `TAP_DWELL_CYCLES = 1800` with live front-end streaming enabled from `t = 0` (`emio_gpio_o = 8'h00`).

Run from the repository root:

```
.\fpga\sim\run.ps1 tb_system
.\fpga\sim\run.ps1 tb_link_a2k
.\fpga\sim\run.ps1 tb_link_a2k -Define STREAM_FROM_T0
.\fpga\sim\run.ps1 tb_link_a2k -Mutate no_train_gate
.\fpga\sim\run.ps1 tb_rev06
```

Optional fault/mutation checks (max 2 concurrent runs, batch XSim only):

```
.\fpga\sim\run.ps1 tb_system -Mutate bad_channel_skew
.\fpga\sim\run.ps1 tb_system -Mutate no_echo_return
.\fpga\sim\run.ps1 tb_system -Mutate eth_skip_fcs
.\fpga\sim\run.ps1 tb_system -Mutate no_retrain
.\fpga\sim\run.ps1 tb_system -Mutate tx_key_from_dsp_ctrl
```

Note: **`run.ps1`** copies **`fpga/sim/design.txt`** (`TEMP 42.5`, `VCCINT 1.00`, `VCCAUX 1.80`) into `fpga/sim/out/work_<runName>/` so the Artix XADC model receives deterministic telemetry stimulus.

Modeled Interfaces & Behavioral Components

Simulation resolution is `` `timescale 1ps/10fs `` (**`tb_system.v`**; `xsim` reports `Time resolution is 10 fs`).

Component / Model	File	Modeled Behavior
Artix-7 Top RTL	**`artix/top.v`**	Real `artix_top` (`ENABLE_ETH = 1`), Si549 `500 MHz` (`#1000.000` ps half-period, default) and `400 MHz` (`#1250.000` ps, `-Define FPGA_CLK_400M`), with A-1 radar reset gate + G-1 `dbg_uart` monitor
Kria K26 PL Wrapper	**`kria/kria_pl_link.v`**	Real `kria_pl_link` with AXI4-Lite CSRs (including `TX_KEY` at `0x38` and read-only `DSP_CTRL[1]` + `kria_dsp_out` result readback), 64-bit AXI4-Stream TX/RX DMA, MMCM, `IDELAYE3`/`ISERDESE3`, `u_train_fsm`, PS `UART1` EMIO -> `pmod_spare1/2`, configurable `pl_clk_100m` (`4999.500` ps `+100 ppm` initial, `-100 ppm` in S5)
LVDS Channel & Fault Hook	**`sim/models/board_lvds_channel.v`**	`sim_board_lvds_channel`: independent `DLY_P_PS` / `DLY_N_PS` leg delays, PRNG differential timing jitter (`JITTER_SPREAD_PS`), transport delays preserving multi-UI transitions (`>1000 ps` @ 1 Gbps), dynamic `cut_fault` and `glitch_inj` inputs
AD9484 400 MSPS Radar ADC	**`sim/models/ad9484_radar_model.v`**	`sim_ad9484_model`: 3-wire SPI (Chip ID `0x6C`), inverted DCO routing, `lvds_skew.py` per-bit skew + eye spread; `mode=0` (`0xAA`/`0x55` IDELAY calibration), `mode=1` (`121.5625 MHz` IF CW -> `+1.5625 MHz` baseband @ 25 MSPS), `mode=2` (closed-loop echo sampling `dacr_d`/`dacr_clk` delayed by `ECHO_DELAY_DAC_CYC = 250` @ DAC clock, upconverted to `120 MHz` IF + noise, `no_echo_mut` fault control)
AD9253 Dual 14-bit SDR ADC	**`sim/models/ad9253_sdr_model.v`**	`sim_ad9253_model`: 3-wire SPI (Chip ID `0x8F`), coherent `6.25 MHz` (Ch A) + `12.5 MHz` (Ch B) @ `50.0` / `62.5 MSPS` (1-lane 16b DDR, `DCO = 400`/`500 MHz`), `lvds_skew.py` skew (`ADCS_D0 -8 ps`, `ADCS_D1 -34 ps`, `ADCS_FCO -18 ps` vs DCO) with `25 ps` transport margin
8x ADAR1000 SPI Array	**`sim/models/adar1000_array_model.v`**	`sim_adar1000_array`: 8 independent slaves on `adar_csb[7:0]`, 24-bit SPI read/write + `tx_load`/`rx_load` active latching, real-time `tr_viol` monitor
AD9708 & AD9767 DAC Monitors	**`sim/models/dac_monitor_models.v`**	`sim_dac_radar_mon` (AD9708 setup `>=2.0 ns`, hold `>=1.5 ns`, LFM chirp zero-crossing slope check) and `sim_dac_sdr_mon` (AD9767 `IQWRT`/`IQCLK`/`IQSEL` 14-bit I/Q quadrature capture)
Housekeeping I2C Slaves	**`sim/models/hk_i2c_periph_models.v`**	`sim_hk_i2c_slave`: open-drain I2C slaves for TMP1075 (`0x48`, `0x2A80`), CAT24C02 EEPROM (`0x50`), and Si549 XO (`0x55`)

Component / Model	File	Modeled Behavior
SGMII PHY + PS GEM3 Peer	`sim/models/sgmii_phy_kria_peer.v`	Behavioral RTL8211FSI + GEM3 peer: `K28.5` comma-pair CDR lock (`ui_tick <= 2'd3` 2-tick = `400..600 ps` UI-center sampling) with 4-error auto-relock, MDIO, UDP/IPv4/ARP TX/RX, and packet sequence scoreboard (`seen_eth_s1`, `seen_eth_s2`)

Simulation Speed Scaling

To complete all six multi-domain scenarios in ~6 minutes of batch XSim while running both eye-scan FSMs at their true hardware-default `TAP_DWELL_CYCLES = 1800` (no dwell `defparam`), **`tb_system.v`** overrides only slow housekeeping/MDIO/watchdog timers via `defparam`:

Parameter	Simulation Value	Hardware Role / Comment
`ETH_ALIVE_TIMEOUT`	`25000`	`200 us` watchdog window (vs `1 s` hw)
`HK_POLL_DIV`	`16000`	Accelerated housekeeping I2C poll period
`XO_FCAL_WAIT_CYC`	`150`	Accelerated Si549 XO FCAL wait
`ETH_MDIO_POLL_DIV`	`1200`	Accelerated MDIO status poll divider

RTL Bugs Caught & Fixed During Co-Simulation

1. **`kria_pl_link` async FIFO reset sensitivity & downlink unpack width (`fpga/kria/kria_pl_link.v`):**
2. `kria_pl_async_fifo` originally used synchronous-only `@(posedge wr_clk)` / `@(posedge rd_clk)` resets and uninitialized pointer/synchronizer registers, and `pcs_rst_rx` lacked an initial value. Added async reset sensitivity (`or posedge wr_rst` / `or posedge rd_rst`) and deterministic `= 0` / `= 1'b1` initial values.
3. `u_fifo_dl` / `dl_fifo_rd_data` had a width mismatch (`130` bits declared vs `122` bits packed: `2` sop/eop + `8` stream_id + `16` len + `32` seq + `64` data), leaving the upper control/ID MSBs `X/0`. Aligned to `122` bits and sliced `[121:0]`.
4. **Mid-run Ethernet peer silence detection (`fpga/artix/top.v`):**
5. `eth_path_ok` previously ignored `eth_remote_alive_stat`, so cutting the peer RX link or stopping peer keepalives did not degrade `eth_healthy` after `ETH_ALIVE_TIMEOUT`. Added `eth_seen_remote_alive` in the `link_clk` domain so `eth_path_ok = eth_link_up_stat & ~ctrl_force_eth_fault & (eth_remote_alive_stat | ~eth_seen_remote_alive)`, allowing initial AN/bring-up before the first peer frame while triggering deterministic failover on mid-run loss.
6. **Mid-packet arbitration & abort drain in `dual_path_mux` (`fpga/artix/dual_path_mux.v`):**
7. When `eth_healthy` dropped during `POL_SPLIT` while `eth_in_lock == 2'd2` (packet `s1` already mid-transfer into `u_fifo_eth`), `ias_in_sel` could latch `s1` mid-packet (`s1_sop == 0`), injecting a headless (`out_sop == 0`) fragment into `u_fifo_ias` that stalled `link_framer`. Added `s0_avail_*` / `s1_avail_*` SOP gating, cross-port lock exclusion (`eth_in_lock` / `ias_in_lock`), and `drop_s0` / `drop_s1` drain on FIFO abort.
8. **Bidirectional uplink idle/AM training gate & MDIO edge/free-run cleanup (`fpga/artix/top.v`, `fpga/artix/eth_mdio.v`, `fpga/artix/xc7a50t.xdc`):**
9. `u_ul_pcs_tx` is now gated (`ul_tx_allow = dl_up_sync[1] & dl_rem_sync2[0]` with packet-boundary `ul_in_pkt` hold) so only `/I/` + `/A/` training blocks are transmitted whenever either direction is unlocked, allowing Kria uplink eye training (`u_kria.train_cnt_l0/l1`) and S6 retrain to lock cleanly with live front-end traffic active from `t = 0`.
10. `eth_mdio.v` now stops `eth_mdc` low (`ST_IDLE`) between 1 ms status polls and reduces IOBUF drive to `4 mA`, paired with `SLEW SLOW` and `DRIVE 4` in **`artix/xc7a50t.xdc`**.

Verification Results (Vivado XSim 2026.1)

Post-Rev08 Phase 1 (A-1..A-4 & G-1) verification ran directly against the final RTL in Vivado XSim 2026.1:

Baseline Full-System Passes (`tb_system`, `500 MHz` and `400 MHz`, Hardware `TAP_DWELL_CYCLES = 1800`, `t = 0` Live Streaming)

- **Default `500 MHz` Si549 mode:** `.\fpga\sim\run.ps1 tb_system` -> **Exit code `0`**, elapsed **`453.23 s`** (**`tb_system.log`**)
- `[S1] PASS REG_LINK_STATUS=0x000100fd 0xE8=0x00000411 uart_resp=00000411 mdio_polls=8 dl_up=1 eth_up=1` (A-1: `adc_trained=0` in `500M` mode)
- `[S2] PASS AD9253=0x8F AD9484=0x6C TMP1075=0x2A80 PPS=1251(+800 ppm)`

- [S4] PASS rx04=4(max=12043) rx05=86(max=8000) dacs_i=35 dacs_q=35 (62.5 MSPS AD9253)
- [SW] PASS 500->400 switch OK 0xE8=0x00460436 drop=2398 ddc_en=1 cap_rst=0 ddc_rst=0
- [S3] PASS chirp zc1=18->zc2=34 echo_snr=152.7x cw_img_rej=60.4 dB
- [S5] PASS -100ppm MIRROR_1P1 + mid-run ETH/IAS1 cuts lost_s1=0 lost_s2=0 mdio_wrs=1
- [S6] PASS glitch->crc_err->clear->retrain(drop=1,up=1,post_crc=0)
- [S7] PASS TX_KEY 0x38 keys dsp_tx_en; DSP_CTRL[1] is RO
- PASS: tb_system full-system verification (S1..S7, +/-100 ppm, Rev05 SI, ETH+IAS1, TX_KEY) passed
- **400 MHz Si549 mode:** .\fpga\sim\run.ps1 tb_system -Define FPGA_CLK_400M -> **Exit code 0**, elapsed **516.44 s** (**tb_system-def-FPGA_CLK_400M.log**)
- [S1] PASS REG_LINK_STATUS=0x003500fd 0xE8=0x00460436 uart_resp=00460436 mdio_polls=7 dl_up=1 eth_up=1
- [S2] PASS AD9253=0x8F AD9484=0x6C TMP1075=0x2A80 PPS=1251(+800 ppm)
- [S3] PASS chirp zc1=18->zc2=34 echo_snr=201.0x cw_img_rej=67.7 dB
- [S4] PASS rx04=5(max=8579) rx05=80(max=7999) dacs_i=32 dacs_q=31 (50.0 MSPS AD9253)
- [S5] PASS -100ppm MIRROR_1P1 + mid-run ETH/IAS1 cuts lost_s1=0 lost_s2=0 mdio_wrs=1
- [S6] PASS glitch->crc_err->clear->retrain(drop=1,up=1,post_crc=0)
- [S7] PASS TX_KEY 0x38 keys dsp_tx_en; DSP_CTRL[1] is RO
- PASS: tb_system full-system verification (S1..S7, +/-100 ppm, Rev05 SI, ETH+IAS1, TX_KEY) passed

Dual-Frequency, Debug UART & Module Testbench Suite (500 MHz + 400 MHz)

- **All 19 unit/module testbenches passed at both 500 MHz (default) and 400 MHz (-Define FPGA_CLK_400M)**, with all artix_top-instantiating benches (tb_dbg_uart, tb_artix_top, tb_clk_mode_switch, tb_e2e, tb_rev06, tb_system) and the 13 standalone submodule benches (tb_adar_ctrl, tb_adcs_capture, tb_adc_ddc, tb_dac_tx, tb_hk, tb_link_a2k, tb_link_axis, tb_link_k2a, tb_pcs_loop, tb_pcs_unit, tb_pmod_spi, tb_serdes7, tb_serdes_us) verified at both frequencies.
- **tb_dbg_uart (G-1):** Verified boot banner, periodic STAT, r/w/s/h CLI, 4-master CSR arbitration, and BREAK framing error recovery (500 MHz & 400 MHz exit 0). Negative mutations -Mutate wrong_divisor (exit 1, ferr=72) and -Mutate drop_monitor_write (exit 1, stale 'r e4' readback 00000001) both failed as designed.
- **Negative mutation (tb_clk_mode_switch):** .\fpga\sim\run.ps1 tb_clk_mode_switch -Mutate no_delta_clamp -> exit 1 as expected when the ±50 ppm Si549 ADPLL_DELTA_M Ethernet clamp was disabled.

Negative Mutation Runs (tb_system -Mutate)

Earlier Part A baseline mutations (bad_channel_skew exit 1 in 306.53 s, no_echo_return exit 1 in 270.72 s, eth_skip_fcs exit 1 in 261.98 s, no_retrain exit 1 in 287.13 s) validated tb_system fault sensitivity. The TX_KEY interlock mutation tx_key_from_dsp_ctrl fails at S7 (FAIL @ 173368788500 ps: S7: DSP_CTRL[1] keyed the transmitter, exit 1).

Explicit Verification Limits

1. **Behavioral peripheral & analog/PHY models:** u_ad9484, u_ad9253, u_adar1000, u_dacr_mon, u_dacs_mon, sim_hk_i2c_slave, sgmii_phy_kria_peer, and sim_board_lvds_channel are Verilog behavioral models approximating datasheet protocols, lvds_skew.py static delays, and SIGNAL_INTEGRITY.md jitter/noise budgets, not SPICE/IBIS full-wave SI or silicon converter models.
2. **PS firmware & Linux stack excluded:** tb_system drives kria_pl_link AXI4-Lite/AXIS ports directly via testbench BFMs rather than executing ARM Zynq PS C code, Linux DMA drivers, or GEM3 MAC microcode.
3. **Scaled timers & watchdog intervals:** Simulation speed-up overrides compress housekeeping polling, Si549 FCAL wait, MDIO polling, and ETH_ALIVE_TIMEOUT (200 us vs 1 s hardware); TAP_DWELL_CYCLES runs at hardware default (1800).
4. **XSim UltraScale+ primitive advisory:** Vivado XSim 2026.1 emits [Unisim IDELAYE3-1] advisories on u_kria.u_idelay_d0/d1 noting behavioral reset limitations when DELAY_FORMAT = TIME.
5. **Vivado 2026.1 implementation signoff refreshed (with post-route phys_opt_design): artix/build.tcl, artix/build_rev06.tcl** (ENABLE_ETH=1), **kria/build.tcl**, and **kria/bd.tcl** were synthesized, placed, routed, and post-route optimized in Vivado 2026.1 against the updated RTL, refreshing **artix/reports/**, **artix/reports_rev06/**, **kria/reports/**, and kria/out/ (ias2rf_k26.bit, ias2rf_k26.xsa) with 0 DRC errors and all timing constraints met:
6. **artix_top (build_rev06.tcl -> reports_rev06/) and ias2rf_k26_bd_wrapper (bd.tcl -> kria/reports/):** utilisation and slack of the current builds in the generated **FPGA figures** table.

Source: fpga/link/LINK_PROTOCOL.md

IAS1-to-RF LVDS Link Protocol & PCS Specification

Scope: Line coding, scrambling, gearbox, framing, 2-lane striping/deskew, training state machine, packet format, and register map for the bidirectional AC-coupled LVDS link between the Artix-7 RF/DAQ FPGA (`XC7A50T-FTG256`) and Kria K26 (`XCK26-SFVC784`).

1. Physical & PCS Layering

Direction	Data Lanes	Clock Pair	Raw Rate / Lane (Nom.)	Aggregate Raw Rate	Net 64b/66b Rate	SERDES Width	Parallel Clock (CLKDIV)
Uplink (Artix -> Kria)	2 (`LINK_RX_D0`, `LINK_RX_D1`)	`LINK_RX_CLK` (500 MHz DDR)	1.0 Gb/s	**2.0 Gb/s**	1.939 Gb/s	8-bit DDR	125 MHz
Downlink (Kria -> Artix)	1 (`LINK_TX_D0`)	`LINK_TX_CLK` (500 MHz DDR)	1.0 Gb/s	**1.0 Gb/s**	0.970 Gb/s	8-bit DDR	125 MHz

- **Rate scaling (`link-decisions.md` #6):** All PCS and SERDES RTL is clock-rate agnostic; `400 MHz DDR` (`800 Mb/s/lane`, `CLKDIV = 100 MHz`) and `500 MHz DDR` (`1.0 Gb/s/lane`, `CLKDIV = 125 MHz`, nominal operating point) run on the exact same gateware.
- **Forwarded clock (`link-decisions.md` #8):** Edge-aligned source-synchronous forwarding driven by an `OSERDES` lane transmitting constant `8'b1010_1010` (`10101010` LSB-first = `0,1,0,1,0,1,0,1` on wire) from the same serial/parallel clocks as the data lanes. Each receiver independently centers the sampling eye with `IDELAY`.
- **Bit ordering on wire (LSB-first):** Within each parallel SERDES byte `tx_byte[7:0]`, bit `0` (`tx_byte[0]`) is transmitted first in time and bit `7` (`tx_byte[7]`) last. Within each 66-bit block `blk[65:0]`, `sync[1:0] = blk[1:0]` is transmitted first (`blk[0]` then `blk[1]`), followed by payload bits `blk[2]` through `blk[65]`.
- **AC-coupling DC balance:** All `LINK_*` pairs are AC-coupled through 100 nF series capacitors (`C101`–`C110`). IEEE 802.3 Clause 49 self-synchronous scrambling bounds continuous run length and keeps DC baseline wander within the 100 nF + 100 Ω (`τ = 10 µs` high-pass) time constant.

2. 64b/66b Block Format

Each 66-bit block on a physical lane is formed as `{payload[63:0], sync[1:0]}`:

`sync[1:0]`	Class	`btype = payload[7:0]`	Symbol	Unscrambled `payload[63:0]` Layout (MSB..LSB)	Purpose
`2'b01`	**Data**	*(all 64 bits)*	`/D/`	`data[63:0]`	64-bit packet timestamp or payload word
`2'b10`	**Control**	`8'h1E`	`/I/` (`BTYPE_IDLE`)	`{40'h0, remote_status[15:0], 8'h1E}`	Idle / training fill block & link health feedback
`2'b10`	**Control**	`8'h4B`	`/A/` (`BTYPE_ALIGN`)	`{32'h9A_C5_3C_69, am_seq[15:0], lane_id[7:0], 8'h4B}`	Periodic 2-lane Alignment Marker (`AM_PERIOD` blocks)
`2'b10`	**Control**	`8'h78`	`/S/` (`BTYPE_START`)	`{seq_num[31:0], pkt_len[15:0], stream_id[7:0], 8'h78}`	Start of Packet header
`2'b10`	**Control**	`8'hFF`	`/T/` (`BTYPE_TERM`)	`{dropped_cnt[23:0], crc32[31:0], 8'hFF}`	End of Packet trailer (IEEE CRC-32 + drop count)
`2'b10`	**Control**	`8'h55`	`/C/` (`BTYPE_CTRL`)	`{ctrl_arg[39:0], ctrl_op[15:0], 8'h55}`	Low-latency single-block ordered command (optional)
`2'b00`, `2'b11`	**Invalid**	n/a	n/a	*(Never transmitted)*	Invalid sync header; triggers Clause 49 error / slip

- **Idle fill during bring-up:** While the link is training (`ST_EYE_SCAN`, `ST_BLOCK_LOCK`, `ST_DESKEW`), TX transmits continuous scrambled `/I/` blocks (with `/A/` every `AM_PERIOD` blocks per lane). Scrambled `/I/` guarantees >200 Mb/s transition density for Kria `IDELAYE3` eye scanning and safe AC-coupled baseline.

3. Scrambler & Descrambler (IEEE 802.3 Clause 49)

- **Polynomial:** $G(x) = 1 + x^{39} + x^{58}$ (58-bit LFSR `scr[57:0]`, reset seed `58'h3FF_FFFF_FFFF_FFFF`).

- **Scope:** `sync[1:0]` (`blk[1:0]`) bypasses the scrambler **unmodified**; only `payload[63:0]` (`blk[65:2]`) is scrambled/descrambled sequentially from bit `0` to bit `63`.
- **Per-bit equations (`i = 0 .. 63`):**
- **TX Scrambler:** `s_bit = payload_in[i] ^ scr[38] ^ scr[57]` `scr = {scr[56:0], s_bit}`
- **RX Descrambler (self-synchronous):** `d_bit = payload_rx[i] ^ scr[38] ^ scr[57]` `scr = {scr[56:0], payload_rx[i]}`
- Because the RX descrambler shifts in the received ciphertext bit `payload_rx[i]`, it automatically synchronizes to the TX scrambler state within **58 received bits** (one 64-bit block) with zero handshake, and each isolated single-bit channel error multiplies into at most 3 bit errors in the descrambled block (`x`, `x+39`, `x+58`), which CRC-32 catches deterministically.

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4. 66:8 / 8:66 Gearboxes & Block Lock FSM

4.1 Gearbox Framing

- At 8 bits per `CLKDIV` (125 MHz @ 1.0 Gb/s nominal), **33 `CLKDIV` cycles = 264 bits = 4 x 66-bit blocks**.
- `link_gearbox_tx` accepts a new 66-bit block via `in_ready` on cycles where internal accumulator occupancy `bit_cnt <= 65` (4 cycles out of every 33). If `in_valid` is low when `in_ready` asserts, an Idle block `{64'h0000_0000_0000_001E, 2'b10}` is substituted automatically after scrambling.
- `link_gearbox_rx` appends 8 bits per `CLKDIV` cycle into a 140-bit shift accumulator and asserts `out_valid` whenever `>= 66` bits are available (4 cycles out of every 33). When `rx_slip` is pulsed for one cycle, 1 bit is discarded from the accumulator head, advancing the 66-bit extraction window by 1 bit time (1 UI = 1.0 ns @ 1.0 Gb/s). This unifies both intra-byte bit alignment (`0..7`) and block boundary alignment (`0..65`) inside plain Verilog-2001 logic.

4.2 Clause 49.2.13 Block Lock State Machine (`link_block_lock`)

- **Valid sync header check:** `sh_valid = (rx_sync == 2'b01) || (rx_sync == 2'b10)`.
- **Unlocked (`block_lock == 0`):**
- Every `sh_valid` increments `sh_cnt`. Reaching **64 consecutive valid sync headers** transitions to `block_lock = 1`.
- Any invalid sync header (`2'b00` or `2'b11`) resets `sh_cnt = 0`, increments `sh_err_cnt`, and pulses `rx_slip = 1` (with a 1-block pipeline settle holdoff before checking the next header).
- **Locked (`block_lock == 1`):**
- Evaluates sliding windows of 64 received blocks (`win_cnt = 0..63`, `sh_invalid_cnt`).
- Every invalid sync header increments `sh_invalid_cnt` and `sh_err_cnt`.
- If **`sh_invalid_cnt == 16`** within a 64-block window, `block_lock` drops to `0`, `rx_slip` pulses, and acquisition restarts. Otherwise at `win_cnt == 63`, `win_cnt` and `sh_invalid_cnt` clear.

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5. 2-Lane Striping & Alignment-Marker Deskew

Applies to the 2-lane uplink (`LINK_RX_D0`, `LINK_RX_D1`). (For 1-lane downlink `LINK_TX_D0`, Lane 0 passes directly without striping.)

1. **TX Striping (`link_tx_lanes`):**
2. Distributes unscrambled packet/idle blocks strictly alternating **Lane 0 (even)**, then **Lane 1 (odd)**.
3. Every `AM_PERIOD` block-pairs per lane (default `16384 = 2^14` in synthesis ≈ 10.8 ms interval; parameterizable e.g. `64` in simulation), pauses user `in_ready` for two lane emissions and injects `BTYPE_ALIGN` (`8'h4B`, magic `32'h9A_C5_3C_69`, shared `am_seq[15:0]`, `lane_id = 0 / 1`) simultaneously onto both lanes.
4. **RX Deskew (`link_rx_lanes`):**
5. After `l0_block_lock && l1_block_lock`, each lane writes descrambled 66-bit blocks into an independent 32-entry circular elastic FIFO (capable of absorbing up to ±15 blocks = ±990 UI of static + dynamic inter-lane skew).
6. Both FIFOs watch for `sync == 2'b10 && data[7:0] == 8'h4B && data[63:32] == 32'h9A_C5_3C_69` (`BTYPE_ALIGN`) and record the write index at which matching `am_seq[15:0]` arrived on Lane 0 and Lane 1.
7. Read pointers `rp0` and `rp1` are initialized cleanly just past the matched AM entry on both lanes, asserting `deskew_lock = 1` and reporting `skew_blocks = wp0_am - wp1_am`.
8. `BTYPE_ALIGN` and `BTYPE_IDLE` control blocks are stripped cleanly during readout, reconstructing the exact single-stream order (Lane 0 even block, then Lane 1 odd block) for `link_deframer`.

6. Packet Format & AERIS Radar Stream Mapping

6.1 Wire Packet Structure

Every packet transfers between **1 and 4096 payload bytes** framed as a contiguous sequence of `N + 3` blocks (`N = ceil(pkt_len / 8)`):

Order	Block Type	sync[1:0]	payload[63:0] Fields
0	**START (/S/)**	2'b10	[7:0] = 8'h78, [15:8] = stream_id[7:0], [31:16] = pkt_len[15:0], [63:32] = seq_num[31:0]
1	**TIMESTAMP**	2'b01	[63:0] = pps_timestamp_ns[63:0] (PPS-disciplined monotonic timestamp)
2 .. N+1	**DATA (/D/)**	2'b01	data_word[63:0] (little-endian byte packed; unused trailing bytes in word N+1 zero-padded)
N+2	**TERM (/T/)**	2'b10	[7:0] = 8'hFF, [39:8] = crc32[31:0], [63:40] = dropped_cnt[23:0]

- **Header constraints:** `1 <= pkt_len <= 4096`. `seq_num[31:0]` increments per packet/chirp per stream so upper layers can also cross-check sequence continuity.
- **Dropped packet counter (`dropped_cnt[23:0]`):** TX-side saturating counter incremented whenever the upstream radar FIFO overflows or rejects a frame; piggybacked in every `/T/` trailer so Kria PS/PL observes upstream losses even if whole packets never entered the link.
- **IEEE 802.3 CRC-32:** Polynomial `0x04C11DB7` (reflected `0xEDB88320`), initial seed `0xFFFFFFFF`, final XOR `0xFFFFFFFF`. Computed LSB-first over the **complete 64-bit `START` word**, the **64-bit `TIMESTAMP` word**, and all **`N` 64-bit `DATA` words** (all `8*N` bytes, with unused trailing bytes in the final word `= 8'h00`).
- **Receiver validation (`link_deframer`):** Buffers or tags incoming packet words and checks `crc32` upon receiving `/T/` plus `1 <= pkt_len <= 4096`. Only asserts `pkt_done_ok` if CRC matches and protocol framing is intact; otherwise asserts `pkt_done_err` and increments `crc_err_cnt`.
- **Intentional error-injection self-test in simulation (`PASS` lines with non-zero `crc_err`):** Normal clean runs of the verification testbenches deliberately inject single-bit channel errors on designated packets to confirm end-to-end CRC-32 error detection and packet rejection (`pkt_done_err` + `crc_err_cnt`):
- `tb_pcs_loop`: deliberately injects bit errors into `3` packets (`p == 5, 13, 21` -> expects **`crc_err=3`**, `rx_good=25` out of `28`, `0` payload mismatches).
- `tb_link_a2k` and `tb_link_k2a`: each deliberately inject a bit error into `1` packet (`p == 7` -> expects **`crc_err=1`**, `rx_good=19` out of `20`, `0` payload mismatches). In all benches, a non-zero `crc_err` matching the exact injected packet count is required for `PASS`; a `0` `crc_err_cnt` causes the run (or the `skip_crc` mutation) to `FAIL`.

6.2 Radar Stream IDs (Aligned with AERIS `radar_protocol.py` Semantics)

Rather than tunneling AERIS's legacy 11-byte (`0xAA .. 0x55`) UART/FTDI USB records verbatim, packets use native 64-bit-aligned bursts tagged by `stream_id[7:0]`:

stream_id	Direction	Payload Contents (Reference: AERIS radar_protocol.py)	Typical pkt_len
8'h01	Artix -> Kria	Raw DDC / ADC I/Q chirp samples (interleaved `int16 I, int16 Q` per chirp; `seq_num = chirp_id`). With `RADAR_CTRL[3]` set, `I[0]` is a CPI mark: 1 on the first sample of every 16th chirp, 0 elsewhere (Rev08 G-8)	512 .. 4096 B
8'h02	Artix -> Kria	Pre-processed range profile / CFAR vector (or `int16` range FFT bins)	256 .. 1024 B
8'h03	Artix -> Kria	Range-Doppler cell tiles (each 9 B AERIS cell `{range_q[15:0], range_i[15:0], dop_re[15:0], dop_im[15:0], det[7:0]}` packed into 12 B or 16 B records, up to 4096 B)	<= 4096 B
8'h10	Kria -> Artix	Host register write command matching `radar_protocol.Opcode` (`{opcode[7:0], addr[7:0], value[15:0]}` for radar mode `0x01`, trigger `0x02`, CFAR `0x21–0x27`, AGC `0x28–0x2C`, chirp timings `0x10–0x16`, status request `0xFF`)	4 .. 16 B
8'h11	Artix -> Kria	Telemetry / `StatusResponse` snapshot (6 x 32-bit status words: mode, stream_ctrl, threshold, chirp timings, AGC gain, self-test flags)	24 .. 64 B
8'h7F	Both	PRBS / loopback diagnostic burst for link bring-up and BER verification	8 .. 4096 B

The ids `8'h20` to `8'h23` never cross the link: they are the Kria PL's own results to its PS (audio, ADS-B, radar detections and maps from `kria_dsp_out`), merged with the link's uplink packets by `kria_ps_framer` into DMA blocks with their own header

word (**FPGA_GATEWARE.md §5.10**).

7. Hardware Training FSM & Register Map

7.1 Hardware Training FSM (`link_rx_train_fsm`)

The receiver training FSM (`link_rx_train_fsm`) supports both receivers via parameterization:

- **Kria K26 Uplink RX (`Bank 66 HP`, 2 lanes):** `IDELAYE3` TIME mode with `VAR_LOAD = TRUE` (512 fine taps @ 4 ps/tap in XSim `ULTRASCALE_PLUS` behavioral simulation; requires `EN_VTC = 0` during `LOAD` and `>= 4` `CLK` cycles after `RST` deassertion per UG571). Sweeps `CNTVALUEIN` across `[0 .. 511]`.
- **Artix-7 Downlink RX (`Bank 14 HR`, 1 lane):** `IDELAYE2` `VAR_LOAD` mode (`REFCLK_FREQUENCY = 200.0`, 32 taps @ 78 ps/tap + 600 ps intrinsic in XSim `7SERIES`). Sweeps `CNTVALUEIN` across `[0 .. 31]`, bypassing multi-lane deskew (`SINGLE_LANE = 1`).

State	Code	Action	Exit Condition
`ST_RESET`	`3'd0`	Hold `en_vtc = 0`; wait `>= 16` `CLKDIV` cycles after `rst == 0` so `IDELAY` reset synchronizer settles	Wait timer expired
`ST_EYE_SCAN`	`3'd1`	If `cfg_tap_override`, jump to load override; else sweep `CNTVALUEIN` from `0` to `MAX_TAP` (step `TAP_STEP`), allowing `link_block_lock` to align on entry into an eye and checking that descrambled blocks are error-free `/I/` (`8'h1E`) or `/A/` (`8'h4B`) training blocks (`l*_rx_blk_ok`); track the full passing tap window `[eye_left .. eye_right]` per lane	Full sweep complete
`ST_LOAD_OPT`	`3'd2`	Compute midpoint `(eye_left + eye_right) >> 1` per active lane and issue a 1-cycle `LOAD` pulse with `en_vtc = 0`	Optimal center tap loaded
`ST_BLOCK_LOCK`	`3'd3`	Wait for Clause 49 `l0_block_lock` (and `l1_block_lock` when `SINGLE_LANE == 0`) while `IDELAY` settles	Active lane(s) locked (or timeout -> re-scan)
`ST_DESKEW`	`3'd4`	Enable `link_rx_lanes` AM deskew across Lane 0 and Lane 1 (bypassed when `SINGLE_LANE == 1`)	`deskew_lock == 1` (or timeout -> restart)
`ST_LINK_UP`	`3'd5`	Assert `link_up = 1` (optional `en_vtc = 1` once BISC/VTC policy allows); monitor loss of `block_lock` or `deskew_lock`	Drops to `ST_BLOCK_LOCK` / `ST_DESKEW` if lock lost

Bidirectional Idle/AM Training Gate (`artix/top.v`): Because `link_rx_train_fsm` requires 6 consecutive clean descrambled `/I/` (`8'h1E`) or `/A/` (`8'h4B`) training blocks per `IDELAY` tap, **`artix_top`** holds `u_ul_pcs_tx.pkt_valid` low (transmitting continuous scrambled `/I/` + `/A/` markers only) until both directions are synchronized (`ul_tx_allow = dl_up_sync[1] & dl_rem_sync2[0]`, where `dl_rem_sync2[0]` reflects Kria's `link_up` fed back via downlink `/I/` `remote_status[0]`). On link drop or manual retrain (`ul_tx_allow -> 0`), `artix_top` lets any single in-flight packet finish cleanly on `ias_mux_eop` (`ul_in_pkt`) before stalling further `/S/` starts and returning the uplink to continuous `/I/` + `/A/` until `link_up` recovers.

7.2 Control & Diagnostic Register Map (Both Ends)

Offset	Register	Access	Reset	Fields & Description
`0x00`	`LINK_CTRL`	R/W	`0x0000_0000`	`[0]` Soft Reset; `[1]` Loopback Enable; `[2]` Retrain Pulse (self-clearing); `[3]` `tap_override_en` (use `IDELAY_CTRL_L0/L1`); `[4]` `prbs7_tx_en` (bypass framer with PRBS-7 test pattern); `[5]` `prbs7_rx_chk_en`; `[6]` Clear Error Counters (W1C pulse)
`0x04`	`LINK_STATUS`	RO	`0x0000_0000`	`[2:0]` `train_state`; `[3]` `l0_block_lock`; `[4]` `l1_block_lock`; `[5]` `deskew_lock`; `[6]` `link_up`; `[7]` `idelayctrl_rdy`; `[23:16]` `remote_status[7:0]` (from `/I/`)
`0x08`	`IDELAY_CTRL_L0`	R/W	`0x0000_0000`	`[8:0]` Software `CNTVALUEIN` override for Lane 0 (`0..511`); `[24:16]` Readback active tap loaded on Lane 0; `[31]` Force `LOAD`
`0x0C`	`IDELAY_CTRL_L1`	R/W	`0x0000_0000`	`[8:0]` Software `CNTVALUEIN` override for Lane 1 (`0..511`); `[24:16]` Readback active tap loaded on Lane 1; `[31]` Force `LOAD`
`0x10`	`ERR_CNT_SH_L0`	RO	`0x0000_0000`	`[31:0]` Saturating invalid sync-header error count on Lane 0
`0x14`	`ERR_CNT_SH_L1`	RO	`0x0000_0000`	`[31:0]` Saturating invalid sync-header error count on Lane 1
`0x18`	`ERR_CNT_CRC`	RO	`0x0000_0000`	`[31:0]` Saturating deframer CRC-32 error packet count
`0x1C`	`PKT_CNT_RX`	RO	`0x0000_0000`	`[31:0]` Valid packets received (`pkt_done_ok`)
`0x20`	`PKT_CNT_DROP`	RO	`0x0000_0000`	`[23:0]` Latest TX `dropped_cnt` reported in `/T/` trailer; `[31:24]` RX FIFO overflow drops

Offset	Register	Access	Reset	Fields & Description
0x24	DESKEW_STATUS	RO	0x0000_0000	[7:0] Signed measured inter-lane skew (skew_blocks); [23:8] Last matched am_seq[15:0]
0x28	PRBS_ERR_CNT	RO	0x0000_0000	[31:0] Saturating bit-error counter when prbs7_rx_chk_en == 1
0x2C	EYE_SCAN_L0	RO	0x0000_0000	[8:0] Discovered eye-left tap; [24:16] Discovered eye-right tap (Lane 0)
0x30	EYE_SCAN_L1	RO	0x0000_0000	[8:0] Discovered eye-left tap; [24:16] Discovered eye-right tap (Lane 1)
0x34	ADCS_CTRL	R/W	0x0000_0009	**AD9253 + DDC:** [0] adcs_enable; [1] conv_spi_start_init (W1P); [3:2] sdr_ddc_ch_enable ([2]=ChA, [3]=ChB, default ChB=1 on IF_RX_C J951 for switch-free HF)
0x38	ADCS_STATUS	RO	0x0000_0000	[0] aligned; [1] idelay_done; [2] idelay_err; [3] bitslip_err; [8:4] best_tap; [16] conv_init_done; [17] conv_init_err; [31:24] ad9253_id
0x3C	CONV_SPI_CMD	R/W	0x0000_0000	[7:0] req_wdata; [20:8] req_addr[12:0]; [21] req_rw (0=W,1=R); [22] req_target (0=AD9484,1=AD9253); [31] Start (W1P)
0x40	CONV_SPI_RDATA	RO	0x0000_0000	[7:0] resp_rdata; [8] resp_valid_sticky; [9] req_ready
0x44	SDR_DDC_NCO_A	R/W	0x0000_0000	[31:0] SDR DDC Ch A NCO frequency tuning word (nco_ftw_a)
0x48	SDR_DDC_NCO_B	R/W	0x0000_0000	[31:0] SDR DDC Ch B NCO frequency tuning word (nco_ftw_b)
0x4C	SDR_DDC_DECIM	R/W	0x0040_0004	[15:0] decim_ratio (>=2, even >=4 enables HB FIR); [25:16] words_per_pkt (default 64 = 512 B)
0x50	SDR_DDC_DROP	RO	0x0000_0000	[23:0] Saturating sdr_ddc.dropped_cnt across async CDC FIFO
0x54	DACR_CTRL	R/W	0x00FF_0000	**AD9708 + AD9767:** [0] chirp_enable; [1] chirp_trig (W1P); [23:16] amp_scale[7:0] (0xFF = full scale)
0x58	DACR_F0_FTW	R/W	0x0000_0000	[31:0] AD9708 radar chirp start FTW (f0_ftw)
0x5C	DACR_DF_FTW	R/W	0x0000_0000	[31:0] Signed AD9708 chirp slope step per clock (df_ftw)
0x60	DACR_PULSE_LEN	R/W	0x0000_0400	[31:0] Radar chirp duration in dac_clk cycles (pulse_len)
0x64	DACR_PRI_LEN	R/W	0x0000_2000	[31:0] Radar PRI in dac_clk cycles (0 = trigger-only single shot)
0x68	DACR_STATUS	RO	0x0000_0000	[0] chirp_active
0x6C	DACR_PULSE_CNT	RO	0x0000_0000	[31:0] Total radar chirps transmitted (pulse_cnt)
0x70	DACS_CTRL	R/W	0x0000_0000	[0] AD9767 tx_enable; [1] ~hf_dac2_mode (0=switch-free HF primary I on DAC2 / IF_TX_C J952, 1=legacy Ch1/Ch2 I/Q); [2] dac1_mute (1=clamp DAC1 to midscale 14'h2000 when hf_dac2_mode=1)
0x74	DACS_UNDERFLOW	RO	0x0000_0000	[31:0] AD9767 underflow_cnt
0x78	DACS_FIFO_LVL	RO	0x0000_0000	[9:0] dac_sdr.fifo_level_link
0x7C	ADAR_CTRL	R/W	0x0000_0000	**ADAR1000 + RF SW:** [4:0] active_beam_id; [5] tr_req (0=RX,1=TX); [6] soft_load (W1P); [7] start_init (W1P); [11:8] rf_sw_req[3:0]; [12] auto_tr_chirp (drive tr_req from chirp_active); [13] scan_en (Rev08: each BEAM_STROBE loads the next of beams 0..scan_last, starting at 0 whenever scan_en is set; soft_load still loads active_beam_id); [20:16] scan_last
0x80	ADAR_GUARD	R/W	0x000C_000A	[15:0] guard_pre cycles; [31:16] guard_post cycles
0x84	ADAR_SW_SETTLE	R/W	0x0000_007D	[15:0] rf_switch.settle_cycles (default 125 = 1 us @ 125 MHz)
0x88	ADAR_TBL_WR	WO	0x0000_0000	[7:0] tbl_wdata; [12:8] byte_idx (0..23); [15:13] chip_id (0..7); [20:16] beam_id (0..31); [31] Write strobe (W1P)
0x8C	ADAR_SPI_CMD	R/W	0x0000_0000	[7:0] wdata; [22:8] addr[14:0]; [23] rw; [26:24] chip_id; [31] Trigger (W1P)
0x90	ADAR_STATUS	RO	0x0000_0000	[0] init_done; [1] init_err; [2] load_busy; [3] tr_ready; [4] sw_ready; [9:5] current_beam_id; [17:10] spi_resp_rdata; [18] spi_req_ready; [22:19] sw_ctrl[3:0]
0x94	HK_I2C_CTRL	R/W	0x0000_0001	**HK + XO + XADC + PPS:** [0] poll_en (auto-poll TMP1075 7'h48 Reg 0x00)
0x98	HK_I2C_CMD	R/W	0x0000_0000	[6:0] dev_addr (0x48 TMP1075 / 0x50 M24C02); [9:7] wr_len (0..4); [11:10] rd_len (0..2); [31] Trigger (W1P)
0x9C	HK_I2C_WDATA	R/W	0x0000_0000	[31:0] Packed TX bytes ([7:0]=byte0 .. [31:24]=byte3)
0xA0	HK_I2C_STATUS	RO	0x0000_0000	[15:0] req_rdata; [16] req_ready; [17] last_ack_err; [18] busy; [19] alert_active (~HK_ALERT_N); [20] tmp_valid
0xA4	HK_TEMP_ERR	RO	0x0000_0000	[15:0] tmp_raw (TMP1075 [15:4]*0.0625 C); [31:16] ack_err_cnt

Offset	Register	Access	Reset	Fields & Description
0xA8	XO_CTRL	R/W	0x0000_0000	[0] use_ext_clk (CLK_SEL D8: 0=Si549 Z, 1=SMA 0); [1] prog_freq_500m (0=400MHz,1=500MHz, triggers safe clk_mode_ctrl MMCM DRP + Si549 switch); [2] prog_start (W1P); [3] delta_start (W1P); [8] xo_busy (RO); [9] xo_prog_done (RO); [10] xo_active_freq_500m (RO); [11] xo_ack_err (RO); [12] xo_boot_err (RO); [13] xo_delta_clamped (RO); [14] xo_boot_done (RO); [31:16] xo_ack_err_cnt (RO)
0xAC	XO_DELTA_M	R/W	0x0000_0000	Signed [23:0] Si549 ADPLL_DELTA_M (Regs 231..233); clamped to ±429553 (±50.0 ppm @ 0.0001164 ppm/LSB) when ENABLE_ETH=1 (unclamped ±950 ppm otherwise)
0xB0	XO_RAW_CMD	R/W	0x0000_0000	[7:0] reg_addr; [15:8] wdata; [16] rw (0=W,1=R); [23:17] I2C device address (0 = the Si549 at 0x55; 0x20/0x21 reach the TCA6416A expanders, Rev08 G-2); [31] Trigger (W1P)
0xB4	XO_RAW_RDATA	RO	0x0000_0000	[7:0] raw_resp_rdata; [8] raw_resp_valid_sticky; [9] raw_req_ready; [10] raw_resp_err
0xB8	XADC_TEMPV	RO	0x0000_0000	[11:0] xadc_temp_raw; [23:12] xadc_vccint_raw; [24] xadc_valid; [25] xadc_overtemp
0xBC	XADC_VCCAUX	RO	0x0000_0000	[11:0] xadc_vccaux_raw
0xC0	PPS_CTRL	R/W	0x0000_0800	[15:0] cfg_ts_step_q8 (default 0x0800 = 8.0 ns/clk); [16] cfg_pps_disc_en; [17] cfg_ts_clear (W1P); [24] pps_locked (RO)
0xC4	PPS_NOM_CYC	R/W	0x0773_5940	[31:0] cfg_nom_period_cyc (default 125,000,000 @ 125 MHz)
0xC8	PPS_PERIOD_CYC	RO	0x0000_0000	[31:0] Measured PPS period in adc_clk cycles
0xCC	PPS_PPM_ERR	RO	0x0000_0000	[31:0] Signed integer frequency offset (ppm) vs PPS_NOM_CYC
0xD0	PPS_CNT	RO	0x0000_0000	[31:0] Rising PPS_SYNC edge counter
0xD4	TS_NOW_LO	RO	0x0000_0000	[31:0] pps_timestamp_ns[31:0] snapshot (sys_clk)
0xD8	TS_NOW_HI	RO	0x0000_0000	[31:0] pps_timestamp_ns[63:32] snapshot (sys_clk)
0xDC	PPS_LATCH_LO	RO	0x0000_0000	[31:0] pps_latch_ts[31:0] captured on last PPS_SYNC edge
0xE0	PPS_LATCH_HI	RO	0x0000_0000	[31:0] pps_latch_ts[63:32] captured on last PPS_SYNC edge
0xE4	RADAR_CTRL	R/W	0x0000_0001	**Rev08 A-1/G-1**: [0] rad_ddc_en (replaces ~pmod_spare1); [1] W1P clear sticky clip/ovf flags & 0xEC counters
0xE8	RADAR_STATUS	RO	0x0000_0000	[0] radar_dis_by_clk_mode (1 at 500M); [1] adcr_mmcm_locked; [2] adc_trained; [3] dco_phase_err; [4] dl_link_up; [5] dl_up & adc_trained (replaces pmod_spare2); [6] adcr_or_sticky; [7] adcs_clip_sticky; [8] ddc_sat_sticky; [9] ddc_ovf_sticky; [10] reg_rad_ddc_en; [21:16] adc_eye_width_min; [23:22] ddc_status
0xEC	CLIP_OVF_CNT	RO	0x0000_0000	[15:0] adcr_clip_cnt (saturating 16b); [31:16] adcs_clip_cnt (saturating 16b)
0xF0	DBG_UART_CTRL	R/W	0x0000_043D	[15:0] baud_div (default 1085 on 125 MHz link_clk = 115,207.4 baud, +0.0064% err); [16] stat_periodic_dis; [17] force_stat_p (W1P); [24] uart_rx_idle_high (RO); [25] uart_tx_busy (RO); [26] uart_banner_done (RO); [31:27] uart_rx_ferr_cnt[4:0] (RO)
0xF4	DBG_UART_STAT_DIV	R/W	0x0773_5940	[31:0] Periodic STAT interval in link_clk cycles (default 125,000,000 = 1.000 s)
0xF8	BUILD_GIT_HASH	RO	generic	[31:0] 8-hex git commit prefix injected via synth_design -generic
0xFC	BUILD_TIMESTAMP	RO	generic	{BUILD_DATE[15:0], BUILD_TIME[23:8]} (MMDD_HHMM) injected via synth_design -generic

Source: fpga/link/PINMAP.md

IAS1-to-RF Link Pin Map & Polarity Verification

Scope: End-to-end hardware signal trace from the RF/DAQ front-end Artix-7 (`U1101`, `XC7A50T-FTG256`) across the adapter PCB (`KV260-IAS2RF`), board-to-board connector (`J101`), KV260 carrier IAS1 connector (`J8`), carrier-side buffers/translators (`U18`, `U19`, `U72`), SOM connector (`SOM240_1`), to the Kria K26 SOM (`XCK26-SFVC784-2LV-C`), plus the two Pmod headers (`J2` on KV260 carrier and `J1102` on the adapter board).

Result (link pin check): All five differential `LINK_*` pairs land **P-on-P and N-on-N** between Artix-7 and Kria K26. There is **no** polarity inversion on any differential pair and **no** pin/direction conflict on any of the four single-ended IAS1 signals (`HK_SCL`, `HK_SDA`, `FPGA_PROG_B`, `FPGA_IRQ`).

Verification Legend & Primary Sources

Every table entry is tagged with its verification basis:

- `[M]` **Measured / Direct Inspection** from project schematics/PCB, Vivado part/board files, or AMD KV260 carrier schematic (`XTP682`).
- `[I]` **Inferred** (none required for the pin map tables below; every link row is `[M]`).

Primary sources inspected:

1. Adapter schematics & PCB: `sheets/CONTROL.kicad_sch`, `sheets/IAS_LINK.kicad_sch`, `KV260-IAS2RF.kicad_pcb`
2. Artix-7 package pins & delays: `_work/layout/xc7a50t_ftg256_pkg_delays.csv`, `_work/layout/lvds_skew.py`
3. KV260 carrier schematic: AMD `XTP682` (`KV260_v2/038-05058-03-A1.pdf`, sheets 6, 8, 13, 17)
4. Vivado Board Store & K26 package definitions (`Vivado 2026.1`):
5. `<Vivado 2026.1 install>\data\xhub\boards\XilinxBoardStore\boards\Xilinx\kv260_carrier\2.0\board.xml`
6. `<Vivado 2026.1 install>\data\xhub\boards\XilinxBoardStore\boards\Xilinx\kv260_som\2.0\part0_pins.xml`
7. `<Vivado 2026.1 install>\data\xhub\boards\XilinxBoardStore\boards\Xilinx\k26c\2.0\part0_pins.xml`
8. `<Vivado 2026.1 install>\data\parts\xilinx\zynquplus\public\ibis\pkg\xck26_sfvc784.pkg`

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1. Five Differential `LINK_*` Pairs

All five pairs are AC-coupled with 100 nF capacitors (`C101`–`C110`) on the adapter PCB near `J101`.

- **Artix -> Kria pairs (`LINK_RX_*`):** Driven by Artix Bank 34 (`VCCO = 2.5 V`, `LVDS_25`), received by K26 Bank 66 HP (`VCCO = 1.2 V`, `PL_1V2`, AC-coupled `DIFF_SSTL12` with `ODT = RTT_48` and `EQUALIZATION` enabled per `link-decisions.md` #3).
- **Kria -> Artix pairs (`LINK_TX_*`):** Driven by K26 Bank 66 HP (`VCCO = 1.2 V`, `DIFF_SSTL12` with `OUTPUT_IMPEDANCE = RDRV_60_60`), received by Artix Bank 14 HR (`VCCO = 3.3 V`) as `LVDS_25` inputs **without** `DIFF_TERM` (`DIFF_TERM = FALSE`, external `100 ohm` differential termination `R105`, `R106` and `10k ohm` pull-ups to `+1V2` `R101`–`R104`, `Vcm = 1.2 V`).

> **Pin-ordering note on `J101` / `J8`:** On `LINK_RX_D1` (pins 29/30) and `LINK_TX_D0` (pins 26/27), the lower connector pin number carries `_N` (`29`, `26`) and the higher pin number carries `_P` (`30`, `27`) on **both** the adapter (`J101` in `KV260-IAS2RF.kicad_pcb`) and the KV260 carrier (`J8` in `XTP682` sh. 13). P still lands on P and N still lands on N.

Signal	Dir	Artix `U1101` Ball & Function (Bank / CC)	Adapter Coupling / Term	`J101` Pin	KV260 `J8` Pin & Net (`XTP682` sh.13)	`SOM240_1` Pin (`XTP682` sh.6)	K26 `SFVC784` Ball & Function (Bank / CC)	P-on-P?	Basis
`LINK_RX_D0_P`	A->K	`L4` (`IO_L1P_T0_34`, Bk34, non-CC)	`C101` (100nF) -> `J_LINK_RX_D0_P`	4	4 (`HPA06_P`)	A3	`A2` (`IO_L8P_T1L_N2_AD5P_66`, Bk66 HP, non-CC)	Yes (P->P)	`[M]`
`LINK_RX_D0_N`	A->K	`M4` (`IO_L1N_T0_34`, Bk34, non-CC)	`C102` (100nF) -> `J_LINK_RX_D0_N`	5	5 (`HPA06_N`)	A4	`A1` (`IO_L8N_T1L_N3_AD5N_66`, Bk66 HP, non-CC)	Yes (N->N)	`[M]`
`LINK_RX_D1_P`	A->K	`M2` (`IO_L2P_T0_34`, Bk34, non-CC)	`C105` (100nF) -> `J_LINK_RX_D1_P`	30	30 (`HPA07_P`)	B7	`B3` (`IO_L9P_T1L_N4_AD12P_66`, Bk66 HP, non-CC)	Yes (P->P)	`[M]`
`LINK_RX_D1_N`	A->K	`M1` (`IO_L2N_T0_34`, Bk34, non-CC)	`C106` (100nF) -> `J_LINK_RX_D1_N`	29	29 (`HPA07_N`)	B8	`A3` (`IO_L9N_T1L_N5_AD12N_66`, Bk66 HP, non-CC)	Yes (N->N)	`[M]`

Signal	Dir	Artix U1101 Ball & Function (Bank / CC)	Adapter Coupling / Term	J101 Pin	KV260 J8 Pin & Net (XTP682 sh.13)	SOM240_1 Pin (XTP682 sh.6)	K26 SFVC784 Ball & Function (Bank / CC)	P-on-P?	Basis
LINK_RX_CLK_P	A->K	N3 (IO_L3P_T0_DQS_34, Bk34, DQS)	C103 (100nF) -> J_LINK_RX_CLK_P	7	7 (HPA05_CC_P)	B1	C1 (IO_L7P_T1L_N0_QBC_AD13P_66, Bk66 HP, **QBC**)	Yes (P->P)	[M]
LINK_RX_CLK_N	A->K	N2 (IO_L3N_T0_DQS_34, Bk34, DQS)	C104 (100nF) -> J_LINK_RX_CLK_N	8	8 (HPA05_CC_N)	B2	B1 (IO_L7N_T1L_N1_QBC_AD13N_66, Bk66 HP, **QBC**)	Yes (N->N)	[M]
LINK_TX_D0_P	K->A	M16 (IO_L7P_T1_D09_14, Bk14, non-CC)	C107 (100nF), R105=100R, R101=10k->+1V2	27	27 (HPA08_P)	C9	B4 (IO_L10P_T1U_N6_QBC_AD4P_66, Bk66 HP, QBC)	Yes (P->P)	[M]
LINK_TX_D0_N	K->A	N16 (IO_L7N_T1_D10_14, Bk14, non-CC)	C108 (100nF), R105=100R, R102=10k->+1V2	26	26 (HPA08_N)	C10	A4 (IO_L10N_T1U_N7_QBC_AD4N_66, Bk66 HP, QBC)	Yes (N->N)	[M]
LINK_TX_CLK_P	K->A	N13 (IO_L11P_T1_SRCC_14, Bk14, **SRCC**)	C109 (100nF), R106=100R, R103=10k->+1V2	10	10 (HPA09_P)	D10	D4 (IO_L11P_T1U_N8_GC_66, Bk66 HP, **GC**)	Yes (P->P)	[M]
LINK_TX_CLK_N	K->A	P13 (IO_L11N_T1_SRCC_14, Bk14, **SRCC**)	C110 (100nF), R106=100R, R104=10k->+1V2	11	11 (HPA09_N)	D11	C4 (IO_L11N_T1U_N9_GC_66, Bk66 HP, **GC**)	Yes (N->N)	[M]

Clock-Capability Notes ([M])

- **LINK_RX_CLK_P/N -> K26 C1/B1 (IO_L7P/N_T1L_N0/N1_QBC_AD13P/N_66):** QBC (Quad-Byte Clock) in UltraScale+ Bank 66 HP. Although XTP682 labels the carrier net HPA05_CC_P/N, C1/B1 is a QBC pin (GC pins in Bank 66 are L11..L14), which directly drives Bank 66 byte-clock routing (BITSLICE / ISERDESE3 component-mode CLK via BUFGCE/BUFGCE_DIV or same-bank MMCM/PLL per UG572). LINK_RX_D0 (A2/A1 in T1L_N2/N3) and LINK_RX_D1 (B3/A3 in T1L_N4/N5) sit in the **exact same T1L lower nibble/byte group** as LINK_RX_CLK.
- **LINK_TX_CLK_P/N -> Artix N13/P13 (IO_L11P/N_T1_SRCC_14):** SRCC (Single-Region Clock Capable) in Artix-7 Bank 14. Drives BUFIO + BUFR directly in Bank 14, and LINK_TX_D0 (M16/N16, IO_L7P/N_T1_14) sits in the same T1 byte group of Bank 14.

Routed PCB & Package Delays ([M] / [I])

Measured by _work/layout/lvds_skew.py on KV260-IAS2RF.kicad_pcb (with _work/layout/xc7a50t_ftg256_pkg_delays.csv), K26 SOM trace delays (k26c/2.0/part0_pins.xml), and KV260 carrier estimate (kv260_carrier/2.0/board.xml / XTP682):

Pair	Adapter PCB + Artix Pkg P / N (ps)	K26 SOM Min–Max P / N (ps)	K26 SOM Mid P / N (ps)	KV260 Carrier J8 <-> SOM240_1 (ps)	End-to-End Total P / N (ps)	Skew vs Ref Clock (ps)
LINK_RX_CLK (A->K)	678 / 677 ([M])	371.84–454.47 / 371.74–454.36 ([M])	**413 / 413** ([M])	180 / 180 ([I]*)	**1271 / 1270**	Reference (A->K)
LINK_RX_D0 (A->K)	773 / 772 ([M])	365.49–446.71 / 365.46–446.68 ([M])	**406 / 406** ([M])	180 / 180 ([I]*)	**1359 / 1358**	**+88 ps** vs LINK_RX_CLK
LINK_RX_D1 (A->K)	717 / 717 ([M])	364.58–445.60 / 364.68–445.72 ([M])	**405 / 405** ([M])	180 / 180 ([I]*)	**1302 / 1302**	**+31 ps** vs LINK_RX_CLK (**-57 ps** vs D0)
LINK_TX_CLK (K->A)	661 / 665 ([M])	364.37–445.35 / 364.28–445.23 ([M])	**405 / 405** ([M])	180 / 180 ([I]*)	**1246 / 1250**	Reference (K->A)
LINK_TX_D0 (K->A)	805 / 810 ([M])	366.85–448.37 / 366.99–448.55 ([M])	**408 / 408** ([M])	180 / 180 ([I]*)	**1393 / 1398**	**+147 / +148 ps** vs LINK_TX_CLK

\Carrier delay note ([I]): kv260_carrier/2.0/board.xml lists a uniform placeholder typical_delay="5" on every connection_map entry and XTP682 does not publish per-net PCB trace lengths. The J8 <-> SOM240_1 carrier flight time is modeled as [I] 180 ps common-mode (~27 mm length-matched MIPI CSI-2 stripline/microstrip with < 5 ps inter-pair skew).*

2. Four Single-Ended IAS1 Signals

All J8/J101 single-ended I/Os operate at **1.8 V** (+1V8_D on adapter, PL_1V8 on KV260 carrier). U1101 Bank 35 is powered at 1.8 V.

Signal	Dir	Artix U1101 Ball (Bank / Func)	Adapter Buffering / Passives	J101 / J8 Pin	KV260 Carrier Net & Active Path (XTP682)	SOM240_1 Pin	K26 SFVC784 Ball (Bank / Func / CC)	Basis
HK_SCL	Bi/OD	K5 (IO_25_35, Bk35)	Shared w/ U1105.6 (CAT24C02), U1106 (TMP1075)	14	IAS1_I2C_SCK -> U18 (TCA9546A, sh.8) ch1 SC1 <-> SCL -> HDA00_CC	D16	G11 (IO_L5P_HDGC_45, Bk45 HD, HDGC)	[M]
HK_SDA	Bi/OD	J5 (IO_L19P_T3_35, Bk35)	Shared w/ U1105.5 (CAT24C02), U1106 (TMP1075)	22	IAS1_I2C_SDA -> U18 (TCA9546A, sh.8) ch1 SD1 <-> SDA -> HDA01	D17	F10 (IO_L5N_HDGC_45, Bk45 HD, HDGC)	[M]
FPGA_PROG_B	K->A	L9 (PROGRAM_B_0, Bk0)	U1103 (74LVC1G07 OD buffer: pin 2 A <- /FPGA_PROG_B, pin 4 Y -> /CONTROL/PROGRAM_B)	21	IAS1_RESET_B (pull-up to PL_1V8) <- U19 (SLG7XL46528, sh.8) PL_RESET_OUT2_B <- PL_RESET_IN2_B <- HDA04	B17	K13 (IO_L2P_AD14P_45, Bk45 HD) *	[M]
FPGA_IRQ	A->K	H5 (IO_L18P_T2_35, Bk35)	R1133 = 47k pull-down to GND	15	HPA13_FLASH -> U72 (SN74AVC4T245, sh.13) 2A1(8, 1.8V) -> 2B1(13, 1.2V) w/ 2DIR(5)=PL_1V8 (A->B) -> HPA13_P	A12	G8 (IO_L16P_T2U_N6_QBC_AD3P_66, Bk66 HP, QBC)	[M]

\Board Store note for som240_1_b17 (HDA04):* k26c/2.0/part0_pins.xml maps som240_1_b17 to K26 ball K13 (and b16->J10, b18->K12), whereas kv260_som/2.0/part0_pins.xml has an off-by-one loc shift on b16/b17/b18 (b17 lists loc="J10" alongside K13's trace delay 0.39667..0.48483 ns). Always verify/override against the K26 SOM schematic (K26 XDC from Vivado board preset k26c vs kv260_som) before carrier bring-up bitgen.

3. Pmod Headers (J2 on KV260 Carrier, J1102 on Adapter)

These two 12-pin Pmod headers are **independent** hardware ports (not wired to each other):

- **J2 (KV260 Carrier, XTP682 sh. 17):** Connected to Kria K26 Bank 45 HD (3.3 V via PMOD_HDA*).
- **J1102 (Adapter Board, sheets/CONTROL.kicad_sch / KV260-IAS2RF.kicad_pcb):** Connected to Artix-7 Bank 15 (3.3 V HR) for radar SPI / PPS / strobe debug.

3a. KV260 Carrier Pmod J2 -> Kria K26 ([M])

J2 Pin	Carrier Net (XTP682 sh.17)	SOM240_1 Pin (XTP682 sh.6)	K26 SFVC784 Ball	K26 Function (Bank 45 HD)	Basis
1	PMOD_HDA11	A17	H12	IO_L4N_AD12N_45	[M]
3	PMOD_HDA12	D20	E10	IO_L7P_HDGC_45 (HDGC)	[M]
5	PMOD_HDA13	D21	D10	IO_L7N_HDGC_45 (HDGC)	[M]
7	PMOD_HDA14	D22	C11	IO_L9P_AD11P_45	[M]
2	PMOD_HDA15	B20	B10	IO_L9N_AD11N_45	[M]
4	PMOD_HDA16_CC	B21	E12	IO_L8P_HDGC_45 (HDGC)	[M]
6	PMOD_HDA17	B22	D11	IO_L8N_HDGC_45 (HDGC)	[M]
8	PMOD_HDA18	C22	B11	IO_L10P_AD10P_45	[M]
9, 10	GND	n/a	n/a	n/a	[M]
11, 12	PMOD_3V3	n/a	n/a	n/a	[M]

3b. Adapter Pmod J1102 -> Artix-7 U1101 ([M])

J1102 Pin	Adapter Net (CONTROL)	Artix U1101 Ball	Artix Function (Bank 15, 3.3 V)	Basis
1	/CONTROL/PMOD_CS	H16	IO_L22P_T3_A17_15	[M]
2	/CONTROL/BEAM_STROBE	J16	IO_L23N_T3_FWE_B_15	[M]
3	/CONTROL/PMOD_MOSI	G16	IO_L22N_T3_A16_15	[M]
4	/CONTROL/PPS_SYNC	H14	IO_L24P_T3_RS1_15	[M]
5	/CONTROL/PMOD_MISO	J15	IO_L23P_T3_FOE_B_15	[M]
6	/CONTROL/PMOD_SPARE1	G15	IO_L24N_T3_RS0_15 (dbg_uart RX / Kria D11 PS UART1 TX, PULLUP)	[M]
7	/CONTROL/PMOD_SCLK	D13	IO_L12P_T1_MRCC_15 (MRCC)	[M]
8	/CONTROL/PMOD_SPARE2	G11	IO_25_15 (dbg_uart TX / Kria B11 PS UART1 RX)	[M]
9, 10	GND	n/a	n/a	[M]

J1102 Pin	Adapter Net (CONTROL)	Artix U1101 Ball	Artix Function (Bank 15, 3.3 V)	Basis
11, 12	Unconnected (NC)	n/a	n/a	[M]

Source: fpga/eth/REV06.md

Rev06 Gateware Implementation: Dual-Path 1000BASE-X SGMII + IAS1 (`ENABLE_ETH=1`)

Implementation and verification record for the **Rev06 Dual-Path Ethernet + IAS1** Artix-7 (`XC7A50T-2FTG256I`) gateware (`fpga/artix/top.v`, `ENABLE_ETH=1`).

1. Architecture Summary

Rev06 adds dedicated `RTL8211FSI-CG` (`U1201`) → `HR911130C` (`J1201`) `1000BASE-T` SGMII Ethernet on its own outer-ring Artix-7 pins while preserving the **complete `2`-lane `IAS1` uplink (`LINK_RX_D0` `L4/M4`, `LINK_RX_D1` `M2/M1`, `LINK_RX_CLK` `N3/N2`) and `1`-lane downlink (`LINK_TX_D0` `M16/N16`, `LINK_TX_CLK` `N13/P13`)**.

Block	Module (`fpga/artix/`)	Clock Domain(s)	Key Function
SGMII PCS / SERDES PHY	`eth_sgmii_phy.v` + `eth_8b10b.v`	`625 MHz` DDR (`ISERDES/OSERDES`), `312.5 MHz` (`10b`), `125 MHz` (`GMII`)	`4`-phase `ISERDESE2` oversampling with `IDELAYE2` (`312.5 MHz` 40-bit sliding window, comma align & dynamic `I/Q` phase selection), `OSERDESE2` `10:1` DDR (`5:1` @ `625 MHz`), `8b/10b` encode/decode (`eth_8b10b_enc/dec`), IEEE 802.3 Clause 37 SGMII Auto-Negotiation (`I1`/`I2`/`C1`/`C2`, `lp_adv_ability`)
PHY Management	`eth_mdio.v`	`125 MHz` → `1.95 MHz` MDC	Clause 22 MDIO master with open-drain `IOBUF` (`.I(1'b0)`, `.T(~(mdio_oe & ~mdio_out))`) for `3.3 V` Bank 14 `M15` pulled up to `2.5 V` `DVDDRG` via `R1213`), `10 ms` reset pulse, and BMSR polling
UDP/IPv4 + MAC Engine	`eth_mac_udp.v`	`125 MHz`	Full GMII/SGMII MAC (`Preamble/SFD`, `CRC-32/FCS` check & append), ARP responder, ICMP echo responder, bidirectional UDP/IPv4 RX (`0xC0DE` control writes mapped to `ctrl_wr_*` registers & `0xE0` dual-path control) and TX streaming (`ip_hdr_csum` `4`-stage pipeline during `TX_PREAM` `tx_hdr_idx == 0..3`; `tx_bytes_rem > 16'd2` word-pop guard)
SDR Stream Source	`eth_sdr_pkt_gen.v`	`125 MHz`	Generates `stream_id=1` SDR UDP packets (`64`-bit header/payload words, `seq_num`)
Dual-Path Store-and-Forward Mux	`dual_path_mux.v`	`125 MHz`	Dual BRAM store-and-forward FIFOs (`dual_path_sf_fifo`, `512 × 64`-bit, `255` pkt descriptors) supporting 4 runtime policies: `0` Stream Split, `1` `1+1` Mirror Duplication, `2` IAS-Only, `3` ETH-Only

Pin Mapping (`fpga/artix/xc7a50t.xdc`)

- **SGMII TX (`ETH_SGTX_PHY`):** `R2` / `R1` (`LVDS_25`, Bank 34 `VCCO = 2.5 V`, `OBUFDS`)
- **SGMII RX (`ETH_SGRX_PHY`):** `R3` / `T2` (`LVDS_25`, `DIFF_TERM = TRUE`, Bank 34 `VCCO = 2.5 V`, `IBUFDS_DIFF_OUT`)
- **MDIO Clock (`ETH_MDC`):** `P1` (`LVCMOS25`, Bank 34)
- **MDIO Data (`ETH_MDIO`):** `M15` (`LVCMOS33`, Bank 14, **open-drain only** via `IOBUF .I(1'b0)`; `BITSTREAM.CONFIG.EXTMASTERCCLK_EN DISABLE` so `EMCCLK` is never active)
- **PHY Reset (`ETH_RST_N`):** `K13` (`LVCMOS33`, Bank 14)
- **Intact `IAS1` Trunk:** `LINK_RX_D0` (`L4/M4`), `LINK_RX_D1` (`M2/M1`), `LINK_RX_CLK` (`N3/N2`), `LINK_TX_D0` (`M16/N16`), `LINK_TX_CLK` (`N13/P13`)

2. XSim Verification (`fpga/sim/`)

All benches run with Xilinx `xsim` (`Vivado v2026.1`):

Testbench / Mutation	Command	Result	Observed Output Summary
`tb_sgmii_lvds`	`.\fpga\sim\run.ps1 tb_sgmii_lvds`	**PASS**	`PASS: tb_sgmii_lvds (+100/-100 ppm 60,000 bits, 0 errors)`
`tb_rev06` (baseline)	`.\fpga\sim\run.ps1 tb_rev06`	**PASS**	`PASS: tb_rev06 ias_s1=79 eth_s1=11 ias_s2=51 eth_s2=61 max_s1=78 max_s2=100 phase_sw=145 lost=0`
`tb_rev06` (`no_phase_select`)	`.\fpga\sim\run.ps1 tb_rev06 -Mutate no_phase_select`	**FAIL (expected)**	Fails SGMII comma lock / auto-negotiation with dynamic phase selection disabled

Testbench / Mutation	Command	Result	Observed Output Summary
`tb_rev06` (`eth_skip_fcs`)	`.\fpga\sim\run.ps1 tb_rev06 -Mutate eth_skip_fcs`	**FAIL (expected)**	Accepts corrupted-FCS UDP control frame instead of dropping it
`tb_e2e` regression	`.\fpga\sim\run.ps1 tb_e2e`	**PASS**	`PASS: tb_e2e peak_k=60 img_rej_db=61.03 pkts=32 crc_err=0 seq_err=0 proto_err=0 ts=0001000000004528`

3. Vivado Place & Route (`XC7A50T-FTG256-2`, `build_rev06.tcl`)

Synthesized, placed, physically optimized, and routed with `-generic ENABLE_ETH=1'b1` (`fpga/artix/reports_rev06/`):

Timing Summary (`reports_rev06/timing_summary.rpt`, `pulse_width.rpt`)

Metric	Result	Failing Endpoints	Total Endpoints
WNS / TNS (Setup)	**`+0.039 ns`** / `0.000 ns`	`0`	`28,902`
WHS / THS (Hold)	**`+0.036 ns`** / `0.000 ns`	`0`	`28,836`
WPWS / TPWS (Pulse Width)	**`+0.008 ns`** / `0.000 ns`	`0`	`8,515`
DRC (`reports_rev06/drc.rpt`)	**`0` Errors** (`50` Warnings/Advisories)	n/a	n/a

Key clock domains closed: `clk_adcr_dco` (`200 MHz`, `WNS=0.076 ns`), `clk_100m_unbuf` (`100 MHz`, `WNS=1.964 ns`), `clk_200m_unbuf` (`200 MHz`, `WNS=0.282 ns`), `clk_400m_unbuf` (`400 MHz`, `WNS=0.210 ns`), `link_clk_unbuf` (`125 MHz`, `WNS=0.444 ns`), `gen_rev06_eth.clk_312p5_u` (`312.5 MHz`, `WNS=0.219 ns`), `gen_rev06_eth.clk_625_0_u` / `clk_625_90_u` (`625 MHz` DDR, `WPWS=0.008 ns`), and `dl_rx_clk` (`125 MHz`, `WNS=2.021 ns`).

Hierarchical Utilization (`reports_rev06/utilization.rpt`)

Hierarchy	Module	LUTs (Logic / LUTRAM)	FFs	RAMB36	RAMB18	DSP48E1
`artix_top` (Total)	n/a	**`6,369`** (`6,223` / `146`)	**`8,088`**	**`8`**	**`1`**	**`87`**
`gen_rev06_eth.u_dual_mux`	`dual_path_mux`	`473` (`473` / `0`)	`299`	`8`	`0`	`0`
`gen_rev06_eth.u_eth_mac`	`eth_mac_udp`	`798` (`798` / `0`)	`868`	`0`	`0`	`0`
`gen_rev06_eth.u_eth_mdio`	`eth_mdio`	`131` (`131` / `0`)	`99`	`0`	`0`	`0`
`gen_rev06_eth.u_eth_phy`	`eth_sgmii_phy`	`561` (`515` / `46`)	`349`	`0`	`1`	`0`
`gen_rev06_eth.u_sdr_gen`	`eth_sdr_pkt_gen`	`20` (`20` / `0`)	`132`	`0`	`0`	`0`
Rev06 Ethernet Subtotal	n/a	**`1,983`** (`1,937` / `46`)	**`1,747`**	**`8`**	**`1`**	**`0`**
`u_adc_cap` + `u_ddc` + `u_ul_pcs_tx` + `u_dl_*` + `u_pmod_spi`	Core + `IAS1`	`4,386`	`6,341`	`0`	`0`	`87`

Final Post-Route Implementation on `main` (`fpga/artix/reports_rev06/`)

With wideband SDR DDC (`u_sdr_ddc`), AERIS-10 Radar DDC (`u_ddc`), dedicated-pin 1000BASE-T SGMII/UDP (`gen_rev06_eth`), 2-lane `IAS1`, XADC/PPS, DACs, and housekeeping enabled (`ENABLE_ETH = 1`):

Resource (`XC7A50T-FTG256-2`)	Used	Available	Utilization
Slice LUTs (`15,250` Logic + `166` LUTRAM; `18,045` packed LUT primitives)	**15,416**	32,600	**47.3%**
Flip-Flops (`Slice Registers`)	**17,445**	65,200	**26.8%**
Block RAM (`RAMB36` eq.) (`13` `RAMB36` + `6` `RAMB18`)	**16.0**	75	**21.3%**
DSP48E1	**110**	120	**91.7%**
Timing (`report_timing_summary`)	`WNS = +0.147 ns`, `WHS = +0.036 ns`, `WPWS = +0.008 ns`	n/a	**0 failing endpoints** (`0` DRC errors)

Full dual-FPGA documentation and Vivado 2026.1 silicon floorplans/schematics: **`docs/FPGA_GATEWARE.md`**.

Source: fpga/eth/REDUNDANCY.md

Ethernet Load-Balancing & Link Redundancy Architecture

> **Production `main` Baseline (`ENABLE_ETH = 1`):** `U1201` (`RTL8211FSI-CG`) is wired to **dedicated Bank 34 `LVDS_25` pins** (`R2/R1 ETH_SGTX`, `R3/T2 ETH_SGRX`, with `ETH_MDIO/MDC/RST_N` on Bank 14 `P1/M15/K13`), keeping **both** `IAS1` data lanes (`LINK_RX_D0` + `LINK_RX_D1`) and `1000BASE-T` Ethernet active simultaneously (`~2.94 Gb/s` combined uplink + `~1.48 Gb/s` combined downlink, Mode 6 below). Earlier shared-pair trade-off modes (`1`–`5`) are retained below for reference.

Analysis of pairing Gigabit Ethernet (`U1201 RTL8211FSI-CG` + `J1201 HR911130C`) with the existing `IAS1` LVDS link (`J8`) as a load-balanced second transport or redundant failover channel between the `XC7A50T-2FTG256I` front-end FPGA and the AMD Kria `KV260` (`XCK26-SFVC784-2LV-C`).

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1. Current Board (`Rev05` / `Rev04+ETH`) With `ETH` BOM Option Fitted

Per `docs/CONTROL_SPEC.md §7` and `docs/SIGNAL_INTEGRITY.md §9.7`, selecting the Ethernet assembly option fits `C1218–C1221` (`100 nF 0402`) and removes `C101, C102, C107, C108`.

1.1 Surviving `IAS1` Lanes vs Claimed Pairs

Signal Pair	Artix-7 Pins (Bank)	K26 SOM Pins (`J8`)	Direction (ETH Option Fitted)	Status
`LINK_RX_D0`	`L4 / M4` (Bank 34, `2.5 V`)	`A2 / A1` (`HPA06`, floating)	Artix `OBUFDS` → `C1220/C1221` → `U1201 HSIP/N` (`ETH_SGTX_PHY`)	**Claimed by Ethernet TX (`1.25 Gb/s`)** (`C101/C102` removed)
`LINK_TX_D0`	`M16 / N16` (Bank 14, `3.3 V`)	`B4 / A4` (`HPA09`, floating)	`U1201 HSOP/N` → `C1218/C1219` → Artix `IBUFDS_DIFF_OUT` (`ETH_SGRX_PHY`)	**Claimed by Ethernet RX (`1.25 Gb/s`)** (`C107/C108` removed)
`LINK_RX_D1`	`M2 / M1` (Bank 34, `2.5 V`)	`B3 / A3` (`HPA07`)	Artix → Kria (`DIFF_SSTL12 ODT=RTT_48`)	**Intact (1 uplink data lane)**
`LINK_RX_CLK`	`N3 / N2` (Bank 34, `2.5 V`)	`C1 / B1` (`HPA05_CC`)	Artix → Kria (`500–625 MHz` DDR source-sync clock)	**Intact (1 uplink clock)**
`LINK_TX_CLK`	`N13 / P13` (Bank 14 SRCC)	`D4 / C4` (`HPA08`)	Kria → Artix	**Intact (unused by Ethernet)**
`HK_SCL/SDA`, `FPGA_PROG_B`, `FPGA_IRQ`	Bank 35 (`1.8 V`)	`J8` pins `14, 22, 21, 15`	Slow I2C / reset / interrupt	**Intact**

Fitting Ethernet does **not** eliminate `IAS1`; it converts `IAS1` from a `2`-lane uplink + `1`-lane downlink into a **`1`-lane uplink (`LINK_RX_D1` + `LINK_RX_CLK`) plus a `1 Gb/s` bidirectional Ethernet path**.

1.2 Signal-Integrity Check on Running `LINK_RX_D1` Concurrently with `ETH_SGTX_PHY`

`CONTROL_SPEC.md §7` and `SIGNAL_INTEGRITY.md §9.7` note that `ETH_SGTX_PHY` runs beside `LINK_RX_D1_N` on **L1** for **`5.2 mm` at `0.17 mm` edge-to-edge gap**, and advise holding `LINK_RX_D1` static in an Ethernet-only build. Evaluating concurrent operation (`LINK_RX_D1` + `ETH` both active at `1.25 Gb/s`):

- **Measured board eyes (`SIGNAL_INTEGRITY.md` & `IAS_LINK_SPEC.md`):**
- `ETH_SGTX_PHY` arrives at `U1201` with **`350 mV` eye / `50 ps` jitter** (Artix LVDS driver launch on `LINK_RX_D0` = `601–607 mV` at `J8` pad).
- `ETH_SGRX_PHY` arrives at `M16/N16` with **`637 mV` eye / `53 ps` jitter**.
- `LINK_RX_D1` opens **`491 / 524 mV`** (`P/N`) at `1.25 Gb/s` (`575 / 559 mV` at `1.0 Gb/s`).
- Receiver threshold for `LVDS_25` (`DS181 Table 11`) is **`100 mV` (`200 mV` differential peak-to-peak)**.
- **NEXT / FEXT coupling magnitude (`SIGNAL_INTEGRITY.md §3.5`):**
- On `L1` (`0.183 mm` microstrip over `0.1164 mm` prepreg), 2D NEXT at `≥ 25 mm` saturated length is **`14.5%` at `0.15 mm`** and **`7.7%` at `0.25 mm`** (linear interpolation at `0.17 mm` ≈ **`13.1%`**).
- Scaling linearly below `25 mm` (`5.2 mm / 25 mm = 0.208`) gives a 2D upper bound of **`2.7%`** (`~9.5 mV` on a `350 mV` leg).
- Per `pair_xtalk.py` (3D openEMS calibration in `SIGNAL_INTEGRITY.md`), 2D overestimates 3D microstrip NEXT by **`~3.5×`** (`12.6 mm @ 0.15 mm` produced **`1.9%`** ≈ `7 mV`). Scaling `1.9%` down to `5.2 mm` and wider `0.17 mm` yields **`~0.7%–0.8%` (`~2.5–3 mV`**

single-ended).

- Even better, `LINK_RX_D1` and `ETH_SGTX_PHY` are co-directional FPGA outputs (`L4/M4` and `M2/M1`), so direct forward crosstalk dominates and backward NEXT appears primarily from downstream reflections. A `< 10 mV` (`2D` worst-case) / `~3 mV` (`3D` estimate) perturbation leaves **`> 140 mV` (`ETH_SGTX_PHY`) and `> 280 mV` (`LINK_RX_D1` @ `1.25 Gb/s`)** differential margin above the `200 mV` threshold.
- **Conclusion:** Holding `LINK_RX_D1` static is safest when Ethernet alone suffices, **but running `LINK_RX_D1` concurrently with `ETH` is electrically sound (`< 3%` 2D / `~0.8%` 3D coupling)** once eye-tested at `1.25 Gb/s`.

1.3 Kria-to-Artix (`K→A`) Control Paths When `ETH` Claims `LINK_TX_D0`

Because `J8` has only one `K→A` high-speed data pair (`LINK_TX_D0`) and Ethernet claims it:

1. **UDP Control over `ETH` (default in-band path):** Bidirectional `1000BASE-T` SGMII natively delivers register writes, `retrain`, `prbs7` test enables, and `ADAR1000` beam updates from Kria Linux (`PS GEM3`) to Artix without extra cables. *Weakness:* shares fate with Ethernet.
2. **External Pmod Cable `J2 ↔ J1102` (out-of-band fail-safe):** Per `fpga/link/PINMAP.md`, Kria `J2` (`Bank 45 HD`, `3.3 V`) and Artix `J1102` (`Bank 15`, `3.3 V`) are not PCB-connected across `J8`; a short 12-pin Pmod ribbon/jumper cable restores the complete `pmod_spi` (`CS_n`, `SCLK`, `MOSI`, `MISO`), hardware `beam_strobe`, `pps_sync`, and `2` spare pins, completely decoupled from both Ethernet and `IAS1`.
3. **Fallback Serial over `LINK_TX_CLK` (`D4/C4 → N13/P13`) + `J8` GPIO:** `LINK_TX_CLK` stays wired `Kria → Artix` through `J8` in `ETH` mode. Repurposing `LINK_TX_CLK` as a DC-balanced Manchester/UART/8b10b low-rate control channel (`10–50 Mb/s`) provides cable-free `K→A` control even if `ETH` is disconnected (and `FPGA_IRQ` + `HK_SCL/SDA` remain intact).

1.4 Aggregate Throughput & Redundancy in `Rev05` Dual Mode

Metric	`IAS1` (`LINK_RX_D1`, 1-lane)	`ETH` (`1000BASE-T` SGMII)	Dual Mode Aggregate
Line Rate	`1.00 Gb/s` (nom.) / `1.25 Gb/s` (`-2` max)	`1.25 Gb/s` (8b/10b → `1.00 Gb/s` MAC)	`2.25` / `2.50 Gb/s` wire
Coding & Header Overhead	`64/66` (`96.97%`) – AM & `/S/`/`/T/`/`CRC` (`~2%`)	`958 Mb/s` (`1500 B` UDP) / **`993 Mb/s`** (`9000 B` jumbo UDP)	n/a
Usable Uplink Payload	**`~0.95 Gb/s`** (`1.0G`) / **`~1.19 Gb/s`** (`1.25G`)	**`~0.99 Gb/s`** (jumbo)	**`~1.94 Gb/s`** (`1.0G IAS1`) / **`~2.18 Gb/s`** (`1.25G IAS1`)
Radar + SDR Fit	Radar `DDC_POST_DECIM=4` (`0.80 Gb/s`) fits 1 lane	Covers SDR I/Q (`<= 0.99 Gb/s`) + control	Covers `1.60 Gb/s` Radar (`DECIM=2`) OR simultaneous Radar (`0.80 Gb/s`) + SDR (`<= 1.19 Gb/s`)
Single-Path Failover	Survives `RJ45`/switch/PHY fault (`~0.95–1.19 Gb/s` degraded uplink)	Survives `J8` `D1` contact/eye fault (`~0.99 Gb/s` degraded uplink + control)	**Eliminates single connector/cable SPOF**

2. KV260 Network Architecture, Bonding vs Application Merge, and Failover

2.1 KV260 Ethernet Port Count & PS vs PL Mapping (`UG1089`, `UG1085`)

- **On-board Ethernet port:** Per `UG1089` and Vivado board preset `k26c/2.0/preset.xml` (`PSU__CRL_APB__GEM3_REF_CTRL__FREQMHZ = 125`), the KV260 carrier provides **exactly one** physical Ethernet port: RJ45 **`J10`**, driven by Zynq UltraScale+ MPSoC **`PS GEM3`** (`MIO 64–77`) through an on-board RGMII PHY (`TI DP83867`).

2.2 Topologies: Direct Cable vs Switch

Aspect	Topology A: Direct Patch (`Adapter J1201 ↔ KV260 J10`)	Topology B: Ruggedized GbE Switch (`Adapter + KV260 + LiDAR + PC`)
Dedicated BW to KV260	Full **`993 Mb/s`** (jumbo UDP) uncontended	Shared on `J10` (`1.0 Gb/s` cap minus LiDAR `~10–100 Mb/s` & control)
Added Latency / Jitter	**`~5–15 µs`** wire + PHY	`+5–20 µs` switch fabric + queuing jitter when LiDAR bursts
External Connectivity	Needs USB-GbE dongle on KV260 for LiDAR/laptop	Native multi-host LAN (`J10` connects all)
Single Point of Failure	Minimal (passive cable only)	Switch PSU / PoE / boot becomes common SPOF

2.3 Linux Kernel `bonding` vs Application-Level Merge

Linux kernel `bonding` (`mode=0` `balance-rr`, `mode=1` `active-backup`, `mode=4` `802.3ad`) **is the wrong layer** for combining `IAS1` (`PL AXI-Stream`) and `ETH` (`PS GEM3` `eth0`):

1. `IAS1` enters K26 PL directly into `fpga/kria/link_axis.v` (AXI4-Stream → AXI-DMA to PS DDR), not as a Linux `net_device`. Emulating an Ethernet TAP/netdev around `IAS1` wastes CPU copies and interrupts, and Linux `balance-rr` would severely reorder packets between a **`~1–3 µs` PL DMA path (`IAS1`)** and a **`~50–250 µs` PHY + `GEM3` + `macb` NAPI path (`ETH`)**.
2. **Recommended: Application-Level Merge using `LINK_PROTOCOL.md` Framing:** `LINK_PROTOCOL` already embeds **`stream_id[7:0]`**, **`seq_num[31:0]`**, **`pkt_len[15:0]`**, and **`pps_timestamp_ns[63:0]`** in every packet. Wrapping the same `16 B` metadata header inside `ETH` UDP payloads lets the Kria PS ingest `IAS1` via AXI-DMA ring and `ETH` via `AF_XDP` / `recvmmsg`, merging them directly by `(stream_id, seq_num)` or `pps_timestamp_ns` in shared DDR ring buffers with zero kernel netfilter overhead.

2.4 Failover Detection, Switch-Over Loss, and Load-Balancing Policies

- **Detection latency:**
- `IAS1` failure: `fpga_irq` + Clause 49 `10_block_lock` / `crc_err` triggers within **`~1–10 µs`** (`3.4 µs` for 64 consecutive invalid sync headers).
- `ETH` failure: PHY MDIO link-down polling takes `10–100 ms`; in-band `seq_num` watchdog / UDP keepalive timeout in Kria PS or Artix RX heartbeat detects link stall in **`1–10 ms`**.
- **Switch-over packet loss vs BRAM buffering:** At `1.0 Gb/s` (`125 MB/s`), `10 ms` of blind flight equals `1.25 MB` (larger than `XC7A50T`'s `75 × 36 Kb = 337.5 KB` total BRAM). However:
- For `IAS1` → `ETH` failover (`10 µs` fault detection via `FPGA_IRQ` / local TX monitoring if `LINK_RX_D1` / `K26` back-channels faults via `ETH` or `Pmod`), a **`64 KB` BRAM elastic buffer** (`~15 × 36 Kb` BRAM, `20%` of chip) holds **`512 µs`** of `1 Gb/s` data, sufficient for **zero-loss** fast switchover on `IAS1` link glitches.
- For **`0`-packet-loss against sudden `RJ45` unplug (`1–10 ms` timeout)**, **Policy 4 (`1+1` Active-Active Hitless Duplication)** sends identical packets (`<= 950 Mb/s`) across both links; the Kria PS deduplicates on `seq_num`, guaranteeing **zero dropped frames** at the cost of no rate aggregation.
- **Load-Balancing Policies:**
- **Active-Backup (`Hot Standby`):** `IAS1 D1` primary (`0.95–1.19 Gb/s`), `ETH` warm standby (carries `K→A` control + keepalive). Minimal jitter, simple failover (`1–10 ms` gap).
- **Stream-Pinned Split (Recommended default):** `stream_id = 0` (Radar DDC `0.80 Gb/s`) pinned to `IAS1 D1`; `stream_id = 1` (SDR ADC + telemetry) + `K→A` control pinned to `ETH`. Zero cross-path packet reordering; full **`~1.94–2.18 Gb/s`** aggregate; on either path failure, drop low-priority stream or dynamically raise `DDC_POST_DECIM` so the surviving `~0.95 Gb/s` lane keeps the primary sensor online.
- **Weighted Packet Striping (`seq_num` Reorder Buffer):** Distribute chunks dynamically across `IAS1` (`~55%` @ `1.25G`) and `ETH` (`~45%`) for a single `> 1.2 Gb/s` burst stream; requires `≥ 512 KB` DDR reorder window on Kria PS to absorb `~50–250 µs` relative `ETH` vs `IAS1` latency skew.
- **`1+1` Hitless Duplication:** Mirror `<= 0.95 Gb/s` mission-critical stream on both `IAS1` and `ETH` and deduplicate via `seq_num` in PS (**`0` packet loss** on instant fault).

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3. Protocol, Jumbo Frames (`9000 B`), and FPGA Utilization

3.1 Raw Layer-2 (`EtherType`) vs UDP/IPv4 + Jumbo Support

Protocol Choice	Overhead per Frame (`1500 B` / `9000 B`)	Effective Wire Rate (`1.00 Gb/s` MAC)	Artix Logic Delta	Operational Trade-off
Raw L2 (`EtherType` `0x88B5`)	`14 B` L2 + `4 B` FCS + `20 B` IFG/pre = `38 B`	`975 Mb/s` / `996 Mb/s`	Baseline (`eth_mac_1g` only)	Lowest LUTs, requires `CAP_NET_RAW` (`AF_PACKET`), non-routable across L3 subnets
UDP/IPv4 (Static ARP/IP)	`42 B` L2/IP/UDP + `4 B` FCS + `20 B` IFG/pre = `66 B`	`958 Mb/s` / **`993 Mb/s`**	`+~400–800` LUTs (fixed header + ARP/UDP TX/RX)	Standard Linux `recvmmsg`/`AF_XDP`, routable across switches/PCs, Wireshark-native

- **Jumbo Frame Support (`9000 B`) Confirmed End-to-End:**
- **`RTL8211FSI-CG`:** Per Realtek datasheet summaries (`search_web`), natively supports jumbo frames up to **`16 KB`**.
- **KV260 `PS GEM3`:** Per AMD `UG1085` and the Linux `macb` driver, `ZynqMP GEM` hardware supports up to **`10,240 B`** frames

(`jumbo_frames` / `JML` register), allowing `ip link set eth0 mtu 9000` cleanly.

- Using **`9000 B` UDP jumbo frames** cuts L2/IP/UDP + preamble overhead from `4.2%` (`958 Mb/s`) to **`0.73%` (`993 Mb/s`)** and reduces Linux PS packet/interrupt rate **6×** (`~13.8 kpps` vs `~82.2 kpps` at `1 Gb/s`).
- **`LINK_PROTOCOL` Reuse:** Prepend the `16 B` `LINK_PROTOCOL.md` header (`{stream_id[7:0], flags[7:0], pkt_len[15:0], seq_num[31:0], pps_timestamp_ns[63:0]}`) directly at UDP payload offset `0` (dropping redundant inner CRC32 if trusting Ethernet `FCS`, or keeping it for end-to-end bus integrity across DMA). That yields `~8,960 B` (`1,120 × 64-bit` ADC/IQ words) per jumbo UDP packet (`99.1%` net sensor efficiency).

3.2 Open-Source `verilog-ethernet` (MIT) vs Current `artix_top` Utilization

From `fpga/artix/reports_rev06/utilization.rpt`, `fpga/eth/test/reports/utilization.rpt`, `fpga/kria/reports/utilization.rpt`, and Vivado `get_parts`:

Resource	XC7A50T-FTG256-2 Available	Current `artix_top`	`sgmii_lvds` PoC	Custom 8b10b/PCS + `verilog-ethernet` (MIT `eth_mac_1g` + `udp` + `64 KB` replay FIFO)	Projected Artix-7 Total (% Used)	Kria `kria_top` Baseline
LUTs	`32,600`	`4,441` (`13.6%`)	`287` (`0.88%`)	`~1,800–3,500`	**`~6,528–8,228` (`20.0%–25.2%`)**	`4,278` / `117,120` (`3.65%`)
Flip-Flops	`65,200`	`6,311` (`9.7%`)	`364` (`0.56%`)	`~1,800–3,000`	**`~8,475–9,675` (`13.0%–14.8%`)**	`6,817` / `234,240` (`2.91%`)
`36 Kb` BRAM	`75` (`337.5 KB`)	`0` (`0%`)	`0` (`0%`)	`~18–22` (`2–6` MAC/UDP + `15` for `64 KB` buffer)	**`~18–22` (`24.0%–29.3%`)**	none (`PS GEM3` uses PS DDR)
DSP48E1	`120`	`87` (`72.5%`)	`0`	`0`	**`87` (`72.5%`)**	n/a
MMCM	`5`	`2` (`40%`)	`1` (or shared)	`0`	**`3` (`60%`)**	n/a

Conclusion: Even with a `64 KB` elastic failover buffer, MIT-licensed `verilog-ethernet` + custom 8b/10b PCS + `sgmii_lvds` uses **`~25%` of LUTs, `~15%` of FFs, and `< 30%` of BRAMs**, leaving over **70% headroom** in `XC7A50T-2FTG256I`. On the Kria side, `GEM3` is a hard PS peripheral requiring **zero PL LUTs**.

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4. Next Board Revision (`Rev06`): Giving Ethernet Its Own FPGA Pins (Report Only)

No board or schematic files are edited here; hardware findings below are strictly for a future `Rev06` revision.

4.1 Free Artix-7 Banks & Differential Pairs (`_work/sheets/control_spec.py` & `_work/layout/xc7a50t_ftg256_pkg_delays.csv`)

Bank 34 (`VCCO = 2.5 V`) currently uses only **`3` of its `9` differential pairs** (`L4/M4`, `M2/M1`, `N3/N2`). **`6` complete differential pairs and `2` single-ended pins (`14` balls total) are completely unused (`NC`):**

Free Bank 34 Diff Pair (`VCCO = 2.5 V`)	Pin Function	Suggested `Rev06` Assignment	Legal `IOSTANDARD` & Advantages
`R2 / R1`	`IO_L7P/N_T1_34`	**`ETH_SGTX_PHY`** (`Artix → U1201`)	**`LVDS_25`** native output (`2.5 V` bank)
`R3 / T2`	`IO_L8P/N_T1_34`	**`ETH_SGRX_PHY`** (`U1201 → Artix`)	**`LVDS_25` with `DIFF_TERM = TRUE`** (legal because `VCCO = 2.5 V`! Removes external `100 Ω` stub; `IODELAY_GROUP` or regional `BUFIO` in Bank 34)
`T4 / T3`	`IO_L9P/N_T1_DQS_34`	Spare LVDS (or `ETH` clk/sync if needed)	`LVDS_25`
`N1 / P1`, `P4 / P3`, `M5 / N4`	`IO_L4..6_T0_34`	Spare LVDS (`T0` nibble shared with `LINK_RX_*`)	`LVDS_25`
`L5`, `P5`	`IO_0_34`, `IO_L10P_T1_34`	`ETH_MDIO`, `ETH_MDC` (or Bank `14/15` `3.3 V` NC pins)	`LVCMOS25` (check `RTL8211FSI` `DVDD_RG`/`VIO` if `2.5 V` or `3.3 V`; if `3.3 V`, use Bank 14/15 NC balls e.g. `K12, M15, K13, L13`)

Wait-free `3.3 V` single-ended control pins for `U1201` (`ETH_MDC`, `ETH_MDIO`, `ETH_RST_N`, `ETH_INT_N`) are also available in **Bank 14 (`10` free balls: `K12, M15, L14, M14, K13, L13, M12, R12, T12, P6`)** and **Bank 15 (`8` free balls: `E16, F15, E15, H11, H12, H13, G14, F14`)**, removing `Rev05`'s strap-only unmanaged PHY limitation!

Putting `ETH_SGTX/SGRX` in **Bank 34 Tile `T1` (`R2/R1, R3/T2`)**:

1. Restores **`LINK_RX_D0` (`L4/M4`)** and **`LINK_TX_D0` (`M16/N16`)** cleanly back to `J8 / IAS1`.
2. Removes all four `C1218–C1221` assembly stubs (`LINK_TX_D0` recovers `+34–41 mV` eye from `477–484` back to `518 mV`).

3. Eliminates the `5.2 mm @ 0.17 mm` `L1` parallel between `ETH_SGTX_PHY` and `LINK_RX_D1_N`.
4. Note on Bank 34 `IDELAYE2`: `XC7A50T` supports `IDELAYE2` + `IDELAYCTRL` in Bank 34 (just like Bank 14), driven from the same shared `200 MHz REFCLK BUFG`, so RX `ISERDESE2` + `IDELAYE2` in Bank 34 works identically to our Bank 14 PoC.

4.2 Artix-7 Package GTP Transceiver Audit (`DS181` & Vivado `get_parts` / IBIS `.pkg`)

Package	Total Pins	XC7A50T GTP Transceivers (Quad 216)	Verified Source
FTG256 (current 17×17 mm, 1.0 mm)	256	**0 (none bonded)**	Vivado `xc7a50t_ftg256.pkg` (`MGT_lines = 0`), `get_parts xc7a50tftg256-2`
CSG324	324	**0 (none bonded)**	Vivado `xc7a50t_csg324.pkg` (`MGT_lines = 0`), `get_parts xc7a50tcsg324-2`
CPG236	236	**2 GTP lanes** (`MGTPRX0..1 / MGTPTX0..1`)	Vivado `xc7a50t_cpg236.pkg` (13 MGT pins), `get_parts xc7a50tcpg236-2`
CSG325	325	**4 GTP lanes** (`MGTPRX0..3 / MGTPTX0..3`)	Vivado `xc7a50t_csg325.pkg` (23 MGT pins), `get_parts xc7a50tcsg325-2`
FGG484	484	**4 GTP lanes** (`MGTPRX0..3 / MGTPTX0..3`)	Vivado `xc7a50t_fgg484.pkg` (23 MGT pins), `get_parts xc7a50tfgg484-2`

Per `DS181 Table 52`, Artix-7 GTPs run `0.500–6.25 Gb/s` on `-2` (`3.75 Gb/s` on `-1`), with `1250 Mb/s` Gigabit Ethernet jitter limits in `Table 59`. However, switching from `FTG256` to `CSG325` (`0.8 mm` pitch) or `FGG484` requires re-fanout of the entire BGA, adding **`1.0 V MGTAVCC`** and **`1.2 V MGTAVTT`** linear/filtered supplies and a dedicated differential `125 MHz MGTREFCLK`, unnecessary when Bank 34 `LVDS_25` SelectIO already achieves `1.25 Gb/s` SGMII cleanly on **`XC7A50T-2FTG256I`**.

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5. Verdict Table Across Operating Modes

Mode / Hardware Config	Uplink (A→K) Capacity	Downlink / Control (K→A)	Redundancy & Failover Loss	PCB / BOM Impact	Recommendation
1. **`IAS1` Only (`Rev05` default)**	**`1.94 Gb/s`** (`1.0G`×2) / **`2.42 Gb/s`** (`1.25G`×2)	**`~0.49 Gb/s`** (`LINK_TX_D0`) + SPI if Pmod wired	None (single `J8` connector)	`C101, C102, C107, C108` fitted (`C1218-21` DNP)	**Best baseline** for pure raw radar/SDR streaming
2. **`Rev05` ETH Only (`LINK_RX_D1` static)**	**`~0.99 Gb/s`** (`9000 B` jumbo UDP)	**`~0.99 Gb/s`** UDP control (or Pmod cable `J2`)	None (single `RJ45` path)	Fit `C1218-21`, remove `C101..102, 107..108`	**Use for switch/network integration** (`DECIM≥4` radar + telemetry)
3. **`Rev05` Dual `IAS1` `D1` + ETH (Load-Balanced)**	**`~1.94 Gb/s`** (`1.0G`+ETH) / **`~2.18 Gb/s`** (`1.25G`+ETH)	**`~0.99 Gb/s`** (ETH UDP) + optional Pmod `J2` / slow `LINK_TX_CLK`	**Active-backup or stream split:** survives either `J8` `D1` or `RJ45` failure at `~0.95–1.19 Gb/s` degraded rate	Same `ETH` BOM; activate `LINK_RX_D1` (`~0.8%` 3D NEXT safe)	**Best `Rev05` multi-sensor mode** (Radar on `D1`, SDR+Ctrl on `ETH`)
4. **`Rev05` 1+1 Hitless Mirroring**	**`~0.95 Gb/s`** effective (duplicated on both)	**`~0.99 Gb/s`** (`ETH`) + `J2`/`LINK_TX_CLK`	**`0` packet loss** on instant fault via `seq_num` deduplication	Same `ETH` BOM	**Best for critical reliability** (`<= 0.95 Gb/s` streams)
5. **`Rev05` `100 Mb/s` Fallback (`-1` or noisy link)**	**`~1.05–1.29 Gb/s`** (`D1` + `100M` ETH)	`100 Mb/s` (`~11.8 MB/s`) UDP control	Survives `D1` fault with `100 Mb/s` degraded telemetry	Same `ETH` BOM (`10×` SGMII oversampling)	**Fallback** if `-1` silicon ever substitutes `-2`
6. **`Rev06` Dedicated Bank 34 ETH (`R2/R1`, `R3/T2`)**	**`~2.93–3.41 Gb/s`** (`2×` `IAS1` + `1G` ETH)	**`~0.49 Gb/s` `IAS1` + `~0.99 Gb/s` ETH (dual path)**	**Full A→K and K→A link-level + connector redundancy** (`0`-loss mirroring or `3+ Gb/s` split)	Future spin only: move `U1201` to free Bank 34 pins + `MDIO/MDC` on Bank 14/15; keep `FTG256-2`	**Recommended `Rev06` hardware improvement**

Source: sw/README.md

KV260 PS Software Bring-Up (`sw/`)

Host/target userspace test utilities and Linux devicetree overlay for the KV260 Zynq UltraScale+ PL bitstream (`fpga/kria/bd.tcl` + `fpga/kria/kria_pl_link.v`).

Files

- `ias2rf_pl.dtsi`: Device Tree overlay fragment for Ubuntu/PetaLinux (`xmutil` or `configfs` DT overlay), exposing:
- `ias2rf_link@80000000` (`kria_pl_link` AXI4-Lite CSRs `0x00..0x34`, interrupts `irq_fpga` / `irq_link_up`)
- `axi_dma_0@80010000` (Direct-register 64-bit AXI DMA S2MM uplink + MM2S downlink)
- `ias2rf_pps@80020000` (`kria_pps`, GPS PPS capture and generator, interrupt `pps`) and the `rpu_mailbox` reservation at `0x3EE00000` for R5F core 0
- `i2c0` (EMIO I2C to Artix/board `HK_SCL`/`HK_SDA`)
- `spi0` (EMIO SPI over KV260 Pmod J2)
- `uart1` (EMIO UART to the front-end FPGA's debug console over the two Pmod spare lines: `/dev/ttyPS1`, 115200 8N1; `screen /dev/ttyPS1 115200` shows the boot banner and the 1 Hz `STAT` line, and `h` lists the commands, **FPGA_GATEWARE §5.4**)
- `ias2rf_dma_test.c`: Standalone C smoke test (`mmap` `/dev/mem` + optional `u-dma-buf` `/dev/udmabuf0`):
- Prints all IAS1 link CSRs (`0x00..0x34`) and flags `0xDEAD_C10C` if the Artix `LINK_RX_CLK` is not yet running.
- Supports `--retrain` (pulses `LINK_CTRL[2]`) and `--rd-adcs` (sends a Stream `0x10` register-read request for Artix `0x0038` `ADCS_STATUS` via `MM2S`, then captures one `kria_ps_framer` block via `S2MM`, up to 69,648 bytes, and lists its first packets: stream id, sequence number, length and PL time; **FPGA_GATEWARE §5.10**).
- Artix registers through the same command channel: `--rd ADDR`, `--wr ADDR VALUE`, and for the radar path `--radar-en 0|1` (`RADAR_CTRL[0]`, `0xE4`) and `--radar-status` (`RADAR_STATUS`, `0xE8`; bit 5 is "link up and ADC trained"). Since Rev08 these replace the two Pmod spare GPIOs, which now carry the debug UART.
- **`kria/`**: Rust for the K26's processors: `kria-core` (shared, `no_std`), `kria-vehicled` (A53: engine data from opendash), `kria-r5f0` (R5F core 0: GPS PPS discipline, IAS1 link watchdog, transmit lock) and `kria-r5f1` (R5F core 1: radar beam scan and the PL fusion grid).
- **`hmi/`**: the in-car screens (**docs/HMI.md**).
- **`integrations/`**: simulations and figures for **docs/INTEGRATIONS.md**.

Build & Run on KV260 (Linux)

```
gcc -O2 -Wall -o ias2rf_dma_test ias2rf_dma_test.c
sudo ./ias2rf_dma_test
# Optional DMA S2MM + Artix register-read roundtrip (with u-dma-buf loaded):
sudo modprobe u-dma-buf udmabuf0=1048576
sudo ./ias2rf_dma_test --rd-adcs
sudo ./ias2rf_dma_test --radar-status       # read-back arrives in the S2MM capture
sudo ./ias2rf_dma_test --radar-en 0         # radar DDC off
```

Source: docs/HMI.md

In-car HMI: the screens, their software and the processing partition (Rev08)

17 November 2026, rewritten 18 November for the real application · built and run on a PC against the simulated board; not yet run on a KV260

These are the screens that drive and display the whole system on a touchscreen in the car. They cover this board's functions (receiver, spectrum, ADS-B, radar, transmitter, system health) and the vehicle integrations analysed in **INTEGRATIONS.md** (vehicle telemetry, GPS, a KrakenSDR and a HackRF Pro). The document also says which part of the K26 does each job.

The screens are a real application, not mock-ups. Every image below is drawn by that application from the snapshot its data service produces. On a PC the data service runs a simulated board: it generates the same DMA blocks, in the same formats, that the PL sends (§4), and every decoder behind the screens is the one that would run on the KV260. The RDS text, the aircraft, the radar detections and the interlock states in the images are decoded from those blocks, not typed in.

Sources: `sw/kria/hmi-core` (the data plane), `sw/kria/hmid` (the data service), `sw/hmi/app` (the screens). `sw/hmi/make_images.sh` regenerates the images below; `sw/kria/README.md` has the build and run commands.

1. Display path on the KV260

Item	What the KV260 has	Source
Video outputs	HDMI (`J5`) and DisplayPort (`J6`) on the carrier	UG1089 Interfaces table `[V]`
Who drives them	**Both come from the PS DisplayPort controller.** Two PS-GTR lanes (`GTR_DP0`, `GTR_DP1`) go to an `STDP4320` DisplayPort hub on the carrier, and the hub drives the DP connector and the HDMI connector	KV260 carrier schematic XTP682 rev 2, pages 10 to 12 `[V]`
GPU	Mali-400 MP2 in the PS (OpenGL ES 2.0)	K26 data sheet `[V]`
Video codec	VCU, H.264 / H.265, a hard block on the PL side; using it means adding its wrapper to the block design	K26 data sheet `[V]`; PL cost not yet measured `[E]`
Touch	A USB touchscreen controller (HID) on one of the four USB 3.0 ports	`[E]`, any car display with USB touch

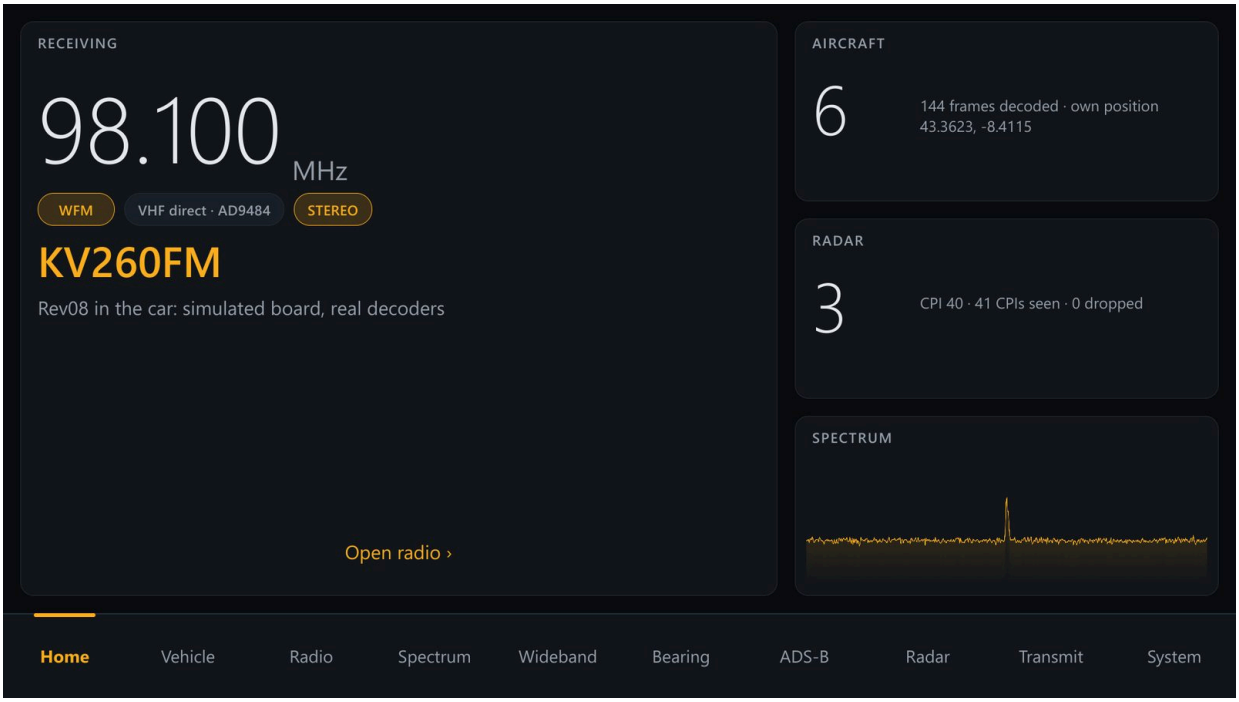
The PL is therefore **not in the display path**. The screens are drawn on the A53s and shown through Linux DRM/KMS with no desktop: Slint's `linuxkms` back end opens the display directly. It can draw with the Mali-400 (`femtovg`, OpenGL ES 2.0) or entirely on the CPU (Slint's software renderer, which needs no GPU driver). The design size is 1280 × 720, which suits 7 to 10 inch car displays. On a 1920 × 1080 panel the same layout scales by 1.5, which is how the images below are drawn.

2. Design rules

- **Glanceable while driving.** One main number per card, in 48 to 96 px figures. Every touch target is at least 56 px, and the bottom bar is 88 px.
- **Night theme by default.** The ground is near-black and text is light grey with at least 4.5:1 contrast. A single amber accent marks the selected item and alerts. Spectra and maps use a dark-to-amber colour scale, so a strong signal is bright and the background stays dark.
- **Transmit is locked while the vehicle moves**, and also while the licence flag is not set. The screen only asks: R5F core 0's interlock decides, and it alone sets `TX_KEY` (§5). Vehicle speed comes from the vehicle's CAN 2.0 bus on R5F core 1 or from the `opendash` stream, with GPS as the fallback (**INTEGRATIONS.md §2.2, §4**). Transmitting with home-built equipment needs an amateur licence and stays inside the amateur bands.
- **The same bottom bar on every screen:** Home, Vehicle, Radio, Spectrum, Wideband, Bearing, ADS-B, Radar, Transmit, System. Ten items of 128 px each at 1280 px.
- **A lost data service is shown, not hidden.** If the screens stop receiving snapshots, a red "No data from kria-hmid" banner covers the top of every screen until they return.

3. The screens

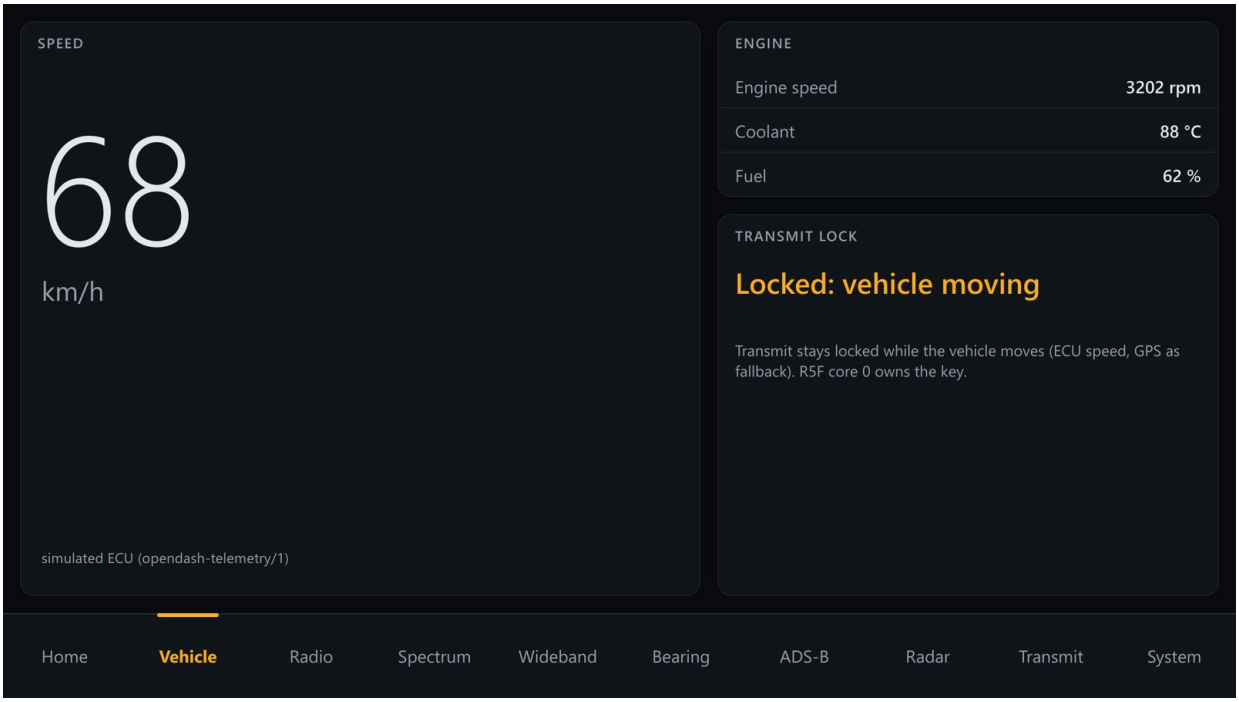
3.1 Home



HMI home screen

What is being received (frequency, mode, the converter it comes from, stereo, the RDS name and text), the aircraft and radar counts, and a spectrum thumbnail. "Open radio" opens Radio.

3.2 Vehicle



HMI vehicle screen

Speed, engine speed, coolant and fuel from the ECU stream (`opendash-telemetry/1`, **INTEGRATIONS.md §4**), and the transmit lock's state and reason as the interlock reports it. Shown: driving at 68 km/h, so transmit is locked.

3.3 Radio



HMI radio screen

Frequency with large step buttons, the five demodulator modes of `kria_channel_rx` (AM, USB, LSB, NBFM, WBFM), the signal meter with the audio level and rate, and the pilot and CTCSS flags from the audio stream. The RDS card shows the station name, RadioText, PI, PTY and the group count, decoded on the A53s from the RDS bits the PL sends with the audio (`kria_hmi_core::audio`, CRC and offset words A to D). The presets cover FM broadcast, HF AM, airband, marine channel 16, a 2 m repeater with CTCSS, PMR446 and 20 m SSB. A frequency and mode becomes the register writes of the G-8 cases (`kria_hmi_core::modes`): the DDC's NCO, the channel's decimation and mode, the front end's switches and amplifiers, the RFFC5072 LO above 300 MHz (direct `30–170 MHz`, `170–300 MHz` not covered). Shown: 98.1 MHz WBFM, stereo, with the simulated station's RDS.

3.4 Spectrum



HMI spectrum screen

The stream the radio is tuned on (HF A or B from the AD9253, or VHF/UHF from the AD9484), as a spectrum and a 60-row waterfall. The FFT (2048 points, Hann window) runs on the A53s on the stream's I/Q. A touch on the trace sets the marker; "Listen at marker" retunes the radio there. "Record IQ" writes the stream to the SSD as interleaved 16-bit I and Q (`.cs16`,

which GNU Radio, SDR# and inspectrum open), with a `.json` beside it giving the centre frequency, sample rate and stream. Checked on the simulated board: one second recorded at 98.1 MHz holds the station 64 dB above the noise at the centre.

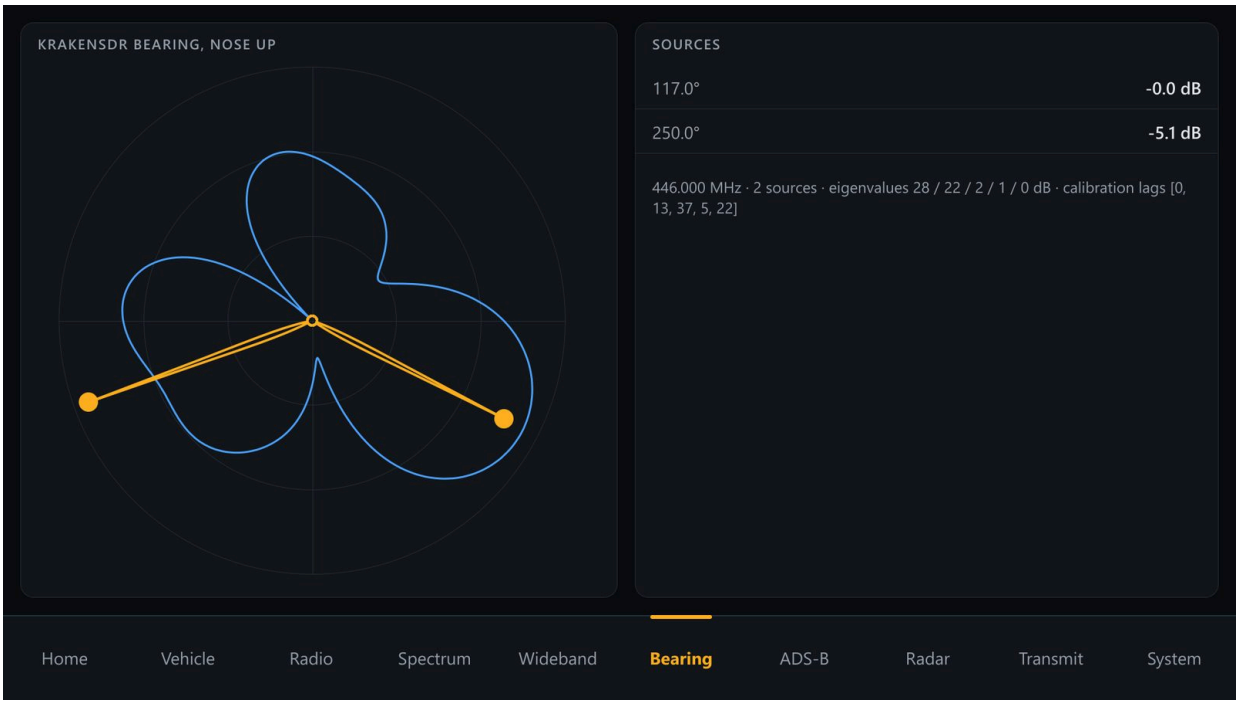
3.4a Wideband (HackRF Pro)



HMI wideband screen

One sweep of a HackRF Pro from 0 to 7.2 GHz (**INTEGRATIONS.md §10**): the band this board covers shaded green, what the HackRF adds shaded blue, the signals `kria-sdrd`'s detector found marked at the top, and the strongest of them listed. The trace is the maximum per MHz of `kria_sweep`'s 78 kHz bins; bins the sweep has not reached hold the last swept value. Shown: the end-to-end run's output, 25 signals of a car's radio environment.

3.4b Bearing (KrakenSDR)

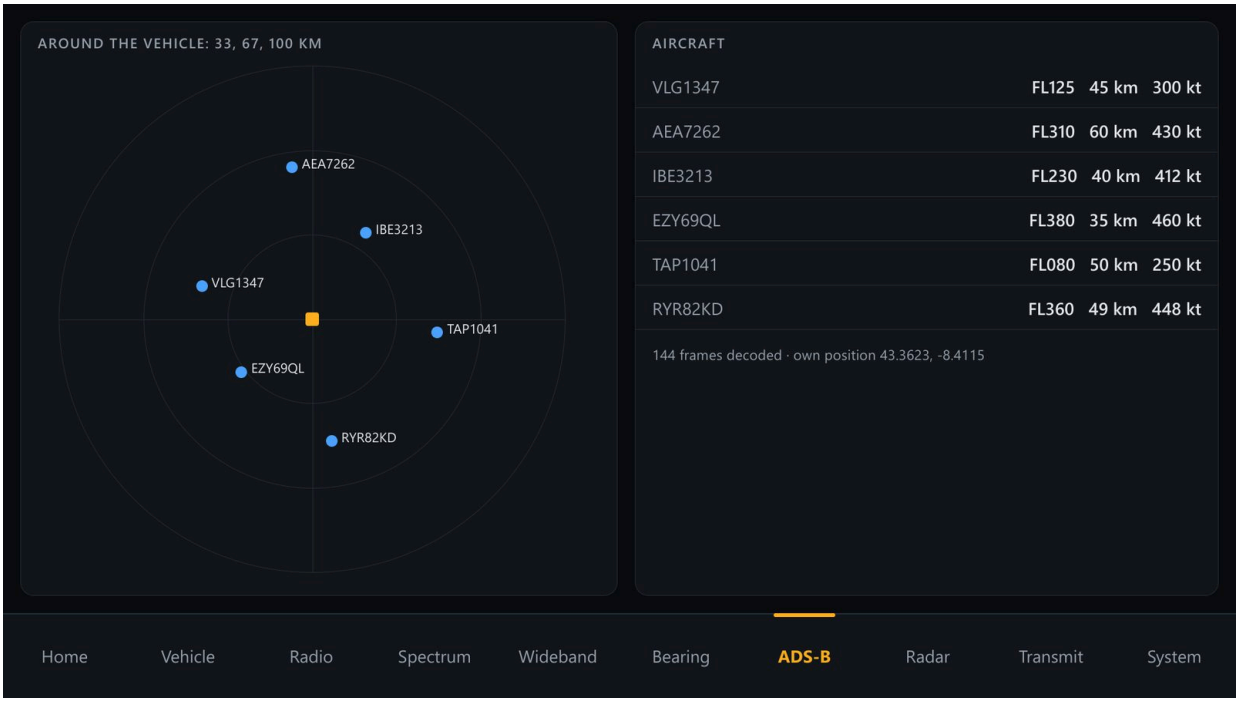


HMI bearing screen

Direction finding with a KrakenSDR (**INTEGRATIONS.md §9**): a polar plot with the vehicle's nose up and bearings clockwise, the Bartlett spectrum from `kria_doa` in blue and the MUSIC spectrum in amber, each source as a dot at the tip of

its MUSIC peak, the sources with their bearings and powers, R's eigenvalues and the calibration lags. Shown: the end-to-end run's output, two emitters at 446 MHz.

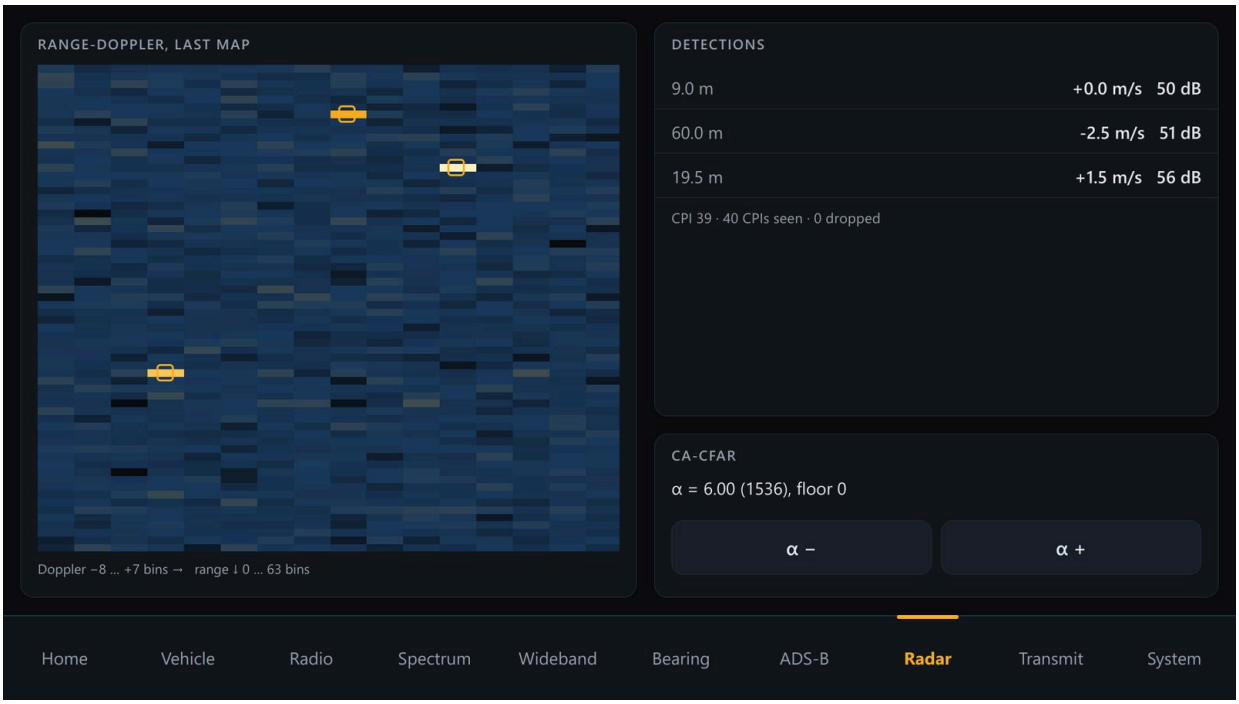
3.5 ADS-B



HMI ADS-B screen

A polar view around the vehicle with 33, 67 and 100 km rings, and the aircraft list (callsign, flight level, range, speed). The PL demodulates the frames and checks their CRC (`kria_adsb_rx`, stream 0x21); the A53s decode identity, altitude, velocity and position (`kria_hmi_core::adsb`: CRC-24, CPR global and local decoding, checked against the published test vectors). **Ranges and bearings need the vehicle's own position**, which comes from the USB GPS (**INTEGRATIONS.md §2**). Shown: six aircraft, 144 frames.

3.6 Radar

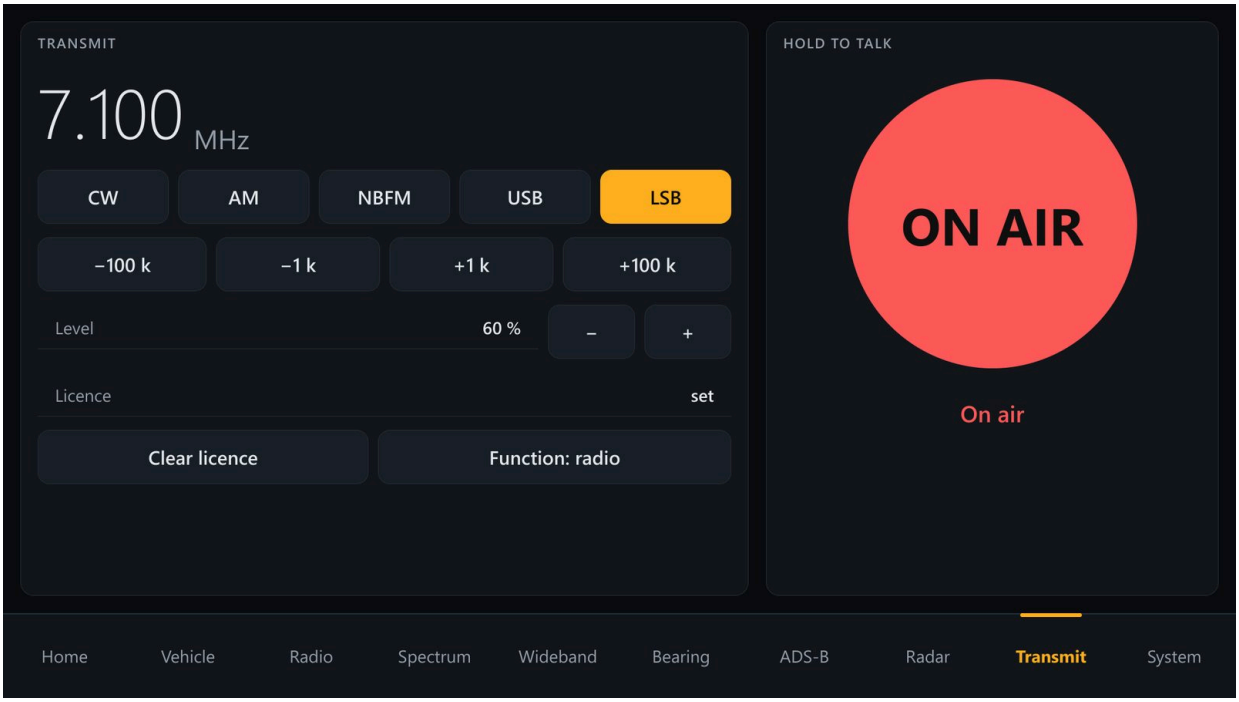


HMI radar screen

The last 64 × 16 range-Doppler map (stream 0x23, sent every fourth CPI), with the CA-CFAR detections outlined, and the

detection list (stream 0x22) with range, radial speed and power. α − and α + step `RADAR_ALPHA` by 1.0. Shown: three targets at 9, 19.5 and 60 m.

3.7 Transmit



HMI transmit screen

Carrier, the five modes of `kria_tx_mod` (CW, AM, NBFM, USB, LSB; `DSP_CTRL[12:10]`), frequency steps, level, the licence flag, and a large hold-to-talk button. **The board transmits on HF only:** `kria_tx_mod` puts the carrier inside the 25 MS/s stream to the AD9767, out of `J952`, so the carrier must stay below 12.5 MHz. Above that the request is not passed on and the screen says why. VHF and UHF transmit goes through the HackRF Pro's gate (**INTEGRATIONS.md §10**). The modulation source is a 1 kHz test tone. Shown: 7.100 MHz LSB, parked and licensed, keyed.

3.8 System

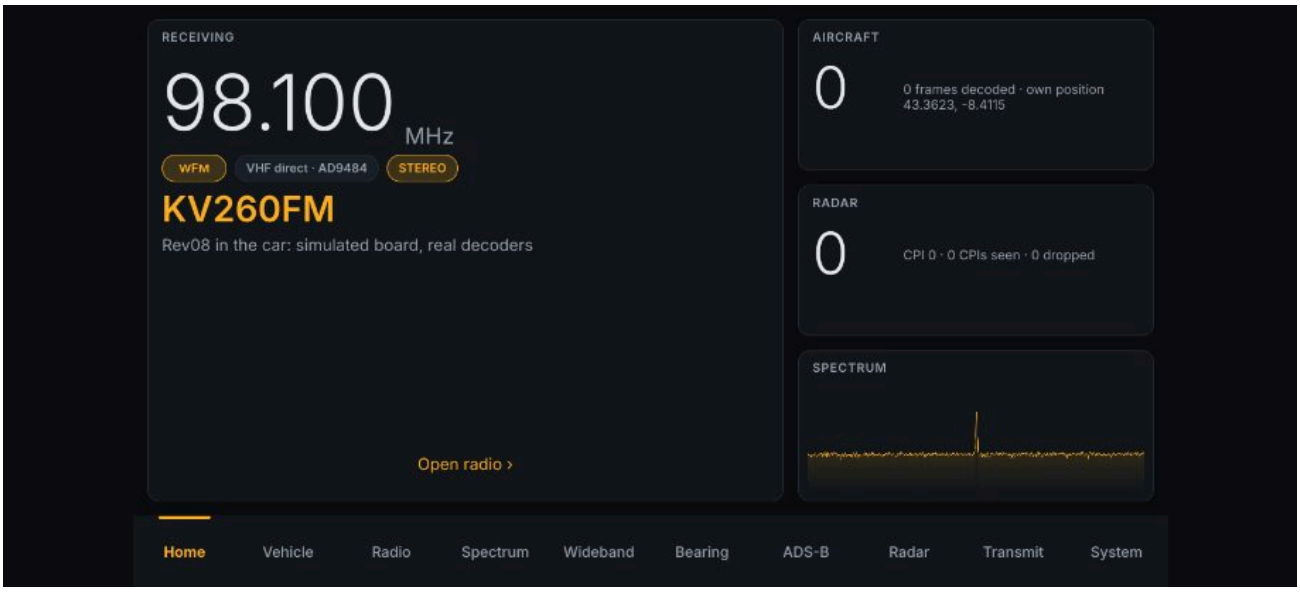


HMI system screen

The IAS1 link, the packet and block counts, sequence gaps and CRC errors on the PL's result stream, the stream rate into

the A53s, the K26 and Artix temperatures, both R5F cores' status, the platform, and the I/Q recording. The function card chooses what the PL's DSP suite runs: the receiver, ADS-B at 1090 MHz, or the radar. The suite runs one function at a time on the one front end.

3.9 In a browser or on a phone



The screens in a phone's browser, landscape

The same application, compiled to WebAssembly, runs in a browser. `kria-hmid --www` serves it on the same port as the snapshots, so a phone on the car's network opens `http://<KV260>:8080/` and gets every screen with live data and working controls. The 1280 × 720 layout is scaled to fit the browser; landscape is the intended orientation. Shown: headless Chrome at a phone's 915 × 412.

4. The software

Part	Where it runs	What it does
PL result path (`kria_dsp_out`, `kria_ps_framer`)	K26 PL	The DSP suite's results as streams: audio with the pilot, CTCSS and RDS flags (0x20), ADS-B frames (0x21), radar detections with a CPI summary (0x22), range-Doppler maps (0x23), enabled by `DSP_CTRL[14]`, maps every 2^`DSP_CTRL[18:15]` CPIs. `kria_ps_framer` merges them with the link's I/Q streams into 64 KiB blocks for `axi_dma_0` (S2MM); every packet has a header word (magic 0xA5, stream id, flags, length, sequence number) and the PL clock's 64-bit time. A flush packet closes a block after 1 ms without data. Tested in `tb_kria_ps_framer` (798 of 798 packets, 136 blocks); see **FPGA_GATEWARE.md**
`kria-hmi-core` (Rust, no I/O)	anywhere; tested on a PC	Parses the blocks (sequence gaps, CRC flags), decodes audio and RDS, ADS-B, radar detections and maps; the spectrum and waterfall; turns a frequency and mode into register writes (the G-8 channel words, the front end, the RFFC5072); holds the snapshot and applies the screens' commands. 18 host tests
`kria-hmid` (Rust)	A53, Linux (`--features hw`); a PC with the simulated board	Each 20 ms takes the DMA blocks (`/dev/mem` and `/dev/udmabuf0`), plays the audio through ALSA, writes the registers (the K26's directly, the Artix's through the link's command stream 0x10), records I/Q, and every 100 ms sends the snapshot over WebSocket. Asks R5F core 0 for transmit through `/run/kria-hmi/tx`, which `kria-vehicled` puts in the mailbox; it cannot key transmit via `DSP_CTRL` (`DSP_CTRL[1]` is read-only and mirrors `TX_KEY[0]`). Serves the browser build
`kria-hmi` (Rust and Slint)	A53 (Linux KMS), a PC, a browser (WebAssembly)	The ten screens. Draws each snapshot, sends the commands. The traces and maps are rasterised in Rust into images, which Slint's renderers then only scale

Why Slint. The screens' requirements were a Rust core, low resource use, one code base for the car, a PC, a phone or a web page, and a clean modern look that is easy to change. Slint compiles its `.slint` markup into Rust, runs without a desktop on Linux KMS, has a software renderer for when the GPU driver is not available, and builds for WebAssembly. Qt Quick and Compose Multiplatform were the alternatives; both bring a larger runtime (a C++ or JVM one) and neither shares the Rust core as directly.

Licence. The screens' source in this repository is MIT, like the rest of `sw/kria`. A built `kria-hmi` binary links Slint, so it is distributed under Slint's terms: on an embedded device such as the KV260 that is the GPL-3.0, which means whoever ships such a binary also offers its source. `kria-hmi-core` and `kria-hmid` do not link Slint. Nothing from Slint is stored in this

repository.

Measured on a PC against the simulated board (`scenes/tour.jsonl`, 59 s of simulated time): FM with RDS "KV260FM" and its RadioText, the 2 m repeater's CTCSS, six aircraft, three radar targets, transmit blocked while driving and keyed once parked and settled, 205,098 packets in 2,949 blocks with 0 sequence gaps and 0 CRC errors. The native build, the headless renderer and the browser build were run; the `aarch64` build with `--features hw` compiles but has not run on a KV260.

5. Processing partition

Unit	Jobs	Why there
PL (`kria_pl_link`, `kria_dsp_suite`, `kria_dsp_out`, `kria_ps_framer`, `kria_bev_axi`, `kria_doa`, `kria_sweep`)	Link, packet streams, channel demodulation with RDS bits, ADS-B demodulation and CRC, radar FFT and CFAR, transmit modulation, the result streams and the blocks for the DMA, the fusion grid (**INTEGRATIONS.md §6**), the KrakenSDR's covariance and Bartlett scan, the HackRF's sweep FFT (§9, §10)	Fixed rates up to 100 MS/s per stream, one sample per clock
A53 × 4 (Linux)	`kria-hmid` and the screens: RDS, ADS-B position decoding, the spectrum and waterfall, audio, recording; the telemetry client (`kria-vehicled`); LiDAR driver and SLAM; the Ethernet and USB devices; `kria-sdrd`: the KrakenSDR's calibration and MUSIC, the HackRF's panorama and transmit gate	General-purpose code, drivers and the display
R5F core 0	1 kHz loop, **written** (**`kria-r5f0`**, Rust): the GPS PPS discipline of `kria_pps`, the watchdog on the IAS1 link (retrain with a back-off), and the transmit interlock (vehicle speed from CAN1 or `opendash`, licence, time-out, link up), which owns `TX_KEY` (`0x8000_0038`). The AGC needs no core: it runs in the Artix fabric (`fe_agc`)	Must keep running when Linux is busy or restarting; deterministic latency
R5F core 1	10 kHz loop, **written** (**`kria-r5f1`**, Rust): the 10.5 GHz radar's beam scan, one step per CPI with a longer dwell where there are detections, `BEAM_STROBE` into the Artix's scan mode; the fusion grid's only command writer (its detections and Linux's ring) and its frames; PS `CAN1` (`0xFF07_0000`, EMIO to `J9` pins 6 and 8) reading the vehicle's CAN 2.0 bus for road speed and raw frames (**INTEGRATIONS.md §2.2**)	Timing tied to the CPI, about 0.4 ms, and CAN polling independent of Linux
Mali-400	The screens, when Slint draws with `femtovg`	OpenGL ES 2.0
VCU	H.265 recording of the screens or of a camera on IAS0	Hardware encoder; costs nothing on the A53s

The software on all these cores is Rust, with the logic in I/O-free crates (`kria-core`, shared by the A53s and the R5Fs, and `kria-hmi-core`) that are tested on a PC (**INTEGRATIONS.md §7**). The two R5F cores can reach the PL's control registers directly. `bd.tcl` already places `kria_pl_link`'s AXI-Lite slave and the DMA's registers on `M_AXI_HPM0_LPD`, in the low-power domain where the RPU sits, so no FPD path is involved. Linux starts and stops the R5F firmware through remoteproc `[E]` and talks to it through a fixed mailbox in reserved memory, stamped with the PL clock both read (`kria_core::mailbox`).

Register ownership: core 0 owns `kria_pps`, the link's retrain bit and the transmit enable (`TX_KEY` at `0x8000_0038`); core 1 owns `BEAM_STROBE`, PS `CAN1`, the grid's command port and its DMA; Linux (`kria-hmid`) owns tuning, modes, streams, the AGC's thresholds and the front end's sequencing. The Artix registers are reached only through the link's command stream, which Linux's DMA carries. The earlier `DSP_CTRL` race is gone: `TX_KEY` sits at its own register offset `0x38` on `pl_clk_100m`, writes take effect only with `24'h4B4559` (`"KEY"`) in `[31:8]` and full byte strobes, and `DSP_CTRL[1]` (`0x40`) is now a read-only reflection of `TX_KEY[0]`, so whole-register writes to `DSP_CTRL` from `kria-hmid` cannot key or clear the transmitter (verified by `tb_system.v` S7 and its mutation `tx_key_from_dsp_ctrl`). Core 0 clears `TX_KEY` on every panicking or unready path even when the IAS1 receive clock is absent. The Zynq's PS `CAN1` controller (classic CAN 2.0 in the low-power domain) is now routed through EMIO (`can1_txn` on `J9` pin 6, `can1_rx` on `J9` pin 8) to the adapter's `TCAN3403` transceiver circuit, so R5F core 1 reads the car's road speed even when Linux or Wi-Fi is down (**INTEGRATIONS.md §2.2**). The 77 GHz imaging radar still needs its own CAN FD adapter or 100BASE-T1 converter (§3).

6. What is left

- **On a KV260:** run `kria-hmid --hw` with the rebuilt PL (the framer and the result streams), the `udmabuf` buffer and ALSA, and the screens on KMS with a USB touchscreen. Nothing of the HMI has run on the board.
- **Not on the screens yet:** the fusion grid and the 77 GHz radar's objects (the Vehicle screen shows the ECU values only), the radar's beam controls, logging a bearing with the GPS position for triangulation, a microphone as the transmit source, and a transmit time-out shown on the screen (the interlock already has one).
- **Usability on the road:** the 56 px minimum and the contrast are design values. They have to be checked on a real display in daylight and at night.

Source: docs/INTEGRATIONS.md

Possible integrations: GPS, 77 GHz radar, vehicle telemetry, LiDAR, fusion on the PL, KrakenSDR and HackRF Pro

17 and 18 November 2026 · analysis, simulation and end-to-end tests on the bench; no vehicle hardware yet

Six devices could be connected to the KV260 alongside this board in the owner's vehicle (a Mitsubishi Montero V80, **VEHICLE_PLATFORM.md**):

- a USB GPS;
- a 77 GHz automotive radar through a CAN-to-USB adapter;
- the engine's live data through opendash, or straight from the car's CAN 2.0 bus on KV260 `J9` (§2.2, §4);
- a 3D LiDAR on a USB-to-Ethernet adapter;
- a KrakenSDR, five coherent receivers for direction finding (§9);
- a HackRF Pro, a transceiver from 100 kHz to 7.1 GHz with a fast sweep (§10).

None of them needs a change to this board. This document gives each one's link, data rate and processing, what it adds to the system, and the simulations and tests behind the numbers. Five pieces are built and tested end to end:

- the GPS's pulse-per-second on a free PL pin, disciplined by an R5F core (§2);
- the engine's live data from opendash into a daemon on the A53s, which feeds the transmit lock on the R5F (§4);
- a fusion grid in the PL that combines the LiDAR and the radars into one occupancy grid, in the K26's block design with its own DMA, fed by R5F core 1, which also scans the board's 10.5 GHz radar beam by beam (§6);
- the KrakenSDR's bearings, with the covariance and the Bartlett scan in the PL and MUSIC on the A53s (§9);
- the HackRF Pro's sweep from 0 to 7.2 GHz through an averaging FFT in the PL, and its transmitter behind the board's transmit lock (§10).

The software that runs on the K26's processors is in Rust, with its logic in one I/O-free crate shared by the A53s and the R5F cores (§7). **HMI.md** shows the screens that display all of it.

1. Summary

Device	Link to the KV260	Data	Processing	Status
GPS receiver with PPS	USB (or UART) for position and time; its PPS on KV260 `J9` pin 12, a free PL pin	1 to 10 fixes/s; one pulse a second	PL: `kria_pps` timestamps it to 10 ns; R5F 0: disciplines the PPS sent to the front end	RTL bench and K26 build; loop simulated (§2)
77 GHz radar	Its own CAN FD bus (USB-CAN FD adapter), or 100BASE-T1 Ethernet through a media converter	Object list or detections at about 20 Hz; classic CAN is too small for either (§3)	A53 or R5F 1: decode; PL: into the grid	Bus load and fog performance simulated (§3, §6)
Engine live data and road speed (CAN / opendash)	The car's CAN 2.0 bus (`J9` pins 6 and 8 -> PS `CAN1` EMIO), or opendash on the phone (Wi-Fi)	Up to `1 Mbit/s` classic CAN 2.0 frames, or up to 40 identifiers at 100 Hz over Wi-Fi	R5F 1 (`CAN1`) or A53 (`kria-vehicled`); R5F 0: fresher speed into the transmit lock (`TX_KEY`)	Built (`G6`/`D6` placed in K26 BD), 7 host CAN tests and emulated opendash E2E; not run on a car (§2.2, §4)
3D LiDAR, Ethernet	USB 3.0 to Gigabit Ethernet adapter	0.2 to 1.3 Mpoints/s, 20 to 70 Mbit/s	A53: driver, SLAM; PL: occupancy grid	Fog performance simulated (§5, §6)
Fusion grid	Inside the PL	100 M cell updates/s	PL: `kria_bev_grid` behind `kria_bev_axi`; R5F 1: its commands, the 10.5 GHz scan, the frames	RTL bit-exact against its model, in the K26 build; end to end from R5F 1's code through the RTL (§6.1)
KrakenSDR	USB 2.0 (five RTL2832U behind its hub)	5 × 2.4 MS/s, 24 MB/s	A53: `kria-sdrd` (alignment, calibration, MUSIC); PL: `kria_doa` (weights, covariance, Bartlett)	End to end from USB transfers through the RTL to the Bearing screen (§9)
HackRF Pro	USB 2.0	Sweep: 1,220 blocks/s, 20 MB/s; stream: 20 MS/s	A53: `kria-sdrd` (panorama, signals, transmit gate); PL: `kria_sweep` (averaging FFT)	End to end from USB transfers through the RTL to the Wideband screen (§10)

The KV260's own Gigabit port (`J10`) already carries this board's Ethernet link, so the LiDAR needs the USB adapter. The four USB 3.0 ports take the GPS, the CAN adapter, the Wi-Fi adapter and the LiDAR's Ethernet adapter, with the

touchscreen on a hub or on the HDMI display's own USB. The KrakenSDR and the HackRF Pro are USB 2.0 devices (24 and 20 MB/s): with them, a powered USB 3.0 hub on one port carries the GPS, the CAN adapter and the touchscreen, and the KrakenSDR takes its own 5 V 2.4 A supply.

2. USB GPS

Role.

- **Own position.** ADS-B ranges and bearings need it. Positions are decoded with CPR: locally from one frame against the vehicle's position, or globally from an even/odd pair. Without a position the ADS-B screen can show the aircraft but no distance.
- **Time.** `chrony` with `gpsd` keeps the Linux clock on GPS time, which stamps recordings, radar CPIs and detections.
- **Heading and speed.** Used when the vehicle is not moving fast enough for the ECU speed to be useful. They are the fallback for the transmit lock (**HMI.md §2**).
- **Odometry.** It is weaker than wheel speed, but useful for the SLAM when the wheel signal is missing.

Limits of USB alone. A USB GPS has no pulse-per-second line. Its time over USB carries some milliseconds of latency and jitter `[E]`. That is enough for logs and ADS-B positions, not for the things below.

2.1 The PPS on a free PL pin

What the PPS is for.

- **The sample clock.** The front end already disciplines its `Si549` (the converters' clock) to the pulse on Pmod `PPS_SYNC`, through `hk_xadc_pps` on the Artix (**CLOCK_SPEC.md**). Until now that pulse was a PS GPIO toggled by software, with the timing of whatever Linux was doing. With the GPS second behind it, the oscillator's error goes from its own tolerance (tens of ppm, kHz at 100 MHz) to the GPS's, and every tuned frequency with it.
- **Absolute time stamps.** The link's packet time stamps count seconds on the same pulse (`kria_pl_link`), so recordings, ADS-B frames and radar CPIs carry GPS time to tens of nanoseconds. That is what ADS-B multilateration with other receivers needs, and what lines the radar's detections up with the vehicle's position.
- **A pulse that keeps going.** When the receiver loses its fix (a tunnel, a garage), the generated second carries on from the learnt frequency instead of stopping.

The pin. The KV260 has no free Pmod pin: `J2`'s eight lines carry the SPI, the beam strobe, `PPS_SYNC` and the debug UART. The Raspberry Pi camera connector `J9` is unused by this design, and one of its pins is wired straight to the SOM:

- **`J9` pin 12 is `HDA10`**, SOM240 `A16`, ball `J12`, bank 45 at 3.3 V `[V]`. The source is the KV260 schematic (XTP682 rev 2, page 13), with the ball from AMD's K26 board file `part0_pins.xml`.
- Pin 11 next to it goes through a reset supervisor and is not usable.

On the board (since 18 November). The receiver plugs into `J1503`, now a 6-way vertical JST-SH (BM06B-SRSS-TB, the plug goes in from above) on the adapter shared with the vehicle CAN (1: ground, 2: `CANL`, 3: `CANH`, 4: ground, 5: PPS in, 6: 3.3 V out through a 0.2 A PTC; expanded from 4 pins when the CAN tap was added, and made vertical the same day because a side-entry plug had no room in front of `J1502`, **LAYOUT §6.8**). The pulse passes an ESD diode and 100 Ω into a 74LVC1G17 Schmitt buffer, and the buffer drives two contacts of `J1502`, a 15-way 1 mm FPC receptacle: pin 12 and pin 4, through 220 Ω each. A 100 mm 15-way FFC joins `J1502` to the KV260's `J9` (STATUS sheet, **LAYOUT §6.8**).

Why two contacts: the two FFC types (contacts on the same side, or on opposite sides) reverse the order, pin *n* to pin 16 − *n*. Whichever cable is fitted:

- one copy of the pulse meets `J9` pin 12;
- the other copy meets `J9` pin 4, a ground, through its 220 Ω (15 mA while the pulse is high).

Only pins 7 and 9 are tied directly to ground on the adapter (pins 6 and 10 now feed the two NPN inputs of the mirror-safe CAN transmitter, §2.2). Adapter pins 7 and 9 land on `J9`'s ground on pin 7 and the unused MIPI pin 9 (or vice versa), and adapter pins 6 and 10 land on `J9` pin 6 (`can1_txn`) and `J9` ground pin 10. `J9`'s pins 11, 13, 14 and 15 (the reset supervisor, the I²C pair and 3.3 V) meet nothing in either case. So a wrong cable cannot harm the KV260, and either cable works. `[E: J9's ground pins are from the Raspberry Pi pinout; check with a meter before the first power-up]`

Any GPS module with a 3.3 V PPS output works, and it can share the USB link for its position and time.

`kria_pps` (**`fpga/kria/kria_pps.v`**) is an AXI-Lite slave at `0x8002_0000`:

- It timestamps each GPS edge on a 64-bit counter at `clk_pl_0` (10 ns). The pulse must first stay high for 1 µs, so a glitch is flagged and never captured.

- It measures the interval between edges and flags a missing pulse after 1.25 s.
- It generates its own second from a fractional period (32 + 32 bits), with a one-shot phase adjustment.
- It drives `PPS_SYNC` from one of three sources: the software GPIO (mode 0, the reset default, as before), the GPS pulse (mode 1) or the generated pulse (mode 2).
- It raises `pl_ps_irq0[4]` on each capture.

The register map is in **FPGA_GATEWARE.md §5.6**.

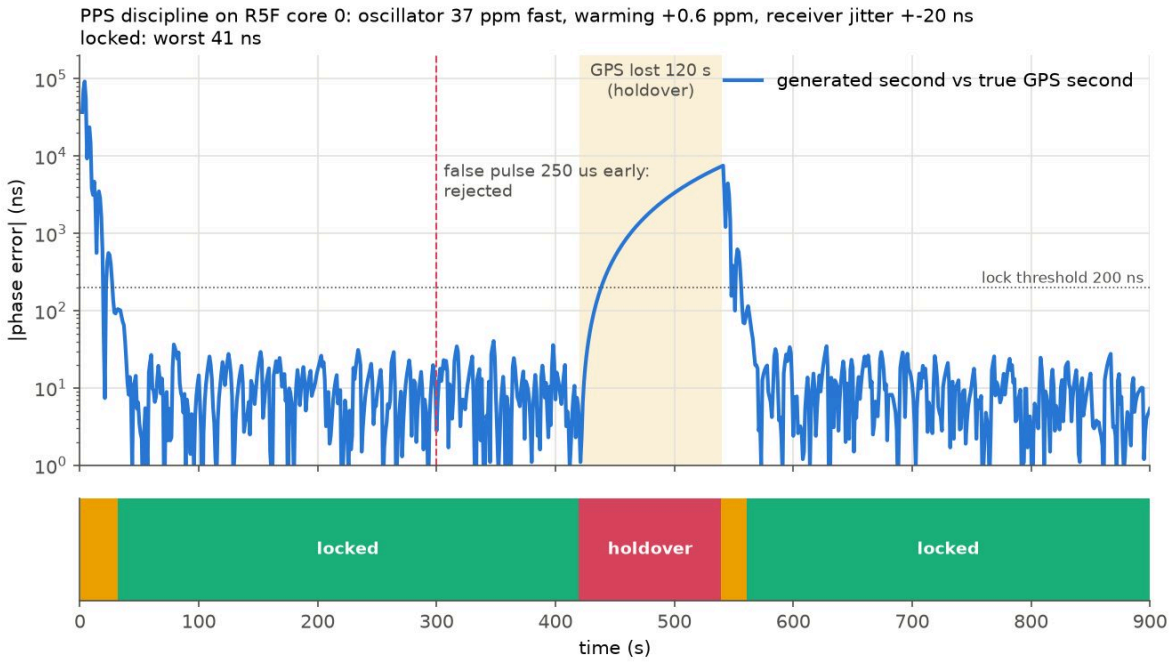
The loop on R5F core 0 (`kria_core::pps`, §7). Once a second it reads the GPS edge and the generated edge and computes three things:

- the frequency over a window of up to 1,024 s, which averages out the receiver's jitter;
- a phase correction of half the error;
- an integral term, which removes the lag of the windowed estimate while the oscillator warms up.

It rejects any interval more than 200 ppm off, or more than 2 µs off the estimate once locked. In holdover it changes nothing.

The simulation runs the same Rust code against a model of `kria_pps`, with:

- an oscillator 37 ppm fast that warms by 0.6 ppm over ten minutes;
- ±20 ns of receiver jitter;
- a false pulse 250 µs early;
- 120 s with no GPS.



PPS discipline

	Result
Locked after	31 s
Phase error while locked	41 ns worst, against the true GPS second
False pulse	rejected, lock kept
After 120 s of holdover	7.3 µs off, almost all of it the warm-up that went on during the outage
Locked again after the GPS returns	21 s

Without the integral term, the warm-up showed up as a constant 300 ns error. The simulation found it, and the term went in. Source: `cargo run --example pps_sim` in **`sw/kria`**; the figure is drawn by **`sw/integrations/kria_sw_figures.py`**.

Verification of the RTL. **`fpga/sim/tb_kria_pps.v`** runs with 10,000-tick "seconds", so a run covers dozens of them. It checks:

- the ID, mode 0 forwarding, and captures with the IRQ and its clearing;
- the capture period, and mode 1 forwarding after qualification;
- a 5-tick glitch: flagged, not counted, not captured, not forwarded;
- the missing flag and its clearing;
- the fractional generator: eight seconds of 10,000.25 ticks total 80,002;
- the one-shot adjustment;
- a closed loop shaped like the R5F's, which holds the generator within 1 tick of a GPS second of 10,000.37 ticks with ±1 tick of jitter;
- five seconds of holdover.

It passes, and the mutation `pps_no_filter` (no glitch filter) fails three checks. The bench also set a rule for the firmware: clear only the status bits that were read, or a capture that lands between the read and the clear is lost.

2.2 The vehicle's CAN bus on R5F core 1

Why. Reading road speed directly from the car's powertrain CAN 2.0 bus on R5F core 1 feeds the transmit interlock (`kria_core::interlock`) even when Linux, Wi-Fi or the phone (`opendash`, §4) is not running. The Zynq UltraScale+ PS controller (`CAN1` at `0xFF07_0000`, `UG1085` ch. 23) supports classic CAN 2.0 up to `1 Mbit/s`, which matches a car's powertrain or diagnostic CAN 2.0 bus (`250` or `500 kbit/s`). It does not support CAN FD, so the 77 GHz radar stays on its own USB CAN FD adapter or 100BASE-T1 converter (§3).

Where it connects. It shares the 15-way 1 mm FFC (`J1502` to KV260 `J9`, the unused IAS1 camera connector) and the expanded 6-way 1 mm vertical JST-SH `J1503` (`1`: `GND`, `2`: `CANL`, `3`: `CANH`, `4`: `GND`, `5`: `PPS`, `6`: `+3V3_D` through the `0.2 A` PTC) with the GPS PPS on the adapter (`_work/sheets/status_spec.py`; placed and routed, **LAYOUT §6.8**).

The two `J9` pins and the FFC mirror trick (`fpga/kria/bd.tcl`, `fpga/kria/xck26_bd.xdc`, `STATUS` sheet):

- **`CAN1` RX (`J9` pin 8):** `can1_rx` enters `J9` pin 8 (`CLK_N`, `SOM240_1 C13`, K26 ball `D6`, Bank 66 `LVCMOS12`, `PULLUP TRUE`). Pin 8 is the centre pin of the 15-way FFC (`16 - 8 = 8`), so it lands on `J1502` pin 8 with both straight and reversing FFC cables. On the adapter, `U1506` (`TCAN3403DDFRQ1`, `3.3 V` supply and VIO, `STB` grounded) drives `CAN_RXD` through a `1.8 kΩ / 1 kΩ` voltage divider (`R1556` / `R1557`, `3.3 V` to `1.18 V`, `2.8 kΩ` load) into `J1502` pin 8 because K26 Bank 66 runs at `PL_1V2` (`1.2 V`).
- **`CAN1` TX (`J9` pin 6):** In `bd.tcl`, `can1_tx_inv` inverts `ps8/emio_can1_phy_tx` to `can1_txn` on `J9` pin 6 (`DATA1_P`, `SOM240_1 A9`, K26 ball `G6`, Bank 66 `LVCMOS12`, `DRIVE 4`, `SLEW SLOW`), so `can1_txn` is `0 V` when recessive and `1.2 V` when dominant. A straight FFC lands `J9` pin 6 on `J1502` pin 6 and `J9` pin 10 (`GND`) on `J1502` pin 10; a reversing FFC swaps them. Only `J1502` pins 7 and 9 remain grounded directly on the adapter. Pins 6 and 10 each feed the base of an `MMBT3904` NPN (`Q1530`, `Q1531`) through `2.2 kΩ` (`R1551`, `R1552`) with a `4.7 kΩ` base-emitter pull-down (`R1553`, `R1554`). Their shared collectors drive `CAN_TXD` with a `2.2 kΩ` pull-up (`R1555`) to `+3V3_D`, implementing `CAN_TXD = NOR(pin 6, pin 10) = TX` regardless of cable direction.
- **Unconfigured fail-safe and bus protection:** While the K26 PL is unconfigured (pins floating or weakly pulled up), the `4.7 kΩ` base-emitter resistors hold both NPNs off so `CAN_TXD` stays high (recessive) and does not clamp the car's bus. `TCAN3403DDFRQ1` provides TXD dominant time-out protection and ±58 V bus fault protection (since the Rev08 audit; the TCAN330 of the first drawing stood only ±14 V, less than a CAN wire shorted to the battery). `CANH` and `CANL` go directly to `J1503` pins 3 and 2 behind an automotive CAN ESD diode (`D1531`, `PESD1CAN`) with **no termination resistor**, because tapping an existing vehicle bus must not add a third terminator.

Firmware and snoop mode (`sw/kria/core/src/can.rs`, `sw/kria/r5f/src/bin/core1.rs`, `sw/kria/r5f/src/bin/core0.rs`):

- At `100 MHz` `CAN1_REF_CTRL`, `can::bit_timing` uses `20` time quanta per bit (`1` sync + `16` prop/phase1 (`TS1 = 15`) + `3` phase2 (`TS2 = 2`), sample point at `85%`, `SJW = 3`, `BRPR = 100 MHz / (20 * bitrate) - 1`), supporting `125 kbit/s`, `250 kbit/s`, `500 kbit/s` and `1 Mbit/s`.
- Core 1 keeps `CAN1` in reset until Linux enables it through `CanConfig`. By default (`active = false`) core 1 puts `CAN1` in `MSR_SNOOP` (`0x04`, listen-only mode), so the board never sends `ACK` or error frames onto a vehicle bus unless `--can-active` is explicitly set.
- If Linux's heartbeat stops for `1 s`, core 1 stops the 10.5 GHz radar scan and occupancy grid (§6.1) but **keeps `CAN1` listening and publishing road speed**, so the transmit interlock stays armed with live bus speed.
- Core 0 reads both `CanStatus.speed` and `ToR5f.ecu` (`opendash`) and passes `can::fresher(bus, ecu)` to `Interlock::step`, selecting whichever speed measurement has the newer `kria_pps` PL tick stamp.

Mailbox layout and ring buffer (`sw/kria/core/src/can.rs`, magic `"KCN1"`):

Offset	Size	Name	Writer	Content
`0x0C0`	`64 B`	`CanStatus`	core 1	Controller state (`Off`, `Snoop`, `Active`, `BusOff`), total frames, speed frames, bus errors, RX FIFO overflows, latest decoded `SpeedSample` (`centi_kmh`, `stamp`), `ring_head`, core 1 heartbeat
`0x180`	`64 B`	`CanConfig`	Linux	`enabled`, `active` (`false` = snoop), `bitrate`, optional DBC `Signal` (`id`, `extended`, `start`, `len` 1..32, `motorola`, `num`, `den` in `0.01 km/h` per raw count, signed `offset`), Linux heartbeat
`0x4000`	`2 KiB`	`CanRing`	core 1 (head)	`128 × 16 B` frame ring (`id`, `len`, `extended`, `rtr`, `stamp_ms`, `data[8]`) for `kria-vehicled` to log or inspect

`kria-vehicled` CLI (`sw/kria/vehicled/src/main.rs`):

- `--can BITRATE` enables `CAN1` (`125000`, `250000`, `500000`, `1000000` bit/s, snoop mode by default).
- `--can-speed ID[x]:START:LEN:intel|motorola:NUM/DEN[:OFFSET]` configures the DBC road-speed signal decoded in core 1, for example `kria-vehicled --can 500000 --can-speed 0x0D0:16:16:intel:1/1` (or an `x` suffix on ID for 29-bit extended frames).
- `--can-active` switches `CAN1` out of snoop mode into normal active mode for bench tests where no other receiver acknowledges frames.
- When `--can` is supplied, `kria-vehicled` keeps running on the CAN bus alone even if the `opendash` TCP server on the phone is unreachable.

Verification and limits: `6` unit tests in `kria-core::can` (bit timing for all four rates at `100 MHz`, `IDR/DLR/DW1/DW2` register packing, Intel and Motorola DBC signal extraction with scaling and offset, `CanConfig/CanStatus/CanRing` round trips, and `fresher` speed selection across wrap) and `1` CLI parser test in `kria-vehicled`. The K26 bitstream places `G6` and `D6` in Bank 66 (`LVCMOS12`). The adapter circuit is placed and routed (DRC 0 errors, 0 unrouted, **LAYOUT §6.8**). None of it has been run on a car or on a KV260. `D1531` is BORN's PESD1CAN (LCSC C343993), not Nexperia's: `[E: same SOT-23 pin-out as Nexperia's, lines on 1 and 2, common on 3; check its datasheet before ordering]`.

3. 77 GHz radar over CAN

Why it is worth adding. VEHICLE_PLATFORM.md §3.4 already makes the case. AERIS-10 is a 10.5 GHz surveillance radar for targets at kilometres. A 77 GHz automotive radar is the sensor built for obstacles in front of a vehicle, legal in 76 to 77 GHz without a licence, and unaffected by fog. The simulation below puts a number on that last point.

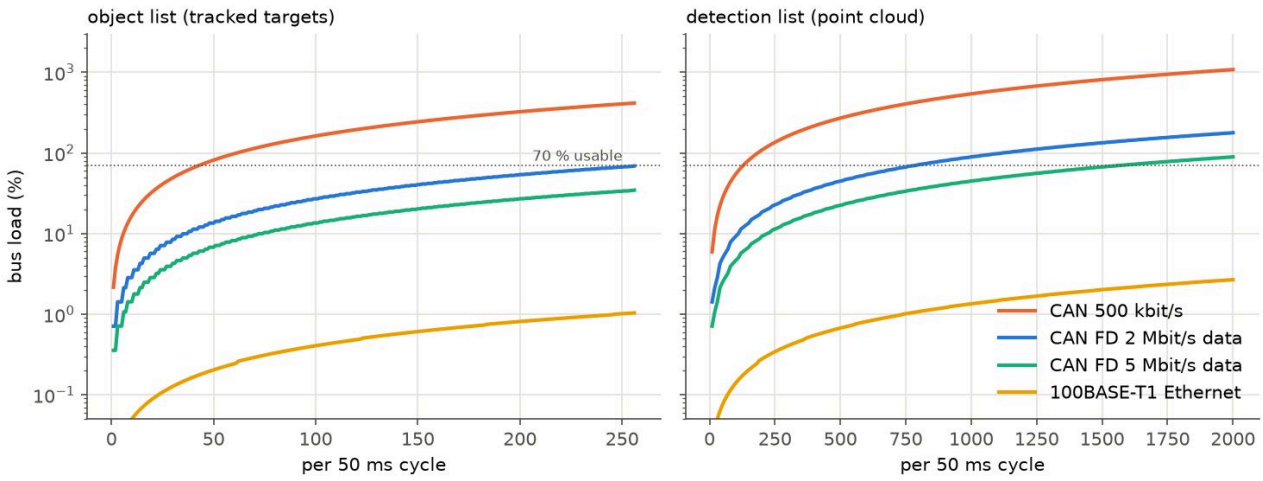
What a radar sends. Two kinds of output, often both:

- an **object list**: tracked targets, each with range, lateral position, closing speed, class and quality, typically three 8-byte CAN frames per object;
- a **detection list**: the raw point cloud before tracking, about 8 bytes per point and hundreds to thousands of points per cycle on the newer imaging radars.

The message layout comes from the sensor's own DBC file or interface document. **The radar goes on its own bus, never on the vehicle's**: a sensor that floods a bus does not belong on the one the engine uses.

Classic CAN is too small. One 8-byte standard frame is at most about 135 bits on the wire, so 500 kbit/s carries at most about 3,700 frames a second. At 20 Hz with three frames per object, that is 40 objects at 70 % load. The figure and the table compare the buses:

77 GHz radar output at 20 Hz: which bus carries it



Radar bus load

Per 50 ms cycle	CAN 500 kbit/s	CAN FD, 2 Mbit/s data	CAN FD, 5 Mbit/s data	100BASE-T1
32 objects	52 %	9 %	5 %	0.1 %
64 objects	104 %	18 %	9 %	0.3 %
100 objects	163 %	27 %	14 %	0.4 %
256 objects	415 %	69 %	35 %	1.0 %
500 detections	271 %	45 %	22 %	0.7 %
1,000 detections	541 %	90 %	45 %	1.3 %
2,000 detections	1,081 %	178 %	89 %	2.7 %

The model:

- **Classic CAN:** worst-case stuffing on every frame.
- **CAN FD:** 64-byte frames, about 30 bits at the 500 kbit/s arbitration rate and 590 at the data rate.
- **100BASE-T1:** UDP in 1,472-byte payloads with all headers, preamble and gap.

Source: `sw/integrations/kria_sw_figures.py`.

The alternatives:

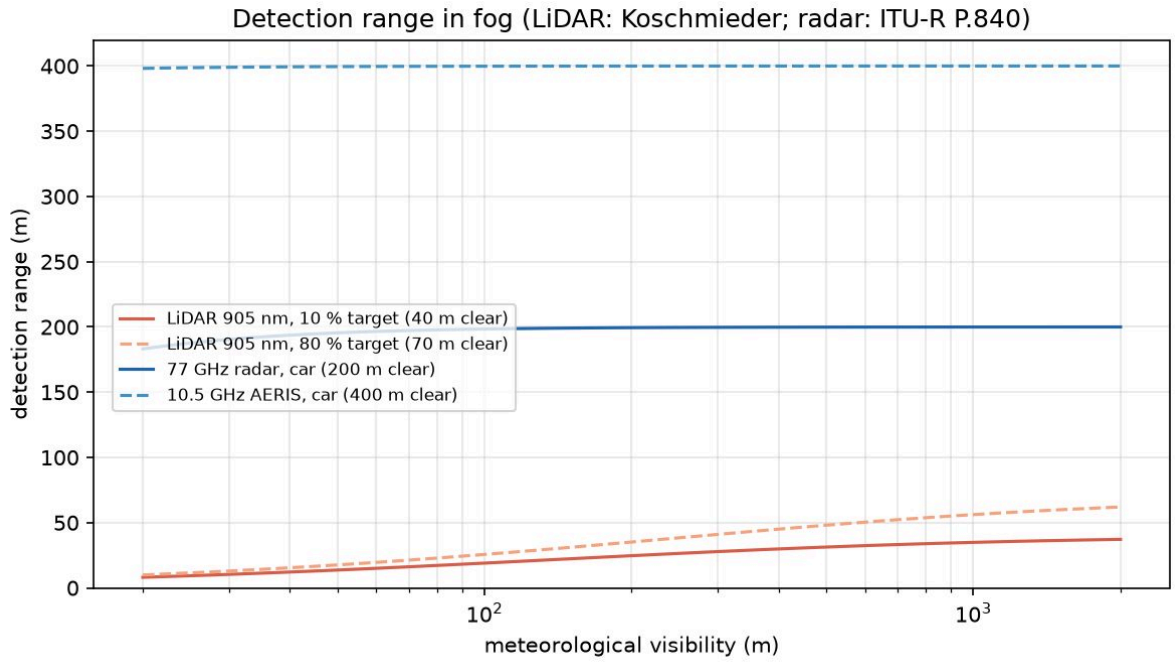
- **CAN FD.** A radar with a CAN FD output, 2 to 5 Mbit/s in the data phase, carries a full object list with room to spare, and a modest detection list.
- On the KV260 it needs a USB CAN FD adapter (gs_usb or PCAN-USB FD class, SocketCAN).
- The Zynq UltraScale+ PS's own CAN controllers are CAN 2.0 only `[V, Zynq UltraScale+ TRM]`, so they cannot do it.
- A CAN FD controller in the PL would be another way, at the cost of a PL pin pair and a transceiver.
- **Automotive Ethernet, 100BASE-T1.** Imaging radars and some long-range ones send their detections over 100BASE-T1, a single twisted pair `[E: e.g. Continental ARS548]`. It carries 2,000 detections at under 3 %.
- The KV260's own Ethernet port is taken by this board's link.
- So the path is a 100BASE-T1 to 100BASE-TX media converter into a USB 3.0 Ethernet adapter, the same kind as the LiDAR's (§5). The radar then arrives as UDP, decoded on the A53s.
- **Development radars** (TI AWR-class evaluation boards) give a USB serial stream, or CAN FD and Ethernet on the automotive parts `[E]`. They are useful on the bench, not as the vehicle's sensor.

Which to choose:

- **100BASE-T1** if the point cloud is wanted for the fusion grid (§6).
- **CAN FD** if only tracked objects are.

Either way the stream is small for the KV260: decoding it takes negligible CPU, and R5F core 1 could own it (**HMI.md §5**).

Fog. Two-way attenuation in fog follows ITU-R P.840. The liquid-water coefficient comes from the double-Debye permittivity of water. The fog's liquid water content comes from its visibility (Eldridge, `V = 0.024 M^-0.65` km). The LiDAR's extinction uses Koschmieder's `sigma = 3.912 / V` on both ways. Each sensor is scaled from its clear-air range: a radar's return falls as `1/R^4`, a LiDAR's on an extended target as `1/R^2`:



Detection range in fog

Visibility	Liquid water	LiDAR, 10 % target	LiDAR, 80 % target	77 GHz attenuation	77 GHz range	10.5 GHz attenuation
1,000 m	0.003 g/m³	34.9 m (of 40)	56.2 m (of 70)	0.01 dB/km	200 m	0.0002 dB/km
200 m	0.038 g/m³	24.7 m	35.2 m	0.12 dB/km	199 m	0.003 dB/km
100 m	0.11 g/m³	19.0 m	25.7 m	0.35 dB/km	198 m	0.008 dB/km
50 m	0.32 g/m³	13.7 m	17.6 m	1.0 dB/km	196 m	0.024 dB/km
30 m	0.71 g/m³	10.4 m	12.9 m	2.2 dB/km	190 m	0.054 dB/km

Between clear air and a 30 m fog the LiDAR loses about three quarters of its range. The 77 GHz radar loses 5 %, and 10.5 GHz loses nothing measurable. Rain is the radar's weather problem instead: tens of millimetres an hour attenuate 77 GHz by several dB/km `[E: ITU-R P.838]`, which over a 200 m two-way path is still a few dB. These curves treat attenuation alone. They leave out the LiDAR's false returns from fog droplets close to the sensor, which §6 models because it matters more than the lost range.

Source: **`sw/integrations/bev_fusion_sim.py`**, which regenerates the figure and the table.

4. Engine live data with opendash

What it is. opendash talks to a Scanmatik SM3 directly, without the vendor's software. Its protocol core (`core/`, Rust) has no I/O, so it builds for the K26's A53s (aarch64 Linux) as it is. **VEHICLE_PLATFORM.md §3.6** dismissed the SM3 on board for lack of Linux support. With opendash's direct protocol that no longer holds.

Links. There are two:

- **SM3 over Wi-Fi.** The SM3 is a TCP server on `192.168.81.1:777` on its own access point, so the KV260 needs a USB Wi-Fi adapter in station mode.
- **SocketCAN on the OBD port.** The same requests go out as ISO-TP from a USB-CAN adapter, with no SM3.

The OBD CAN adapter has to be a different one, or a different channel, from the radar's (§3).

The fast way to read live data. opendash's `docs/protocol.md` documents it:

- `2C <dpid> <id16>…` declares a packet of the module's own identifiers.
- `AA 04 <dpid>…` starts them.
- The module then streams 8-byte frames on `0x5E8` at 100 Hz per packet. That is about 30 times what polling achieves.
- A round holds at most 40 identifiers, and a packet at most seven bytes.
- The stream stops about five seconds after the tester goes quiet, so a `3E` TesterPresent goes out every two seconds.

Measured here, against an emulated ECU. The ECU here is the Opel Astra J's Denso SH7059, running its own flash image in `sh705x-emu` behind that emulator's emulated SM3 on this workstation. The SM3 test client declared one-byte identifiers in 5, 6 and 7 packets and counted the frames that arrived over 6 to 8 s:

Packets × identifiers	Rate per packet	Frames/s	Values/s
5 × 6 = 30	100.0 Hz	500	3,000
6 × 6 = 36	100.0 Hz	600	3,599
7 × 5 = 35	100.0 Hz	700	3,500
7 × 6 = 42	refused: the seventh declaration gets `7F 2C 31`, over the 40-identifier ceiling		

The emulator ran the ECU at 2.85 times real time on this machine (`sh705x bench`, 197 M SH-2E instructions/s), so the stream was never short of ECU time. The figures match what the real car gave on the SM3: seven packets at 98.9 Hz and 3,163 values/s (opendash's measurements).

The Montero. The fast stream above is a GMLAN feature of the Astra's ECU. The V80's own ECU speaks Mitsubishi's protocol, for which opendash carries a catalogue (`plugins/mitsubishi-mut3se`). By the owner's own measurement, filling every request frame, about 42 parameters come at around 100 Hz `[E, to be confirmed on the vehicle]`. Either way the data rate is a few kB/s, nothing for the KV260.

What it gives the system.

- The Vehicle screen.
- **Wheel speed for the SLAM's odometry**, which the LiDAR mapping needs to remember the ground it has already passed.
- **Ego speed for the radars.** A stationary target's Doppler is `v cos(theta)`, so speed separates moving targets from the ground.
- **The transmit lock.**

4.1 The integration, end to end

The stream reaches the board through opendash's **telemetry output**, added to opendash for this (its `docs/telemetry.md`):

- The app sends every live value it receives as one JSON line (`opendash-telemetry/1`) to any client on TCP port 35001.
- It takes back a **selection**: the rows to read, by identifier, including the rows that must ride in every round (road speed).

A selection sent while streaming replaces the one on the phone's live screen exactly as a preset does. The app stops the module's packets, declares the new ones and starts them again. This is opendash's rotation mechanism, which already cycles through rounds when more than 40 identifiers are selected. So the car's screen can ask for any parameter the ECU has, at the cost of a couple of seconds per change.

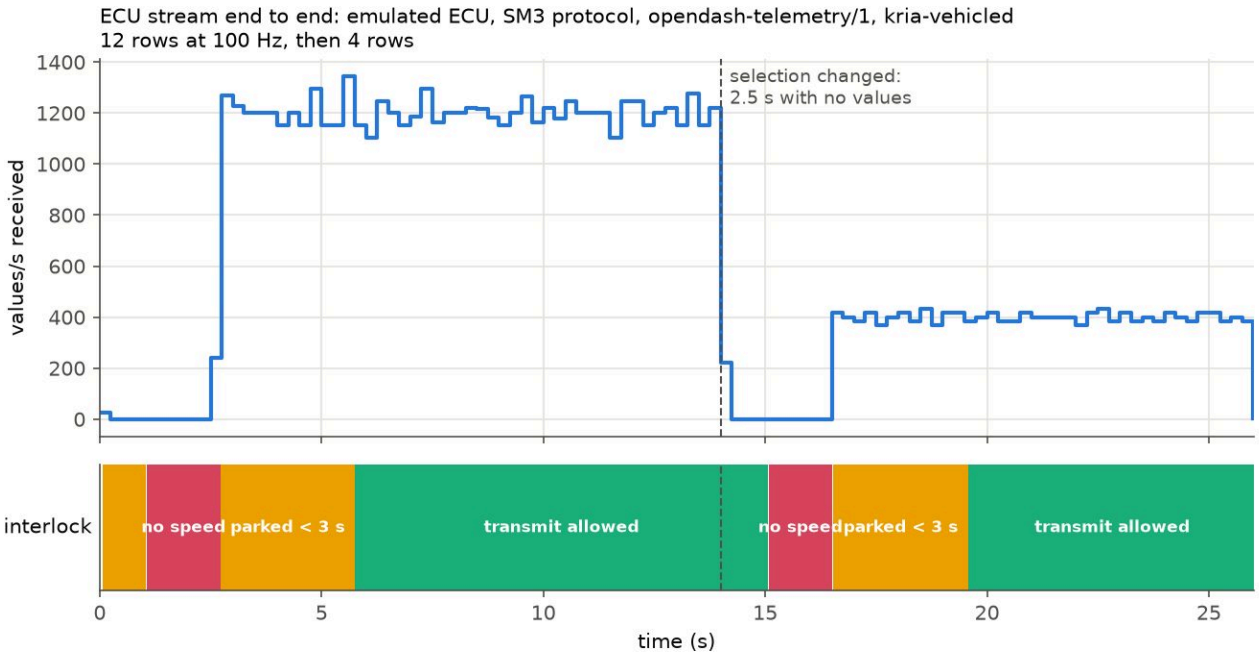
On the board, **`kria-vehicled`** (**`sw/kria/vehicled`**, Rust) does the rest:

- It connects to that port and sends the selection.
- It keeps the latest value of every row.
- Every 50 ms it writes road speed to R5F core 0 through the shared mailbox, stamped with the PL clock both sides read.
- The transmit lock on the R5F (§7) runs on that speed.

Tested end to end on the workstation, with only the ECU emulated. The chain was:

- the Astra J's ECU in `sh705x-emu` (its own flash image), behind the emulator's SM3;
- a bench bridge that speaks the SM3 protocol and serves `opendash-telemetry/1` exactly as the app does (not in this repository);
- `kria-vehicled`, with the interlock also running on the PC.

The daemon asked for 12 identifiers with road speed always on. After 14 s it changed to 4, as a screen changing page would:



ECU stream end to end

	Measured
12 identifiers	1,200 values/s (100 Hz each)
4 identifiers	400 values/s
Gap when the selection changes	2.5 s with no values
Transmit lock through that gap	locked 1.1 s into the gap (speed older than 1 s); allowed again 4.5 s later (the 2.5 s gap, then 3 s parked)

The gap is the declaration: each `2C` with more than two identifiers is a multi-frame ISO-TP exchange with flow control. The bridge alone measured 2.4 to 3.7 s per change, with 1 to 6 packets. Two consequences follow:

- **A screen should change the selection only when it needs to**, not on every page.
- **The GPS fallback matters.** Without it, every selection change locks the transmitter for about four seconds. With a fresh GPS speed (under 2 s old), the interlock switches source instead; the core test `falls_back_to_gps_then_fails_safe` covers this.

To rerun, with the emulator and a server on port 35001:

```
cargo run --release -p kria-vehicled -- --server 127.0.0.1:35001 --select 0x000D,0x000C,0x0005,0x000B,0x0004,0x0010,0x000F,0x0023,0x308A,0x1A2D,0x303A,0x131F --always 0x000D --licensed --interlock --seconds 26 --
then-after 14 --then-select 0x000D,0x000C,0x0023,0x308A --csv run.csv
python sw/integrations/kria_sw_figures.py --telemetry-csv run.csv
```

The figure plots only rates and interlock states. The engine values come from the owner's own ECU image and stay out of the repository.

5. 3D LiDAR on a USB-Ethernet adapter

VEHICLE_PLATFORM.md §3.1 names the candidates: the Livox Mid-360 (360° × 59°, about 200,000 points/s) or the Unitree L2. A 64-beam spinning LiDAR is the upper end, at up to 1.3 million points/s (64 × 2,048 × 10 Hz). On the wire that is roughly 20 to 70 Mbit/s of UDP `[E, from the point formats]`. A USB 3.0 Gigabit adapter (RTL8153 or AX88179 class) carries it with room to spare. Its time stamps come from PTP over the adapter (software time stamping) or from the GPS (§2).

The LiDAR is the sharpest sensor in clear air and the weakest in fog (§3). Its returns from droplets also land close to the sensor, where they read as obstacles. That is why the integration that matters is the fusion in §6, not the LiDAR alone.

6. Fusion on the PL: `kria_bev_grid`

`fpga/kria/integrations/kria_bev_grid.v` is a bird's-eye-view occupancy grid: 256 × 256 signed 8-bit log-odds cells around the vehicle. At 0.5 m cells it covers 128 m × 128 m. It is in the K26's block design behind an AXI wrapper, with a DMA channel for its frames, and R5F core 1 feeds it (§6.1).

What it does.

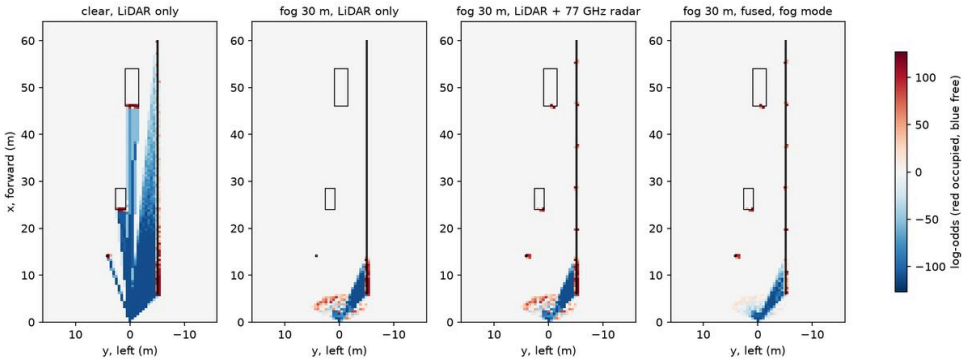
- **Detections.** The host sends detections already transformed to the vehicle frame (x and y in Q8.8 cells), each tagged with its sensor.
- **Hits.** A detection adds that sensor's hit weight to its cell.
- **Ray casting.** For sensors with ray casting on (the LiDAR), every cell on the line from the sensor to the detection first loses that sensor's miss weight: the beam went through, so the space is free. The line is drawn with Bresenham, one cell per clock.
- **Decay.** A decay pass moves every cell toward zero by `max(1, |v| >> 3)`, so obstacles that are not seen again fade.
- **Dump.** A dump streams the 65,536 cells out, eight per 64-bit beat, for the HMI or the SLAM.

Each sensor has its own weights and origin, set by the host.

Fog mode. In fog the LiDAR's near returns multiply. The host can see that in its point statistics, and lowers the LiDAR's hit weight. The radar's objects then carry the grid. The simulation uses the scene shown below:

- a car at 24 to 28 m;
- a truck at 46 to 54 m;
- a post at 14 m;
- a guard rail on the right.

It runs four frames of a ±60° LiDAR (0.2° steps, 10 % reflectivity on the car, Koschmieder losses, false returns at 0.8 to 6 m whose probability grows with the extinction) and of a 77 GHz radar (two scatterers per object, 0.15 to 0.2 m noise):



Fused occupancy grid in fog

- **Clear air, LiDAR only.** The car, truck, post and guard rail are occupied, and the free space up to them is clear.
- **30 m fog, LiDAR only.** Nothing beyond about 12 m is seen, and the near field fills with false obstacles.
- **Fused.** The radar restores the car, the truck, the post and the rail.
- **Fused in fog mode.** The near-field clutter fades below the occupancy threshold too.

Verification.

- **Bit-exact against the model.** `fpga/sim/tb_kria_bev_grid.v` feeds the fog-mode run's 974 commands with random gaps and random output backpressure. All 65,536 dumped cells match the Python model in `sw/integrations/bev_fusion_sim.py`, which is written to be bit-exact.
- **Mutation `bev_no_forward`.** It removes the read-modify-write forwarding; the bench catches it on two beats.

To rerun: first `python sw/integrations/bev_fusion_sim.py` (writes `fpga/sim/out/bev/`), then `fpga/sim/run.ps1 tb_kria_bev_grid`.

Cost on the K26 (out-of-context synthesis and implementation, `xck26-sfvc784-2LV-c`, Vivado 2026.1):

	Used	Of the K26
CLB LUTs	344	0.3 %
CLB registers	301	0.1 %
Block RAM tiles	16	11 %
DSP48E2	0	0
Timing at 100 MHz (`clk_pl_0`)	WNS +2.361 ns, WHS +0.057 ns	

In the full build it costs about what it costs alone (§6.1). The 64 K × 8 memory is cascaded over 16 block RAMs, so the read-modify-write path is about 6.5 ns. The core closes at 100 MHz but not at 250 MHz (−2.5 ns). A registered RAM output, with one more forwarding stage, would be the way up if it were needed.

Does it need the PL? One cell update per clock is 100 million per second. A Mid-360's 200,000 points/s with 60-cell rays is 12 million cell updates per second, which one A53 core can probably keep up with `[E]`. A 1.3 Mpoint/s LiDAR is 78 million, scattered across 64 KB, which is where a core that never misses its cache and never waits for Linux pays off. Doing it in the PL also leaves the A53s for the SLAM.

Not done yet:

- **Ego-motion.** The grid is vehicle-centred, so as the vehicle moves the host has to shift it, or keep a world-anchored grid and recentre it.
- **A LiDAR DMA.** The wrapper's stream input (`s_axis_det`) is there for a LiDAR's points at full rate; nothing drives it yet.
- **Real data.** Real point clouds and object lists.

6.1 On the K26: wrapper, DMA and R5F core 1

In the block design (`fpga/kria/bd.tcl`):

- **`kria_bev_axi`** (`fpga/kria/kria_bev_axi.v`, AXI-Lite at `0x8003_0000`) holds the per-sensor origins, weights and ray-casting flags, and a command port: `DET_XY`, then `DET_CMD`, which pushes the command into a 512-entry queue. A second input, `s_axis_det`, takes commands as a stream for a LiDAR DMA; the queue has priority over it. The register map is in **FPGA_GATEWARE.md §5.7**.
- **`axi_dma_1`** (S2MM only, `0x8004_0000`, interrupt `pl_ps_irq0[5]`) writes each dump, 64 KiB, into one of two frame buffers after the mailbox region (`0x3EE1_0000`, `bev_frames` in **`sw/ias2rf_pl.dtsi`**), in about 82 µs.

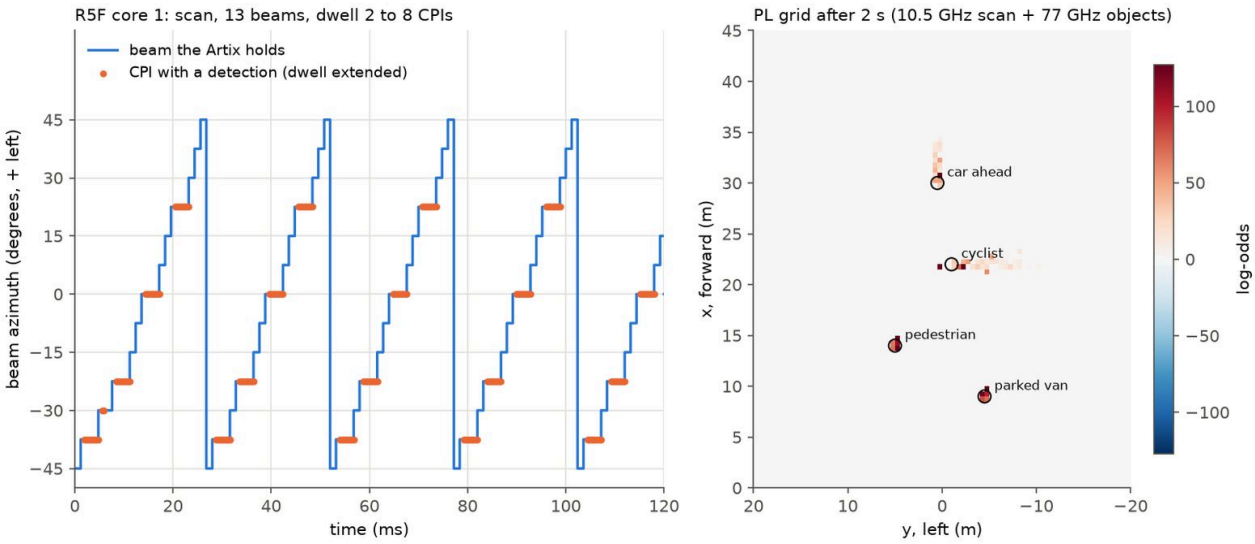
R5F core 1 owns the command port. A command is two register writes, so two writers would pair one's position with the other's command. Core 1 (**`sw/kria/r5f/src/bin/core1.rs`**) is the only writer. Every 100 µs it:

- **Scans the 10.5 GHz radar.** It reads `RADAR_STAT` and steps `kria_core::radar::Scheduler` once per CPI. The scheduler dwells 2 CPIs on a beam, plus 2 more for each CPI with a detection, up to 8. It ignores the CPI that straddles a beam change and pulses `BEAM_STROBE` for the next beam. In the Artix's new scan mode (`ADAR_CTRL[13]`), each strobe loads the next of beams `0..scan_last`, so no register write is needed per beam. `RADAR_STAT[31:26]` now counts CPIs, which is how core 1 knows one has finished.
- **Puts each detection in the grid.** The strongest cell of the CPI is converted back from the map's conjugate position, then from range and beam azimuth to vehicle coordinates (`bev::Mount`), and pushed as the 10.5 GHz radar's point.
- **Drains Linux's ring.** The 77 GHz radar's objects (decoded on the A53s, §3), and anything else Linux wants in the grid, go through a ring in the shared region (**`kria_core::ring`**), 64 per loop.
- **Makes the frames.** Every `frame_ms` (100 ms by default) it arms the DMA on the free buffer, pushes a decay pass and a dump, and publishes the buffer in its status block when the DMA finishes.

Linux sets the scan (beams, azimuths, dwell, range and Doppler per bin), the radar's mount and the frame cadence in the mailbox (`Core1Config`), and writes the grid's weights and origins once. Silent for a second, Linux stops core 1's scan and grid while core 1 keeps the vehicle CAN (§2.2) running.

End to end. **`sw/kria/core/examples/radar_grid.rs`** runs core 1's code in core 1's order for 2 s. Around it are models of the Artix's beam scan, of `kria_radar_proc` (a CPI every 400 µs, three CFAR cells per target in the beam, the conjugate map) and of a scene: a car ahead closing at 2 m/s, a pedestrian, a cyclist crossing, and a parked van. The 77 GHz radar sees the same objects every 50 ms, through the ring. Its 2,705 commands then go through the RTL: **`tb_kria_bev_axi`** alternates them between the register port and the stream, and the dump matches the bit-exact model in all 65,536 cells.

CPIs in 2 s	4,999, none missed
Beam changes	1,034; a full scan of 13 beams in about 25 ms
CPIs with a detection	2,525, every one on a real target's beam and range
Commands	2,525 radar detections, 160 objects through the ring (none dropped), 19 decay passes, 1 dump



R5F core 1: the scan and the grid

On the left, the dwell grows on the four beams with a target. On the right, the grid after 2 s:

- the car's trail as it closes;
- the cyclist's track across the road;
- the pedestrian and the van as fixed cells.

To rerun:

1. `cargo run --release --example radar_grid` in `sw/kria/core`;
2. `python sw/integrations/radar_grid_replay.py`, which writes the expected grid and the figure;
3. `fpga/sim/run.ps1 tb_kria_bev_axi -PlusArg BEV_DIR=../radar_grid`.

Verification of the wrapper. `tb_kria_bev_axi` on the fog run of §6 (974 commands) checks:

- the reset values;
- the configuration read-back;
- both command paths against the model;
- the queue filling to 512 with `STATUS.overflow` set and cleared;
- `COUNT`.

The mutation `bev_axi_no_stage` (`DET_CMD` ignores `DET_XY`) fails it. The Artix's scan mode is in `tb_adar_ctrl`: five strobes load beams 0, 1, 2, 0 and 1, each with its own weights; the mutation `scan_ignored` fails it. The CPI count is checked by the system bench `tb_system_signals` in the G-8 radar case, which passes again with it.

Cost in the K26 build: `kria_bev_0` takes `781` LUT (`192` of them LUTRAM), `623` FF and `16` BRAM36, and its DMA `axi_dma_1` `1,046` LUT, `1,590` FF and one BRAM36 and one BRAM18. Including `kria_dsp_out`, `kria_ps_framer`, `TX_KEY`, PS `CAN1` EMIO and the KrakenSDR and HackRF Pro blocks (§9, §10), the whole block design is at `53,294` LUT (`45.5 %`), `46,879` FF (`20.0 %`), `44.0` BRAM36 eq. (`30.6 %`), `1` URAM (`1.6 %`) and `229` DSP48E2, and meets timing with `WNS = +0.991 ns` and `WHS = +0.010 ns` (**FPGA_GATEWARE.md §3.3**).

7. Software on the K26's processors

Code that runs on the Kria's ARM cores is written in Rust, with its logic in an I/O-free core, as in opendash. `sw/kria` holds it:

Crate	Runs on	What it does
`kria-core`	A53 and R5F (`no_std`, no allocation, no `unsafe`)	`pps` (the loop of §2.1), `interlock` (the transmit lock), `link` (the IAS1 link watchdog), `can` (the PS `CAN1` register driver, DBC speed extractor and mailbox blocks of §2.2), `radar` (the beam scan), `bev` (the grid's commands and coordinates), `ring` (Linux's grid commands for core 1), `telemetry` (`opendash-telemetry/1` lines), `mailbox` (the shared blocks' layout and seqlock)
`kria-vehicled`	A53, Linux	§2.2, §4.1
`kria-r5f0`	R5F core 0, from TCM, started by remoteproc	At 1 kHz: the PPS loop on `kria_pps`, the IAS1 link watchdog, the transmit lock (it owns `TX_KEY` at `0x8000_0038`), and status back to Linux

Crate	Runs on	What it does
`kria-r5f1`	R5F core 1, from its own TCM	At 10 kHz: the 10.5 GHz radar's beam scan, the fusion grid's command port and frames (§6.1), and the vehicle's CAN 2.0 bus on PS `CAN1` (§2.2)
`kria-hmi-core`	A53 (any host; tested on a PC)	The screens' data plane: the PL's result blocks, RDS, ADS-B, radar, spectrum, a frequency and mode to register writes (**HMI.md §4**)
`kria-hmid`	A53, Linux	The HMI's data service: DMA blocks in, audio, register writes, I/Q recording, snapshots over WebSocket; asks core 0 for transmit through `kria-vehicled` and the mailbox
`kria-hmi`	A53 (Linux KMS), a PC, a browser	The ten screens, in Slint (**HMI.md §3**)

The transmit lock (`kria_core::interlock`) runs on R5F core 0 every millisecond:

- **Speed source:** the car's road speed first (whichever of core 1's `CAN1` speed reading and `opendash`'s ECU reading has the newer `kria_pps` tick stamp, via `can::fresher`, while fresh within 1 s), then the GPS's (2 s).
- **Moving or parked:** 3 km/h or more is moving. Parked needs under 1 km/h for 3 s, with hysteresis in between.
- **Licence:** the flag must be set.
- **Time-out:** at most 180 s of continuous transmission, then a 10 s cooldown after the button is released.
- **Fail-safe:** no fresh speed from any source, Linux silent for 0.5 s, or the IAS1 link down means locked.

On the R5F it holds while Linux is busy or restarting. Core 0 switches the transmitter on and off exclusively through `TX_KEY` (`0x8000_0038` in `kria_pl_link`), which requires `24'h4B4559` (`"KEY"`) in `[31:8]` and full byte strobes (`0x4B45_5901` on, `0x4B45_5900` off). `TX_KEY` is clocked on `pl_clk_100m`, so core 0 can always clear it (including from `on_panic()`) even when the IAS1 receive clock is missing. `DSP_CTRL[1]` (`0x8000_0040`) is now read-only and mirrors `TX_KEY[0]`, so whole-register writes to `DSP_CTRL` by Linux (`kria-hmid`) cannot key or clear the transmitter. Core 0 also requires the IAS1 link to be up: with the link down the transmit samples do not reach the front end, and when it returns they should not resume on their own.

The IAS1 link watchdog (`kria_core::link`), also on core 0 every millisecond:

- **Down:** after 20 ms with `link_up` low, it pulses `LINK_CTRL[2]` to retrain. If the link stays down, it retrains again after 100 ms, then 200, 400 and so on up to 5 s, so a front end that is switched off is not hammered. The first training after start gets 3 s.
- **Errors:** more than 100 CRC errors within a second of link time retrain it once.
- **Health and counts:** go to Linux in the mailbox.

A link register read can abort: `kria_pl_link` answers SLVERR when the link's receive clock is missing, which is when the link is down. The firmware's data-abort handler counts the abort and resumes at the next instruction, and the watchdog takes an aborted read as "down". A core that hung on that abort would leave the transmitter as it was.

AGC and front-end sequencing stay where they are. The AGC loop already runs in the Artix fabric (`fe_agc`, Rev08 G-5): it reads the AD9484's peak every 131 µs and drives the `PE4312` and the LNA bypass with no processor in the loop. The front end's sequencing is a handful of Artix register writes at start-up and on a band change. The Kria reaches those registers only through the link's command stream (`0x10`), whose DMA Linux owns. So both stay as they are, with Linux setting the AGC's thresholds and doing the sequencing.

The mailbox:

- **Where:** a 64 KiB `reserved-memory` region at `0x3EE0_0000` (**`sw/ias2rf_pl.dtsi`**), with the grid's two frames right after it.
- **Layout:**

Offset	Block	Writer
`0x000`	speeds, licence, transmit request	Linux
`0x040`	PPS, interlock and link status	core 0
`0x080`	scan and grid status, the latest frame	core 1
`0x0C0`	vehicle CAN status and decoded road speed (`CanStatus`)	core 1
`0x100`	scan and grid configuration	Linux
`0x180`	vehicle CAN bitrate and DBC speed signal (`CanConfig`)	Linux
`0x1000`	grid command ring	Linux (head), core 1 (tail)
`0x4000`	vehicle CAN received frame ring (`CanRing`, `128 × 16 B`)	core 1 (head)

- **Who writes:** one writer per block, and each block is a seqlock.

- **Time base:** `kria_pps`'s `NOW`, the PL clock that all three read. Reading `NOW_LO` latches `NOW_HI` for whoever reads it next, so each reader takes two pairs and keeps them only if they agree.

RPMsg (OpenAMP) is the general-purpose alternative. For a few numbers a millisecond, a fixed block with no driver is enough.

Tests:

- **`kria-core`:** 35 tests on the host.
- PPS: lock with a fast and a slow oscillator, a frequency step, a false pulse, holdover and reacquisition, a counter that wraps.
- Interlock: settling, creeping, GPS fallback and fail-safe, licence, time-out and cooldown.
- Link watchdog: power-up training, the back-off sequence and its reset, slow errors counted, a burst retrained once.
- Vehicle CAN: bit timing for 125 kbit/s to 1 Mbit/s at 100 MHz, `CAN1` frame register packing, Intel and Motorola DBC signal extraction with scale and offset, `CanConfig`/`CanStatus`/`CanRing` round trips, and `fresher` speed selection across counter wrap.
- Radar scan: dwell and beam order with nothing in view, a target holding the beam, the conjugate map, negative Doppler, CPIs missed across the counter's wrap.
- Grid: command words against the RTL layout, cell edges, sine and cosine within 2e-6, mounts, configuration words.
- Telemetry: lines exactly as opendash writes them, and junk.
- Mailbox and ring: round trips, seqlock, counters that wrap.
- **Cross-builds:** the core builds for `armv7r-none-eabihf` and `aarch64-unknown-linux-gnu`.
- **The R5F firmware:** two images, each linked into its core's ATCM and BTCM (`armv7r-none-eabihf`).
- **The daemon:** 1 host test (`--can-speed` parser), builds for the A53s, and ran the end-to-end test of §4.1.
- **Core 1 end to end:** §6.1.

None of it has run on a car or on a KV260 yet.

8. What it would take, in order

1. **On a KV260:**
2. the bitstream with `kria_pps`, `TX_KEY`, PS `CAN1` EMIO, the grid and its DMA;
3. the overlay with the PPS and grid nodes, the mailbox and the frame buffers;
4. `kria-r5f0` and `kria-r5f1` loaded through remoteproc;
5. the Artix's beam table loaded in scan order and `ADAR_CTRL[13]` set;
6. `kria-vehicled` with `--can` on the vehicle's CAN 2.0 bus (`J9` pins 6 and 8) and/or against opendash on the phone;
7. `gpsd` and `chrony` for the GPS's position and time, and its PPS on `J9` pin 12.

Everything here is built and tested on the bench. Only the board is missing.

1. **The LiDAR on its USB adapter.** Its ROS 2 driver and a SLAM (FAST-LIO2 or similar), fed with the wheel speed from step 1.
2. **The 77 GHz radar on its own CAN FD adapter or 100BASE-T1 converter (§3).** Its DBC or interface document and a decoder, with its objects on the Vehicle screen.
3. **The LiDAR into the grid at full rate:** a DMA channel (MM2S) into `kria_bev_axi`'s `s_axis_det`, and the points converted to grid commands on the A53s.

1. **The KrakenSDR and the HackRF Pro (§9, §10).** Built and tested end to end like the grid. On a KV260 they need `kria-sdrd` built with `--features hw` against KrakenRF's librtlsdr and libhackrf, and the two blocks' nodes in the overlay.

9. Direction finding with a KrakenSDR

Added 18 November 2026. Built and tested end to end, from synthetic USB transfers through the PL's RTL to the screen; not run on a KV260.

What it is `[V, KrakenRF's pages and its open-source code]`:

- five RTL2832U receivers with R820T2 tuners, 24 to 1,766 MHz, on one clock, behind one USB hub;
- 2.4 MS/s per channel by default, unsigned 8-bit I/Q, 4.8 MB/s per channel and 24 MB/s in all, inside USB 2.0's 480 Mbit/s;

- a noise source that the control channel's bias-tee GPIO switches onto all five inputs through calibration switches, for the coherence calibration;
- five SMA inputs with a 4.5 V bias tee each; it takes 5 V at 2.4 A over USB-C.

What it adds. This board receives VHF and UHF on one antenna (`J961`, §5 of **REV08_PLAN**); it cannot say where a signal comes from. A KrakenSDR on one of the KV260's USB ports, with five antennas on the roof, gives the bearing of a transmitter from 24 MHz to 1.77 GHz: a repeater, a beacon, an interferer, a lost model aircraft. On the move, bearings logged with the GPS position fix the transmitter by triangulation.

Why not on the board. It is five complete receivers with their own ADCs. Adding them would mean a new RF section, which reopens every check of the board (DRC, signal integrity, renders, fabrication, documents). Over USB it costs nothing on the board, and it is a product people already own.

9.1 The chain

Step	Where	What
USB	A53, `kria-sdrd`	Five devices, one bulk stream each, through KrakenRF's librtlsdr (feature `hw`, `sw/kria/sdr/src/usb.rs`). The transfers (256 KiB) arrive from the five devices in no fixed order and are reassembled per channel
Noise source on	A53	Bias-tee GPIO 0 of the control channel (serial 1000), as KrakenRF's own software switches it
Delay	A53	Each stream starts at its own moment: a whole number of samples. The peak of the cross-correlation with channel 0 over ±64 samples finds it; the streams are then read from aligned offsets
Phase and gain	A53	With one common source, the covariance's dominant eigenvector is the channels' gains up to a common factor. The weights are its inverse, with each channel's amplitude from its power
Noise source off	A53	The CPI: 2^15 aligned snapshots (13.7 ms at 2.4 MS/s), packed two 64-bit beats per snapshot into a DMA buffer
Weights, covariance, Bartlett	PL, `kria_doa`	Each channel times its Q2.14 weight; $R = \Sigma\, y\, y^{H}$ over the CPI (15 entries, 48 bits); then a^H R a for 360 bearings, one per clock, from a table of steering cross-products the A53 writes for the array and the frequency
Scale	A53	Reads R's diagonal, picks `SHIFT` so the largest entry fits 25 bits, asks for a scan of the held R
MUSIC	A53	R's eigendecomposition (5 × 5, Hermitian, through its 10 × 10 real form), the number of sources from the eigenvalues (10 dB above the smallest), the noise subspace's pseudo-spectrum on the same 360 bearings
Screen	A53	The Bearing screen (**HMI.md**): both spectra on a polar plot, the bearings, the eigenvalues, the calibration

The PL takes the part that grows with the sample count: 50 complex products per snapshot, 120 M multiplies a second at 2.4 MS/s, which would occupy an A53 core. What stays on the A53s grows with the number of antennas, not the samples: an eigendecomposition of a 5 × 5 matrix per CPI.

The methods. Cross-correlation for the streams' offsets, the principal eigenvector for an array's calibration from a common source, Bartlett (the delay-and-sum beamformer) and MUSIC (Schmidt, 1986) are textbook methods. `kria-sdrd` implements them from their definitions. KrakenRF's heimdall_daq_fw and krakensdr_doa do the same jobs on a Raspberry Pi and were read for the device's facts: the noise source's GPIO, the default rate, the array conventions. They are GPL; none of their code is used here, and this repository stays under Apache-2.0.

`kria_doa` (**`fpga/kria/integrations/kria_doa.v`**), at `0x8005_0000`, fed by `axi_dma_2` (MM2S) at `0x8006_0000`:

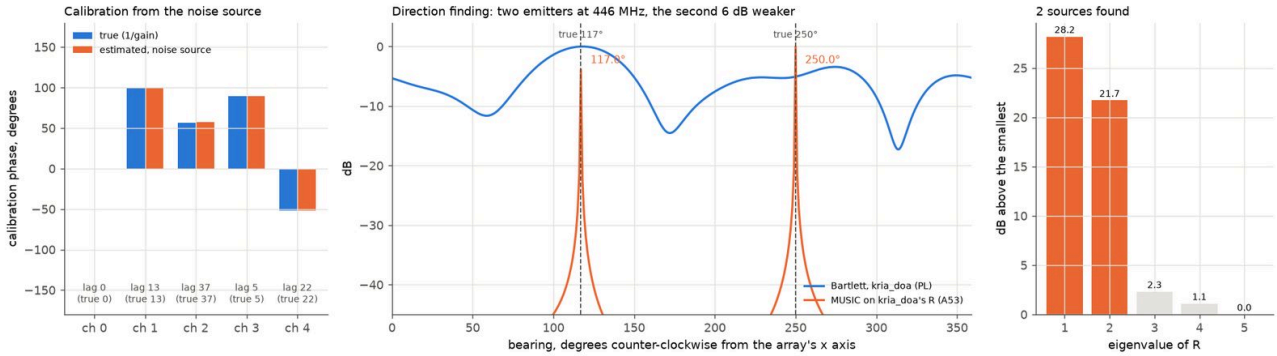
Offset	Register
`0x0000`	ID `DOA1`
`0x0004`	CTRL: start a CPI, scan when it ends, scan the held R now
`0x0008`	STATUS: accumulating, scanning, done, CPI count
`0x000C`, `0x0010`	N_LOG2 (CPI of 2 to 65,536 snapshots), SHIFT
`0x0020` to `0x0030`	the five weights, Q2.14
`0x0100` to `0x01EF`	R, 15 entries of 48 bits
`0x0800` to `0x0D9C`	P(θ), 360 bearings
`0x8000` to `0xD9FC`	the steering table, 10 cross-products per bearing

9.2 End-to-end test

- **The capture** (`sw/integrations/kraken_sim.py`):
- five channels at 2.4 MS/s on a circular array of five elements, half a wavelength apart at 446 MHz (28.6 cm radius);

- each stream starts 0, 13, 37, 5 and 22 samples late, and each channel has a random complex gain;
- 65,536 samples with the noise source on, then two FM emitters at 117° and 250°, the second 6 dB weaker, with each channel's thermal noise;
- quantised as the RTL2832U does and cut into 256 KiB transfers.
- **The A53** (`kria-sdrd kraken-pre`) reassembles the transfers in a shuffled order, finds the offsets and the weights, and writes what its driver sends the PL: the register writes, the snapshots, and from its bit-exact model of `kria_doa` the R and P the PL must return.
- **The RTL** (`tb_kria_doa`) runs the driver's sequence: the 3,606 register writes, a CPI with gaps in the stream, R's diagonal read back and `SHIFT` chosen from it as the driver does, the rescan. R and all 360 values of P equal the model's, bit for bit. Mutation `doa_no_conj`, the product without its conjugate, fails at the first entry.
- **The A53 again** (`kria-sdrd kraken-post`) reads the RTL's R and P, runs MUSIC, and writes the record the Bearing screen draws.

Result	Value
Stream offsets found	0, 13, 37, 5, 22: all exact
Calibration phases	within 1° of the truth on every channel
Sources found from R's eigenvalues	2 (28.2 and 21.7 dB above the smallest; the noise eigenvalues within 2.3 dB)
MUSIC bearings from the RTL's R	**117.0° and 250.0°** (true 117° and 250°)
Bartlett from the PL	118.0° for the strong emitter; the weaker one is not resolved (its lobe merges into a 274° sidelobe region)



KrakenSDR end to end: calibration, Bartlett and MUSIC, eigenvalues

Bartlett is what the PL computes cheaply and what the screen shows as the coarse picture. Five antennas give it a beam about 70° wide, too wide to separate two emitters 133° apart when one is 6 dB weaker. MUSIC uses the same R and places both to a tenth of a degree. MUSIC needs the number of sources, which R's eigenvalues give, and fails when two sources are coherent (a reflection of the same signal). Forward-backward averaging of R is the usual cure, an A53 change if needed.

Not tested: a real KrakenSDR, and the `hw` paths of `kria-sdrd` (the librtlsdr calls and `/dev/mem`), which build only against the libraries on the board. The array's own errors (cable lengths, antenna placement, the car body's reflections) are not in the model. KrakenRF calibrates the cable lengths through the noise source as here; the body's effect needs a measured array manifold, which the steering table can hold as it is (any complex value per bearing and pair).

10. HackRF Pro: 1.1 to 7.1 GHz and a fast sweep

Added 18 November 2026. Built and tested end to end, from synthetic USB transfers through the PL's RTL to the screen; not run on a KV260.

What it is `[V, Great Scott Gadgets' documentation and the hackrf repository, firmware and host code]`:

- a half-duplex transceiver from 100 kHz to 6 GHz, tunable from 0 to 7.1 GHz;
- 20 MS/s of 8-bit I/Q over USB 2.0 (Type-C); 16-bit samples at lower rates (9 to 11 effective bits); 4-bit at up to 40 MS/s;
- built from a MAX2831 transceiver, an RFFC5072 mixer and synthesiser (the part this board's VHF/UHF front end uses), a MAX5864 converter, an iCE40 UltraPlus FPGA and an LPC43xx microcontroller;
- a TCXO, clock input and output on SMA (also usable as trigger in and out), a 3.3 V 50 mA port supply, and a trace to cut to disable transmit.

What it adds to this board and the other integrations:

Capability	This board	HackRF Pro
Receive, HF	0 to 25 MHz (AD9253)	from 100 kHz, but 8 bits at 20 MS/s
Receive, VHF/UHF	25 MHz to 1.1 GHz (`RX_VU`, Rev08)	yes
Receive, 1.1 to 7.1 GHz	no	**yes**: L-band, mobile bands, 2.4 and 5 GHz, 5.8 GHz video links, ITS-G5
Transmit, 1.1 to 6 GHz	no (the DACs reach HF and low VHF)	**yes**: the 23, 13, 9 and 6 cm amateur bands
Spectrum of the whole range	no	**yes**: its sweep mode, about 12 GHz/s
Direction finding	no	no (the KrakenSDR, §9)

So the integration does three things: the sweep, through the PL; reception above 1.1 GHz as a 20 MS/s stream to the A53s (the same path as any USB SDR, with the waterfall on the GPU); and transmission above 1.1 GHz behind the same lock as this board's own transmitter. On the board it would be a second complete transceiver with its own USB, the same objection as §9.

The sweep `[V, firmware/hackrf_usb/usb_api_sweep.c, host/hackrf-tools/src/hackrf_sweep.c]`:

- the firmware retunes for every block and sends 16,384-byte blocks, each starting with `0x7F 0x7F` and the block's frequency f as a little-endian u64;
- the LO sits at f + 7.5 MHz; the steps alternate +5 MHz and +15 MHz ("interleaved"), and from each block two 5 MHz quarter bands are kept, [f, f + 5) and [f + 10, f + 15) MHz, away from the LO and the filter's edges;
- after each retune the Pro's firmware discards one block (the One discards two), so 1,220 blocks a second reach the host: about 12 GHz/s;
- `hackrf_sweep` on a PC Fourier-transforms the last N samples of each block, once.

`kria_sweep` (**`fpga/kria/integrations/kria_sweep.v`**), at `0x8007_0000`, fed and drained by `axi_dma_3` at `0x8008_0000`:

- takes the USB transfers as they come, checks each block's header (a bad one is dropped and counted), and keeps its frequency;
- transforms the block's last 2^k segments of 256 samples (k = 3: 2,048 of its 8,187), each with a Hann window, and sums their powers bin by bin (Welch's method without overlap);
- returns per block the frequency and 128 powers, the two quarter bands at 78.125 kHz, for the A53 to place on the panorama.
- The window and the 128 twiddles are written by the A53 at start. One block takes about 54,500 clocks, 0.545 ms at 100 MHz, against 0.82 ms between blocks. The FFT works in one block RAM with one write and one read port, six clocks per butterfly.

Why the averaging. One FFT of a noise-like signal (LTE, Wi-Fi, DVB-T) is ragged, ±5 dB from bin to bin. The sum of eight is within ±1.8 dB. A PC keeps one FFT per block to save its CPU; the PL has the time.

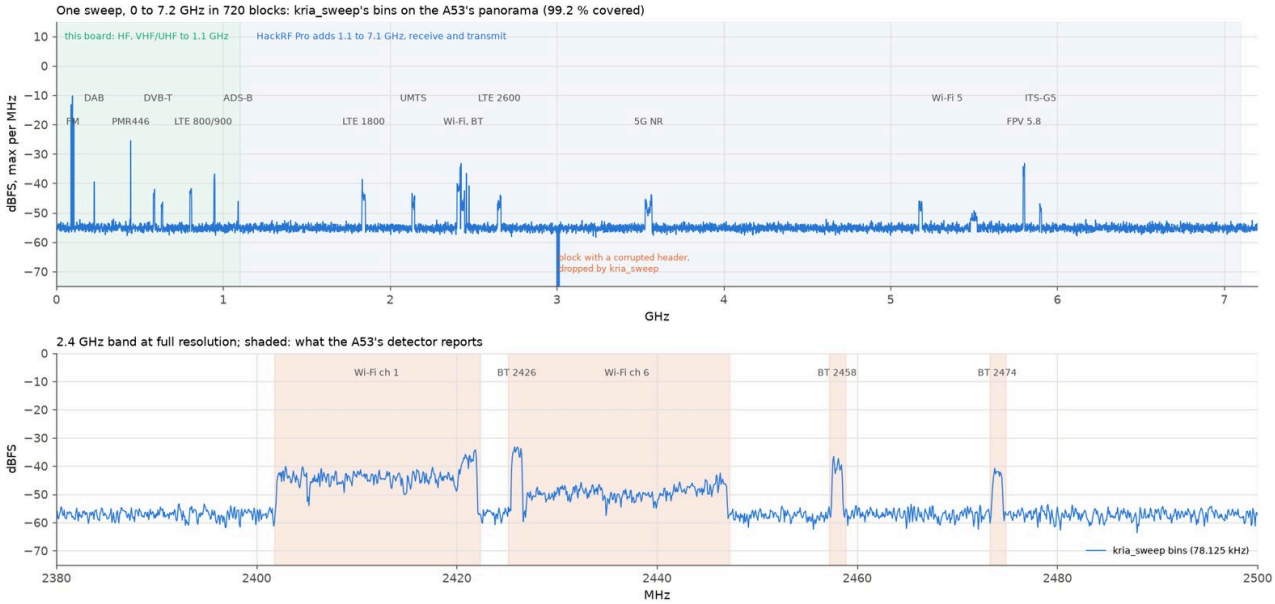
Transmit. `kria-sdrd` keys the HackRF only while R5F core 0's interlock reports `transmit` (§7: licence, vehicle stopped, time-out, link up) and only inside the bands of the licence (`TxGate`, the amateur allocations of ITU Region 1 from 1.24 to 5.85 GHz). The HackRF's port is a second transmitter on the same lock, not a way around it.

10.1 End-to-end test

- **The capture** (`sw/integrations/hackrf_sim.py`): one sweep from 0 to 7.2 GHz, 720 blocks, as libhackrf delivers them. The scene is a car's radio environment: five FM stations, DAB, two DVB-T multiplexes, PMR446, LTE at 800, 900, 1,800 and 2,600 MHz, UMTS, ADS-B, 5G NR at 3.5 GHz, Wi-Fi at 2.4 and 5 GHz, three Bluetooth hops, a 5.8 GHz video link and ITS-G5, 25 signals from −9 to −38 dBFS. The baseband filter is 15 MHz wide. Block 300's header is corrupted on purpose.
- **The A53** (`kria-sdrd hackrf-pre`) writes its driver's register writes and the blocks for the PL, and from its bit-exact model of `kria_sweep` the 46,735 output beats the PL must return.
- **The RTL** (`tb_kria_sweep`) takes 1.47 million input beats with gaps and back-pressure on its output. Every output beat equals the model's, the block with the bad header is dropped and counted (`BAD` = 1, `BLOCKS` = 719). Mutation `sweep_twiddle_conj`, the conjugate twiddle, fails at the first block.
- **The A53 again** (`kria-sdrd hackrf-post`) places the RTL's bins on the panorama, finds the signals (power averaged over 700 kHz, 5 dB above the median floor, runs less than 1 MHz apart joined), checks the transmit gate, and writes the record the Wideband screen draws.

Result	Value
Range covered by one sweep	99.2 % of 0 to 7.25 GHz (the dropped block's 10 MHz missing)

Result	Value
Signals of the scene found	**25 of 25**, with no false detection
The same with one FFT per block, as `hackrf_sweep`	25 of 25 at 5 dB but 28 false detections; at 8 dB 24 found and the wide signals in fragments
Carriers	within 0.1 MHz (FM, PMR446), level within 1.3 dB
Wide signals	Wi-Fi 20.2 MHz wide, FPV 8.6 MHz, LTE 800 9.5 MHz; their peak bin is 10 to 15 dB below the total power, which is spread over the channel
Transmit gate	2,400.1 MHz keyed; the same while moving, blocked by the interlock; 2,412 MHz keyed (inside 2,300 to 2,450); 5,760.1 MHz keyed



HackRF Pro end to end: the sweep from 0 to 7.2 GHz, and the 2.4 GHz band

Not tested: a real HackRF Pro, its gains and its spurs, and the `hw` paths of `kria-sdrd` (the libhackrf calls); the 20 MS/s stream path and the transmit path beyond the gate, which use libhackrf's calls as `hackrf_transfer` does. Bluetooth hops faster than a sweep (1,600 hops a second against 1.7 sweeps a second); the panorama sees a few hops per sweep, and the peak-hold shows the band.

10.2 Both blocks in the K26 build

Both blocks and their DMAs are in the K26 block design (`fpga/kria/bd.tcl`), built on 18 November (**FPGA_GATEWARE.md §3.3**):

Instance	LUT	FF	BRAM36 / 18	DSP
`kria_doa_0`	10,117 (3,200 of them LUTRAM)	2,089	0 / 1	115
`axi_dma_2`	563	841	1 / 1	0
`kria_sweep_0`	1,586	638	2 / 1	8
`axi_dma_3`	1,667	2,415	2 / 2	0
Whole K26 design	**53,336 of 117,120 (45.5 %)**	46,896 (20.0 %)	44.0 eq. (30.6 %), 1 URAM	229 (18.3 %)

- **Timing:** `WNS = +1.043 ns`, `WHS = +0.010 ns` (build of 19 November); the worst path is in the ADS-B receiver, not in the new blocks.
- **Clock-domain crossings:** none added by `kria_doa_0`, `kria_sweep_0`, `axi_dma_2`, `axi_dma_3` or PS `CAN1` EMIO. The four streaming instances run on `clk_pl_0`, the clock of the HP0 and HPM0_LPD ports (**FPGA_GATEWARE.md §3.3**).
- **Addresses**, as Vivado assigned them (the XSA's hardware handoff): `kria_doa_0` `0x8005_0000`, `axi_dma_2` `0x8006_0000`, `kria_sweep_0` `0x8007_0000`, `axi_dma_3` `0x8008_0000`, each 64 KiB, after the existing five slaves at `0x8000_0000` to `0x8004_FFFF`. The overlay (`sw/ias2rf_pl.dtsi`) adds the four nodes and the DMA buffers `kraken_buf` (`0x3EE4_0000`, 512 KiB) and `sweep_buf` (`0x3EF0_0000`, 832 KiB).
- **The first build** put `kria_sweep`'s FFT memory, read at four places at once, in flip-flops and multiplexers: 43,305 LUT for that block alone. The memory is now one block RAM with a write and a read port, six clocks per butterfly; the block fell

to 1,586 LUT, and the benches above were re-run on it.

- **Not done:** `kria_doa`'s steering table stays in LUTRAM; moving it to block RAM would free about 3,200 LUT.

Part III: Schematic Subsystem Specifications

12 technical document(s)

Source: docs/IAS_LINK_SPEC.md

IAS_LINK sheet: specification and review guide

25 September 2026 · `sheets/IAS_LINK.kicad_sch` · *drawn by* `_work/sheets/ias_link.py` *from the connection list in* `_work/sheets/ias_link_spec.py`

The link to the Kria: the Hirose connector on IAS1 with its five LVDS pairs and four single-ended signals, each pair AC-coupled, and the two pairs the FPGA receives terminated here. Plus the IAS0 connector, which is only mechanical.

Everything on this sheet follows **INTERFACE_SPEC.md** §2–§6, which was verified against the carrier schematic (XTP682). This sheet adds no new allocation.

1. What is on the sheet

Part	What
J101	Hirose BM20B(0.8)-34DP on **IAS1** (KV260 J8). Pins as INTERFACE_SPEC §2–§4. Footprint `AVT_KHK_Lib:J-BM20B(0.8)-34DP`, the one in the original layout
J102	The same part on **IAS0** (KV260 J7). The SOM reaches IAS0 only through the carrier's AP1302 (B-01), so the board uses none of its signals: its 11 grounds connected, everything else marked no-connect until Rev08. **Since Rev08** every one of its 34 contacts is wired to the same contact of `J103` (REV08_PLAN §4)
J103	Rev08: BM20B(0.8)-34DS-0.4V(51), the receptacle, on the tongue's top face over `J102`, contact for contact, so an IAS camera module plugs into this board as it would into the carrier's `J7`. Nothing on the board uses its 23 signal nets
C101–C110	100 nF in series on all ten lines (§6.1: the HPA bank is at 1.2 V and the FPGA's LVDS is not). 0 Ω is the alternative stuffing if `VCCO_HPA` turns out to be 1.8 V
R101–R104, C111, C112	On the two pairs the **FPGA receives** (`LINK_TX_D0`, `LINK_TX_CLK`): 10 k from each leg to `+1V2`, decoupled. That restores the common mode the capacitors removed. *Until 12 Nov these were 2 × 49.9 Ω, which also terminated the pair here, 45 mm from the receiver; the termination is now R105/R106 at the FPGA (below, and LAYOUT §6.5)*
R105, R106 (CONTROL sheet)	100 Ω across `LINK_TX_D0` and `LINK_TX_CLK` on the bottom face under the FPGA's balls: the termination, at the receiver

The connector splits every pair across its two rows of pins, so it is drawn with a label on each pin, and the capacitors sit in an orderly block beside it. The carrier's rails on pins 13, 17/18 and 23/24 are left unconnected: the adapter takes no power from the connector (ARCHITECTURE §9.1).

2. Decisions this sheet makes, for your approval

Decision	Evidence	Alternative
Termination and bias for the FPGA-bound pairs at +1V2	An AC-coupled LVDS input needs its common mode restored. The XC7A50T has only HR banks, and those have no internal bias for AC-coupled inputs, so it's external. 1.2 V is the LVDS common mode, and the rail already exists	A resistor divider from another rail
No parts for the Kria-bound pairs beyond the capacitors	Their receiver is inside the SOM, in an HP bank at 1.2 V. UG571 (read 12 Nov, INTERFACE_SPEC §6.3): `LVDS` there would be input-only with no internal termination, but `DIFF_SSTL12` with `ODT = RTT_48` terminates the pair (about 96 Ω) and re-biases it at 0.6 V on the die. The Kria side drives `LINK_TX` as `DIFF_SSTL12` with `RDRV_60_60`	Footprints for an external bias network, fitted only if needed
The single-ended signals pass straight through	`HK_SCL`/`HK_SDA` (14/22), `FPGA_PROG_B` (21) and `FPGA_IRQ` (15) are at the carrier's levels, **1.8 V, verified** in XTP682 (INTERFACE_SPEC §4.3). Translating them belongs next to the FPGA, on CONTROL. Pin 32, first given to FPGA_IRQ, is the carrier's 48 MHz camera clock and is left unconnected	n/a

3. Two things this sheet hands on

- **To CONTROL and POWER: the FPGA's link bank must be at 2.5 V, not 1.2 V.** The FPGA *drives* three of the pairs, and Artix-7 LVDS outputs (`LVDS_25`) need a 2.5 V bank. The power tree's line *"+1V2 → FPGA VCCO, IAS-facing bank"* (ARCHITECTURE §9) doesn't hold for outputs. `+1V2` stays in use, as the termination centre here. **To confirm in UG471** (7 Series SelectIO), not in the repository.
- **To the root:** the old IAS0/IAS1 blocks from Rev01 still hold their own copies of these connectors. They go when the

root is wired, the last step.

4. How the drawing was verified

Check	Result
`_work/check_sheet.py ias_link`: 26 nets exact, 32 no-connects alone, every pin of the 18 parts accounted for	**PASS**
KiCad ERC on the sheet	1 × `power_pin_not_driven` on `+1V2`, until POWER exists

5. How to review this sheet

About 15 minutes.

1. **J101's pins against INTERFACE_SPEC §2–§4.** The connector is drawn with labels, so check each pin's label against the tables. Watch pins 26/27 and 29/30: N comes before P.
2. **§2's decisions**, and **§3's 2.5 V bank**.

```
py _work/check_sheet.py ias_link
```

6. Bring-up: measuring the link on the board

Added 12 November 2026. Nothing here is built yet: it is the test plan for the first boards.

Why not Vivado's IBERT. The IBERT IP, the one that plots 2-D eyes, drives only the gigabit transceivers (GTH/GTY). This link runs on ordinary SelectIO pins through `OSERDESE2`/`ISERDESE2` on the Artix-7 and `ISERDESE3` on the Kria, so IBERT cannot see it. The eye is measured instead with each receiver's input delay line, as a **bathtub curve**: bit errors against the sampling point.

The test.

1. The transmitter sends PRBS7 on every data lane of a direction, with the lane's clock forwarded as usual (source-synchronous DDR, up to 1 Gb/s per lane on a 500 MHz clock).
2. No clock recovery is involved, and the PRBS7 checker locks by itself after seven bits, so no 8b/10b is needed for the test.
3. PRBS7 is balanced enough for the AC-coupling capacitors (C101–C106): its longest run is seven bits. The real traffic still needs 8b/10b or a scrambler (ARCHITECTURE §4.2).
4. The receiver steps its delay line through its whole range, one tap at a time. At each tap it counts errors over a fixed number of bits and stores tap against count.
5. 10^9 bits per tap is one second and resolves a BER of 10^{-9}. Each further decade costs ten times as long.
6. The counts go to the PS on the Kria side (AXI), or over the return channel and the HK bus from the Artix-7 side. Plotted, they make a U: its flat floor, where the count is zero, is the eye's open width at that BER.
7. The gateware keeps the same routine for start-up: centre each lane in its floor, as the ADCR bits are calibrated (CONTROL_SPEC).

Resolution on each side.

Direction	Receiver	Delay line	Step	Points per 1 ns bit
`LINK_RX_*` (FPGA → Kria)	K26, HP bank	`IDELAYE3`, 512 taps, `TIME` mode, up to 1.1 ns	about 2 ps	about 500
`LINK_TX_*` (Kria → FPGA)	XC7A50T, HR bank	`IDELAYE2`, 32 taps, `IDELAYCTRL` at 200 MHz	78 ps	about 13

So the `LINK_TX` bathtub comes out much coarser than the `LINK_RX` one. Both ranges span more than one bit, `IDELAYE3`'s only just: 1.1 ns on UltraScale+ (UG571 Table 2-12).

What it cannot measure.

- **The eye's height.** The delay moves the data against the clock, but the receiver's threshold cannot be moved, so the simulated eye openings in mV cannot be checked this way.
- **The sampling window, separately.** The floor is the bit minus the jitter on the lane minus the input flip-flop's setup and

hold window. Take that window from the data sheets (DS181 for the Artix-7, DS925 for the Zynq UltraScale+ HP banks) before comparing with the simulation.

What to expect, from the board as routed (SIGNAL_INTEGRITY §8, `lvds_eye.py` at 1 Gb/s PRBS7; `lvds_skew.py` for the skew).

Pair	Eye opening, routed / ideal	Zero-crossing spread, routed / ideal	Data − clock skew
`LINK_RX_D0`	457 / 509 mV	31 / 25 ps	+95 ps
`LINK_RX_D1`	372 / 385 mV	51 / 41 ps	+39 ps
`LINK_RX_CLK`	392 / 395 mV	10 / 10 ps	n/a
`LINK_TX_D0`	665 / 674 mV	62 / 64 ps	−40 ps
`LINK_TX_CLK`	643 / 642 mV	63 / 63 ps	n/a

- **The width.** The simulation's spread is the board's own contribution: lossless lines, an ideal driver edge, no crosstalk, no driver or clock jitter. The floor should come out as roughly 1 ns minus that spread minus the receiver's window, and **narrower** by whatever the silicon adds. A floor much narrower than that points at the board: crosstalk, a reflection or a return path.
- **The centres.** The data − clock skew moves each lane's centre. On the Kria side, `LINK_RX_D0`'s floor should sit about 56 ps (95 − 39) away from `LINK_RX_D1`'s, give or take each receiver's own input delay. That is a direct check of the routed lengths.

7. Bandwidth: what the five pairs carry, and how fast they can go

Added 12 November 2026.

Five pairs at 1 Gb/s are not 5 Gb/s of data. Two of the five pairs are the forwarded clocks, one per direction, and carry no data. One data pair runs the other way.

Pair	Direction	Carries	Raw rate
`LINK_RX_D0`	FPGA → Kria	data	1 Gb/s
`LINK_RX_D1`	FPGA → Kria	data	1 Gb/s
`LINK_RX_CLK`	FPGA → Kria	the 500 MHz DDR clock for the two above	n/a
`LINK_TX_D0`	Kria → FPGA	data	1 Gb/s
`LINK_TX_CLK`	Kria → FPGA	its clock	n/a

That makes 2 Gb/s towards the Kria and 1 Gb/s back.

Payload after line coding. The link is AC-coupled (C101–C106), so the stream must be DC-balanced: either 8b/10b, or a scrambler with 64b/66b framing.

Direction	Raw	8b/10b (80 %)	64b/66b (97 %)	Needed	Margin, 8b/10b / 64b/66b
FPGA → Kria	2 Gb/s	1.6 Gb/s	1.94 Gb/s	radar DDC ÷16, one channel, 0.8 Gb/s + two SDR channels of 16-bit I/Q at 3.9 MSPS, 0.25 Gb/s = **1.05 Gb/s**	~35 % / ~45 %
Kria → FPGA	1 Gb/s	0.8 Gb/s	0.97 Gb/s	beam tables, TX baseband, control	n/a

Two radar channels at ÷16 (1.6 Gb/s) would leave no margin under 8b/10b, and 18 % under 64b/66b (ARCHITECTURE §3.2).

How fast the pairs can go. These pins are SelectIO, not transceivers: the K26's GTH lanes do not reach any KV260 connector (BLOCKERS_AND_RISKS, item 3). The silicon sets the ceiling, about **1.25 Gb/s** per pair for the Artix-7 −2 HR banks (DS181) and about **1.6 Gb/s** for the UltraScale+ HP banks in native mode (DS925). Both figures are **to confirm** in those data sheets. Several Gb/s per pair is out of reach on this connector.

The board as routed, simulated at higher rates (`lvds_eye.py`, PRBS7; eye opening, routed / an ideal 100 Ω pair of the same length):

Rate per pair	`LINK_RX_D0`	`LINK_RX_D1`	`LINK_TX_D0`
1.0 Gb/s	457 / 509 mV	372 / 385 mV	665 / 674 mV

Rate per pair	`LINK_RX_D0`	`LINK_RX_D1`	`LINK_TX_D0`
1.25 Gb/s	576 / 581 mV	491 / 524 mV	401 / 401 mV
1.6 Gb/s	271 / 225 mV	**44 / 48 mV**	324 / 328 mV
2.5 Gb/s	0 / 0	0 / 0	0 / 0

The routed pair follows the ideal one at every rate. What closes the eye is the LVDS driver's edges and the receiver's input capacitance, not the copper. The opening also varies non-monotonically with rate, because the reflections of the 2 pF inputs land at different points of the bit. So **the routing holds at 1.25 Gb/s, which is also the silicon's ceiling**. At 1.6 Gb/s `LINK_RX_D1` is nearly closed, even in the ideal case.

If more is ever needed:

- run the pairs at 1.25 Gb/s: 2.5 Gb/s raw towards the Kria, 2.4 Gb/s of payload under 64b/66b;
- add J9, the KV260's 15-pin camera connector: two more data pairs and a clock, on another cable (R-04 in ARCHITECTURE §4.1);
- reduce what crosses the link: decimate further on the Artix-7.

Source: docs/CLOCK_SPEC.md

CLOCK sheet: specification and review guide

23 September 2026 · first sheet drawn for Rev03 · pilot for the drawing method · ***reviewed and accepted 24 September 2026***

`sheets/CLOCK.kicad_sch`, drawn by `_work/sheets/clock.py` from the connection list in `_work/sheets/clock_spec.py`, and checked against that list by `_work/check_sheet.py`.

1. What drawing it changed in the architecture

Drawing this sheet exposed three problems in the clock plan of `ARCHITECTURE.md` §5.3. It had a TCXO, a selector and an ADCLK944 fan-out feeding ADC, DAC, FPGA and a spare output. Each problem was checked against a datasheet before changing anything:

Problem	Evidence	Resolution
A fan-out copies **one** frequency to every output, but the converters run at different rates (AD9484 400 MSPS, AD9253 ≤ 62.5 MSPS, DACs ≤ 125 MSPS)	ADCLK944 has no dividers	The AD9253 **divides its clock internally**, 1 to 8, with inputs up to 1 GHz (AD9253 Rev. D, "Input Clock Divider"). One master clock serves both ADCs
The DACs cannot take a differential LVPECL clock	AD9767 Rev. G Table 6: `CLK1/IQCLK` is a CMOS input; AD9708 likewise	DAC clocks come from the **FPGA**, which sends the DACs their data anyway. `CLK_DAC_P/N` removed from the interface
A TCXO cannot produce 400–500 MHz	TCXOs are tens of MHz	Local master is a **Si549** programmable XO, 0.2–1500 MHz, 95 fs jitter

And one addition: the selector and the fan-out became **one chip, the ADCLK948** (two selectable inputs, eight LVPECL outputs), instead of a separate selector feeding an ADCLK944.

1.1 The frequency plan

Master	AD9484	AD9253 (÷8)	FPGA	Use
400 MHz	400 MSPS	50 MSPS → HF to 25 MHz	400 MHz ref	Radar mode: AERIS-10 runs at 400 MSPS, so its firmware ports unchanged
500 MHz	500 MSPS	**62.5 MSPS → all of HF**	500 MHz ref	SDR mode: the AD9253's full 1-lane rate (B-02), covering to 30 MHz

The Si549 is reprogrammed over I²C to switch between the two. Its **±950 ppm fine-tuning with 100 µs settling** (Si549 Rev. H, DCO) lets the FPGA discipline it to the GPS PPS. That recovers the frequency accuracy the TCXO was there for, and does it better.

1.2 Interface changes

Made by `_work/rev03_clock_interface.py`, then `_work/sync_sheet_pins.py`:

Signal	Change	Why
`CLK_DAC_P/N`	**removed**	DACs take CMOS clocks from the FPGA
`DACS_IQCLK`, `DACS_IQRESET`	**added**, FPGA → AD9767	Interleaved mode needs IQCLK, IQWRT, IQSEL and IQRESET (Table 6); the hierarchy only had two of the four
`CLK_SEL`	**added**, FPGA → CLOCK	Reference select, driven open-drain (§3)
`XO_SCL`, `XO_SDA`	**added**, FPGA → CLOCK	Programs the Si549. 3.3 V levels: its I²C needs VIH ≥ 0.7·VDD, which the Kria's IAS I²C would not give

2. Parts

Ref	Part	Source
U401	ADCLK948BCPZ	Datasheet Rev. B (Internet Archive, `_work/fetch_datasheets.py`)
Y401	Si549, LVPECL, 3.3 V, 5×7 mm, **pinout code C**	Datasheet Revision H. Code C is the Si570-compatible pinout, so the stock KiCad `Si570` footprint fits

Ref	Part	Source
J401, J402	Edge-mount SMA	On the edge the board grows towards (INTERFACE_SPEC §5.3)
FB401 + 25 passives	see `clock_spec.py`	Each with its source

The Si549 is ordered configured. Its part number encodes output format, supply, package, pinout and startup frequency, and Skyworks ships samples in 1–2 weeks. Order it as LVPECL, 3.3 V, 5×7 mm, pinout C, total stability ±25 ppm or better. The startup frequency doesn't matter, because the FPGA sets 400 or 500 MHz at boot.

The ADCLK948 has no stock footprint. Its package (CP-32-21) has a 2.70 mm exposed pad; every stock 5×5 mm LFCSP-32 in KiCad has 3.1 mm or more. Draw one at layout from the package drawing on datasheet page 12.

3. Every value, and where it comes from

Item	Value	Source
ADCLK948 output pull-downs (R404–R411)	200 Ω	Datasheet Figure 17, AC-coupled LVPECL
Output series capacitors (C414–C421)	100 pF	Figure 17: "0.1 nF"
Receiver termination	100 Ω across each pair	Figure 17; drawn on the **consuming** sheet, next to the receiver
Unused outputs Q4–Q7	left open	Output stage is an open emitter (Figure 13): no pull-down, no current
CLK1 input (Si549)	series 100 nF, VT1 tied to VREF1, 100 nF to ground	Figure 21, AC-coupled differential input
CLK0 input (SMA)	series 100 nF; CLK0-bar, VT0 and VREF0 tied, 100 nF to ground	Figure 22, AC-coupled single-ended input
Reference level at J401	0.4 – 3.4 Vpp	Table 1, input differential range. 50 Ω on chip
Si549 source pull-downs (R402, R403)	130 Ω	Si549 Figure 4.1, AC-coupled LVPECL at VDD 3.3 V
Si549 I²C pull-ups (R413, R414)	4.7 kΩ to VDD	Si549: "must be connected to VDD via an external pull-up"
`IN_SEL` pull-up (R401)	10 kΩ	Table 3: logic 1 ≥ VCC − 0.4 V, and **0.6 mA flows out at logic 0**, so there is an internal pull-up. Default (open) = CLK1 = the Si549. The FPGA drives it open-drain, so the high level is exactly VCC
ADCLK948 decoupling	6 × 1 nF, one per VCC pin; 1 µF; 10 µF	Datasheet p.10

Judgement calls, not from a datasheet, which deserve the hardest look:

Item	Choice	Reasoning
FB401	ferrite, 220 Ω @ 100 MHz, 2 A, ≤ 0.1 Ω (HCB1608KF-221T20)	Keeps +3V3_D switching noise off the clock chips. The branch draws up to 483 mA (drops 48 mV max at rated load while attenuating the 580 kHz buck ripple to 0.1–0.4 mVpp; **history/ REV06_REVIEW §3**, **`sim/fb401_filter.png`**)
C401	10 µF ceramic	The datasheet mentions a 1 µF electrolytic for bulk; a ceramic does the same job with lower ESR
C422	100 nF at the Si549	Its datasheet gives no decoupling recommendation
R412	49.9 Ω on Q3-bar	Loads Q3-bar like the instrument loads Q3 on J402, so the pair stays balanced
C409–C413	100 nF	Figures 21 and 22 show the capacitors without a value

4. How the drawing was verified

Check	Result
`_work/check_sheet.py clock`: all 30 specified nets exist with **exactly** their pins; interface nets carry their labels; the 10 no-connects are alone; all 119 pins of the 41 parts accounted for; no part missing or extra	**PASS**
The same check with one wire deleted on purpose	Fails, naming the pin: `CLK1_P: not connected: ['U401.5']`: the check can see an error

Check	Result
KiCad ERC on the sheet	2 errors, both "power input not driven" on `+3V3_D` and `GND`: nothing drives them until the POWER sheet exists. 6 warnings, `isolated_pin_label` on the clock outputs, until the receiving sheets are drawn
Pin tables of the two new symbols	Si549 agrees with KiCad's stock Si570 pin for pin. The ADCLK948 has **no independent second source**, only its datasheet's own Figure 2 and Table 7, which agree

The fan-out on the right is drawn so no lines cross: lines that rise turn top-first, lines that fall turn bottom-first.

---

5. How to review this sheet

Open the project in KiCad and go into the CLOCK sheet. Keep this document and the two datasheets next to it (`_work/datasheets/`, fetched by `_work/fetch_datasheets.py`). About 30 minutes.

1. **The plan (§1).** Do 400/500 MHz and dividing inside the AD9253 fit what you want from the SDR? That's the decision everything else hangs on.
2. **U401's pin numbers against the datasheet.** Page 6, Figure 2 and Table 7. This is the part with no second source. Check CLK0/CLK1, VREF/VT, IN_SEL, and that each `Qn` (true) sits on the higher of its two pin numbers.
3. **The two input networks against Figures 21 and 22** (page 11). CLK1 is differential; CLK0 is single-ended, with CLK0-bar tied to VT0 and VREF0.
4. **One output block against Figure 17** (page 9). The other three are identical.
5. **The judgement calls in §3.** They're the ones not backed by a datasheet.
6. **Anything that reads badly.** Layout, labels, where text lands. Fix that directly in KiCad: from now on the `.kicad_sch` is the source, and the generator is not re-run over hand edits.

To confirm the wiring after you've touched it:

```
py _work/check_sheet.py clock
```

Source: docs/ADC_RADAR_SPEC.md

ADC_RADAR sheet: specification and review guide

24 September 2026 · `sheets/ADC_RADAR.kicad_sch` · *drawn by* `_work/sheets/adc_radar.py` *from the connection list in* `_work/sheets/adc_radar_spec.py`

The radar receive path: the 120 MHz IF from AERIS-10 into the AD9484, through two AD8352 drivers. It is AERIS-10's own Main Board circuit (ARCHITECTURE §7.1: *"replicated on the adapter board"*), rebuilt from the datasheets and checked part by part against AERIS's schematic (`_work/aeris_reference_circuit.py U1 U4 U8`).

```
IF_RX_B ──► U502 AD8352 ──► U503 AD8352 ──► U501 AD9484 ──► 10 LVDS pairs to the FPGA
single-ended   single-ended in,  differential,    8 bits,
50 ohm         15 dB             10 dB            400 / 500 MSPS
```

Rev08 (16 November 2026). The AD9484 now has a third source: SW2's second throw carries the VHF/UHF front end's IF from `J961` (**ROUTING_SPEC** §1.2, **RX_VU_SPEC**). Nothing on this sheet changed. In the 500 MHz mode the G-7 path D2 samples it at 500 MSPS (**FPGA_GATEWARE** §4.3).

1. What drawing it changed

1.1 CONVERTERS became four sheets

The CONVERTERS sheet would have held about 200 parts, more than one review can check properly. It is now `ADC_RADAR`, `ADC_SDR`, `DAC_RADAR` and `DAC_SDR`, each about the size of CLOCK. The split is clean because the interfaces separate: the ADCs have the SPI bus and the LVPECL clocks, and the DACs have parallel CMOS buses. Done by `_work/rev03_split_converters.py`; `hier_label_mismatch` stays at

1. The root page went from A3 to A2 to make room for the four blocks.

1.2 Interface changes

Signal	Change	Why
`IF_RX_A_P/N` … `IF_TX_B_P/N`	**became `IF_RX_A`, `IF_RX_B`, `IF_TX_A`, `IF_TX_B`, single-ended 50 Ω**	What carries them is single-ended: the M3SWA2 routing switches (SPDT, one RF path each) and the SMAs. Eight differential lines could never have gone through four SPDTs. The AD8352 takes a single-ended input by itself (its datasheet, Figure 26), so the receive side needs no balun; the DACs will drive one
`ADCR_D_P[7..0]`, `ADCR_D_N[7..0]`	**became `ADCR_D0_P` … `ADCR_D7_N`**, one label per line	As the `ADCS_*` lines already were. The drawn sheet then has no bus, and `check_sheet.py` checks every line by name

1.3 Decisions this sheet makes, for your approval

Decision	Evidence	Alternative
Two AD8352s in cascade, 15 + 10 dB = 25 dB	AERIS-10 does exactly this: U8 with RG 56 Ω (15 dB), then U4 with RG 115 Ω (10 dB)	One stage (fewer parts, 37 mA less) if the IF arriving here is stronger than at AERIS's own ADC. Changing it is a resistor value; removing a stage is a redraw
The first stage takes the single-ended values (Table 7: RG 68 Ω, CD 0.6 pF), not AERIS's differential ones (Table 5: RG 56 Ω)	AERIS feeds its first stage differentially from the mixer; this board gets the IF through a single-ended switch	n/a
The AD8352s run at 5 V, not 3.3 V	The datasheet characterises the part at 5 V only (Table 1); 3 V is merely inside the allowed range. AERIS runs its two at 5 V. The power budget moved them from `+3V3_A` to `+5V0`	3.3 V saves ~0.1 W but runs on uncharacterised distortion
ENB tied to VCC, PWDN tied to ground	The AD8352 evaluation board ties ENB to the supply (R10). The AD9484 powers down through SPI (register 0x08) as well as the pin	AERIS drives both from the FPGA (`EN_OPAMP_IF_*`, `ADC_PWRD`). Three more FPGA lines to save ~0.9 W when the radar is idle. Say if you want them

1.4 Two requirements this sheet puts on CONTROL

- **`CONV_SPI_*` must be 1.8 V signals.** The AD9484's logic pins have an absolute maximum of DRVDD + 0.2 V = 2.0 V

(datasheet, Absolute Maximum Ratings). A 3.3 V FPGA bank would damage it. AERIS scales its PWDN line with a 830 Ω / 1 kΩ divider for the same reason. The FPGA drives the SPI from a 1.8 V bank, or through a translator.

- **The LVDS pairs are terminated at the receiver, 100 Ω each** (AD9484 p.16: *"as close to the receiver as possible"*): in the FPGA (`DIFF_TERM`) or as resistors on CONTROL. AERIS uses resistors (R2–R12).

2. Parts

Ref	Part	Footprint	Note
U501	AD9484BCPZ-500	**custom**	CP-56-5 has a **5.10 mm** exposed pad (Figure 40). KiCad's 8×8 mm 56-pin parts have 6.6 mm or 5.1×4.96 mm. Draw it at layout, like the ADCLK948's
U502, U503	AD8352ACPZ	`Package_CSP:LFCSP-16-1EP_3x3mm_P0.5mm_EP1.6x1.6mm`	CP-16-22: 1.60 mm pad, matches
FB501–FB503 + 51 passives	see `adc_radar_spec.py`	0402, bulk 0805, ferrites 0603	Each with its source

The two datasheets are in the AERIS-10 repository, not in `_work/datasheets/`: The PLFM_RADAR repository's `7_Components Datasheets and Application notes/AD9484/` holds `AD9484.pdf` (Rev. A), `ad8352.pdf` (Rev. C) and the AD9484 evaluation board schematic.

3. Every value, and where it comes from

Item	Value	Source
Input termination R501	64.9 Ω	AD8352 Figure 26: 65 Ω
RN R502, VIP to RGN	200 Ω	AD8352 Figure 26 and text: *"an external resistor (RN) of 200 Ω is added between VIP and RGN"* to balance the outputs
VIN to ground R503, through C502	24.9 Ω	AD8352 Figure 26: 25 Ω
Stage 1 RG / RD / CD	68 Ω / 4.3 kΩ / 0.6 pF	AD8352 **Table 7**, 15 dB, single-ended, 200 Ω load
Stage 2 RG / RD / CD	115 Ω / 4.3 kΩ / 0.2 pF	AD8352 **Table 5**, 10 dB, differential, 200 Ω load. Same as AERIS R14, R15, C43
VCM decoupling C504, C513	100 nF	AD8352 Table 4: *"typically decoupled to ground with a 0.1 µF capacitor"*
Coupling capacitors C501, C502, C507, C508, C510, C511, C516, C517	100 nF	AD8352 Figure 26, AD9484 Figure 30
Load legs R506/R507, R510/R511	200 Ω	AD9484 Figure 30
Centre-tap capacitors C509, C518	100 nF	AD9484 Figure 30
Series R512, R513	24 Ω	AD9484 Figure 30 shows *R* without a value; 24 Ω is AERIS's (R1, R13) and the AD8352 datasheet's (p.14: *"the output 24 Ω resistors provide isolation"*)
Shunt C519 across VIN±	2.7 pF	AD9484 Figure 30 shows *C*, *"dependent on the input frequency"*; 2.7 pF is AERIS's (C3), at the same 120 MHz IF
Clock termination R514	100 Ω	ADCLK948 Figure 17 and AD9484 Figure 31: 100 Ω across the pair at the receiver. AERIS R173
VREF R515	20 kΩ to ground	AD9484 p.17: internal reference = *"pin is connected to 20 kΩ to ground"*. AERIS R38
AVDD, DRVDD decoupling	11 + 3 × 100 nF, one per pin; 10 µF per rail	AD9484 evaluation board: C320–C333 (AVDD, 11), C323/C327/C328 (DRVDD, 3), C314/C315
AD8352 decoupling	2 × 100 nF per device, 10 µF shared	AD8352 evaluation board: C6, C7, C1

Judgement calls, not taken from a datasheet:

Item	Value	Reasoning
FB501, the drivers' ferrite	600 Ω at 100 MHz, ≥ 0.5 A	Isolates the RF drivers from the `+5V0` buck. 78 mA flows through it
FB502, FB503, the ADC's ferrites	220 Ω at 100 MHz, ≥ 1 A, DCR ≤ 0.1 Ω	The evaluation board has a ferrite per rail (E302, E303, *"50 ohms"*) without a part number. At 300 mA and 0.1 Ω, AVDD drops 30 mV and stays inside 1.7–1.9 V. Since 12 Nov +1V8_A starts at 1.85 V, to cover the copper's drop on the way as well (SIGNAL_INTEGRITY §9.1)

Item	Value	Reasoning
CML joined to the centre tap	as Figure 30	**AERIS leaves CML open** and only decouples the centre tap. CML is an output that the SPI enables; while disabled it does nothing, and enabled it biases the inputs where the ADC wants them. Following the datasheet costs nothing
Load tables for 200 Ω	Tables 5 and 7	The stages actually see about 300–350 Ω (400 Ω of load legs in parallel with the next input). The datasheet says to interpolate between its 200 Ω and 1 kΩ tables; AERIS uses the 200 Ω values on the same circuit

Signal level, for orientation: the AD9484's full scale is 1.5 V p-p differential. With 25 dB of gain that is about 84 mV p-p at `IF_RX_B`, **roughly −17 dBm** into 50 Ω. That ignores the small losses in the coupling and the 24 Ω/2.7 pF network, so it is an approximation.

4. How the drawing was verified

Check	Result
`_work/check_sheet.py adc_radar`: all 61 specified nets exist with **exactly** their pins; interface nets carry their labels; power nets their names; the 9 DNC pins are alone; all 199 pins of the 57 parts accounted for; no part missing or extra	**PASS**
The same check with the wire from RN to the RGN line deleted on purpose	Fails, naming the pins: `S1_RGN: not connected: ['R504.1', 'U502.3']`
KiCad ERC on the sheet	3 × `power_pin_not_driven` (`+5V0`, `+1V8_A`, `+1V8_D`, until POWER exists); 2 × `pin_not_driven` (SCLK and CSB, until CONTROL drives them); 23 × `isolated_pin_label` on the outputs and SPI, until the root is wired
Pin tables	AD9484 and AD8352 both cross-checked against a second source (`_work/crosscheck_pinouts.py`: no conflicts). Their symbols were only **rearranged** for this sheet, not renumbered

Why the pin order of the AD8352 symbol looks odd. Down the left it reads VIP, RGN, RGP, RDP, RDN, VIN, which is not the chip's order. Each pair that takes a part is exactly one resistor length (7.62 mm) apart, so RN, RG, RD and CD each sit straight across their two pins, and nothing crosses. ENB sits on top next to VCC, which is what it is tied to. The pin **numbers** are unchanged: check them, not their position.

The ERC total moved from 500 to 672, and not because of this sheet. After the split, KiCad started reporting 144 sheet pins in the root as not connected, including CLOCK's and IAS_LINK's, which it had not reported before. They are genuinely unconnected, because the root gets wired last. Why KiCad did not count them before is **not established**.

5. How to review this sheet

Open the project in KiCad and go into ADC_RADAR. Keep this document and the two datasheets (§2) next to it. About 40 minutes.

1. **The decisions in §1.3.** The IF single-ended, the 25 dB split over two stages, 5 V on the drivers, and dropping the FPGA's control of ENB and PWDN. These are yours to accept.
2. **U501's pins against AD9484 Table 7** (p.8): VIN± 35/36, CML 40, VREF 31, CLK± 44/45, SDIO/SCLK/CSB 25/26/27, PWDN 29, and that each output's true pin (+) goes to the `_P` label.
3. **Stage 1 against AD8352 Figure 26** (p.12) **and Table 7** (p.13): RN from VIP to **RGN** (not RGP), 65 Ω termination on the source side of C501, 25 Ω on VIN.
4. **The interstage and output networks against AD9484 Figure 30** (p.15). Stage 2 against AD8352 Table 5 (p.11).
5. **The judgement calls in §3.**
6. **Anything that reads badly.** Fix it directly in KiCad. From then on the `.kicad_sch` is the source, and the generator is not re-run over hand edits.

To confirm the wiring after you've touched it:

```
py _work/check_sheet.py adc_radar
```

Source: docs/ADC_SDR_SPEC.md

ADC_SDR sheet: specification and review guide

24 September 2026 · `sheets/ADC_SDR.kicad_sch` · *drawn by* `_work/sheets/adc_sdr.py` *from the connection list in* `_work/sheets/adc_sdr_spec.py`

The SDR receive path: two single-ended inputs into two channels of the AD9253, each through an AD8352. The same method and building blocks as **ADC_RADAR**; read that one first, this document only covers what differs.

```
IF_RX_A ──► U602 AD8352, 12 dB ──► AD9253 channel A ┐
IF_RX_C ──► U603 AD8352, 12 dB ──► AD9253 channel B ┴──► one lane each (ADCS_D0, ADCS_D1) + DCO + FCO
            AD9253 channels C and D unused
```

> **Rev07 (15 Nov).** `IF_RX_C` now arrives through a 30 MHz anti-alias low-pass on the ROUTING sheet (ROUTING_SPEC §1.1, SIGNAL_INTEGRITY §9.9): channel B is the HF input. Channel A stays wideband.

1. Decisions this sheet makes, for your approval

Decision	Evidence	Alternative
Two channels, not one. A second SDR input, **`IF_RX_C`**, is added to the interface (and `IF_TX_C` for the AD9767's second DAC)	The interface already carried two data lanes (`ADCS_D0`, `ADCS_D1`), and ARCHITECTURE §5.1 had "2 of 4 channels"; but only one analogue input existed. Two channels give diversity, two antennas, or I/Q from a quadrature front end	One channel: drop U603 and its network, and the second lane
AD8352 drivers, as on the radar chain	One verified part for both ADCs, and a single-ended input without a balun. The AD9253 datasheet recommends a transformer for the best SNR (p.22); but a transformer gives no gain and most cut off above 100 kHz, which loses the bottom of HF. The SDR front end has its own LNA	A wideband 1:1 transformer (Mini-Circuits' T1-1T class reaches down to about 100 kHz; check the exact part): cheaper and quieter, no gain
12 dB per channel (Table 7: RG 120 Ω)	Full scale (2 V p-p) at about 0.5 V p-p in, **roughly −2 dBm**, a sensible top for an HF SDR behind an LNA	Any row of Table 7; one resistor per channel
Channels C and D unused, inputs tied to VCM	Their outputs are left open and they are powered down through SPI. Held at VCM, their inputs sit at the common mode with no differential signal	Leave them floating. The datasheet does not say either way
SYNC tied low	One ADC, so its clock divider has nothing to line up with	An FPGA line, if a second AD9253 is ever added

2. What differs from ADC_RADAR

- **The inputs need a bias.** The AD9253's analogue inputs *"are not internally dc-biased"* (p.22). The centre tap of each channel's load legs goes to the ADC's **VCM** output through 200 Ω, and VCM is decoupled at the pin, as in AD9253 **Figure 58**. On the AD9484 the inputs bias themselves.
- **Series resistors and shunt capacitor from AD9253 Figure 58:** 33 Ω per leg, 5 pF across.
- **One-lane mode**, set by SPI (register 0x21). In one-lane mode, channel A comes out on **D0±B** (pins 24/23) and channel B on **D1±B** (22/21), per Table 8 and its footnote 1. The sample rate must then be ≤ 62.5 MSPS, which is the 500 MHz master clock divided by 8.
- **Reference:** SENSE to ground selects the internal 1.0 V reference (Table 9). VREF is decoupled with 1 µF ‖ 0.1 µF, and RBIAS takes 10 kΩ 1 % (p.38, Table 8).
- **The footprint is stock:** CP-48-13 has a 5.60 mm pad (Figure 77), matching KiCad's `QFN-48-1EP_7x7mm_P0.5mm_EP5.6x5.6mm`.
- **A symbol layout was added for the AD9253**, like the AD9484's. It puts channel A at the top of the left side and channel B at the bottom, so each chain runs in without crossing the clock and SPI wires. The pin numbers are unchanged.

Every value, with its source, is in `adc_sdr_spec.py`. The judgement calls are the ferrites, as on ADC_RADAR, and the decisions in §1.

3. How the drawing was verified

Check	Result
`_work/check_sheet.py adc_sdr`: 55 nets exact, labels and rails named, 12 unused outputs alone, every pin of the 63 parts accounted for	**PASS**
KiCad ERC on the sheet	2 × `pin_not_driven`, SCLK and CSB, until CONTROL drives them. The rails' "not driven" errors show once for the whole design, on ADC_RADAR

4. How to review this sheet

About 30 minutes, with `_work/datasheets/AD9253.pdf` and `ad8352.pdf` (§2 of ADC_RADAR_SPEC).

1. **§1's decisions**, especially the second channel and the AD8352s instead of a transformer.
2. **U601's pins against Table 8** (p.12). The one-lane pins are the ones to check: 24/23 and 22/21, and that 28–25 and 16–9 are the unused ones.
3. **One channel's input network against AD8352 Figure 26 and AD9253 Figure 58** (p.23). The other channel is identical.
4. **The reference pins:** SENSE, VREF, RBIAS and VCM against p.38.

```
py _work/check_sheet.py adc_sdr
```

Source: docs/DAC_RADAR_SPEC.md

DAC_RADAR sheet: specification and review guide

24 September 2026 · `sheets/DAC_RADAR.kicad_sch` · *drawn by* `_work/sheets/dac_radar.py` *from the connection list in* `_work/sheets/dac_radar_spec.py`

The radar chirp DAC: AERIS-10's AD9708 and its reconstruction filter, with a balun added so the output is single-ended 50 Ω like everything the routing switches carry.

```
DACR_D0..7, DACR_CLK ──► U701 AD9708 ──► 50 Ω loads ──► LC filter (AERIS-10) ──► T701 balun ──► IF_TX_B
(FPGA, 3.3 V CMOS)       8 bits, 20 mA                  differential, 5 poles     2:1 Z         50 Ω
```

1. Decisions this sheet makes, for your approval

Decision	Evidence	Alternative
Internal 1.2 V reference, not AERIS's arrangement	AERIS ties REFLO to AVDD, which disables the internal reference, and REFIO to +3.3 V. That makes 3.3 V the reference input, but the datasheet allows **0.1–1.25 V** there (Table 1, *Reference Input, Input Compliance Range*). Here REFLO goes to ACOM and REFIO gets its 0.1 µF, as the pin description says. **Worth telling the AERIS-10 author**: it may explain a lower-than-expected full scale on their board	n/a
20 mA full scale (RSET = 1.91 kΩ)	I_OUTFS = 32 × V_REFIO / RSET (Table 1 note 2). 20 mA is the maximum and gives the most output. Across 49.9 Ω that's 1.0 V, inside the 1.25 V output compliance	A larger RSET for less output: 3.83 kΩ gives 10 mA
A 5th-order Butterworth for 100 Ω, −3 dB at 50 MHz (13 Nov), same topology and footprints as AERIS-10's filter	Here the filter sits between 100 Ω differential at both ends: R702 + R703 at the DAC, and the 50 Ω line seen through T701's ratio of 2. AERIS-10's values (fitted as 110 nH / 110 pF) sag **2.0 dB** between 10 and 45 MHz in that termination (−3 dB at 70 MHz, −24 dB at 100 MHz). An independent review found this (docs/RF_REVIEW_EXTERNAL.md M1) and the ABCD model confirms it. New values, all E24, same parts and topology: C707/C708 22 pF to ground (11 pF differential) plus **C709 8.2 pF**, **L701–L704 270 nH** (Murata LQW18ANR27G, ±2 %), **C710 62 pF**, **C711 20 pF**. Response: flat to 30 MHz, −0.4 dB at 40, −3.4 dB at 50, −31 dB at 100, −40 dB at 125 MHz (the image of a 0–40 MHz tone clocked at 125 MSPS). The inductors' 3.4 Ω DCR, two per leg, costs about 0.6 dB flat	AERIS's values: wider passband (to ~65 MHz) but with the sag
A balun after the filter (T701)	The routing switch and the SMAs are single-ended; AERIS fed its mixer differentially	Keep the output differential and route it as a pair. That breaks the single-ended interface of §1.2 of ADC_RADAR_SPEC
Series resistors on the data lines sit on CONTROL, not here	A series resistor terminates the line at its *source* (the FPGA). AERIS uses 22 Ω (R23–R30); the datasheet suggests 20–100 Ω (p.9)	n/a
SLEEP tied low	It has an internal pull-down (pin 15); AERIS drives it from the FPGA	One more FPGA line

T701 is a Mini-Circuits ADT2-1T+ (chosen at layout, 25 Sep; **LAYOUT.md** §5). Its datasheet gives an impedance ratio of 2 (secondary/primary), 50 Ω, 0.4–450 MHz. The 100 Ω secondary (pins 6 and 4) takes the filter's differential output, the primary (3 to the line, 1 to ground) drives the 50 Ω single-ended line. The centre tap (5) is unused. The symbol is new, from the datasheet's Pin Connections table.

2. Every value, and where it comes from

Item	Value	Source
COMP1 to AVDD, C701	100 nF	Pin 19: *"Add 0.1 µF to AVDD for optimum performance"* (AERIS C39)
COMP2 to ACOM, C706	100 nF	Pin 23: *"Decouple to ACOM with 0.1 µF"* (AERIS C38)
REFIO, C705	100 nF	Pin 17: *"Requires 0.1 µF capacitor to ACOM when internal reference activated"*
RSET, R701	1.91 kΩ 1 %	32 × 1.20 V / 1.91 kΩ = 20.1 mA
Loads, R702/R703	49.9 Ω	AERIS R115, R116 (50 Ω)
Filter	22 p (×2, to ground), 8.2 p, 270 nH, 62 p, 270 nH, 20 p	100 Ω Butterworth, §1; topology from AERIS C308/C309, C127, L22/L25, C141, L26/L27, C59 (`_work/aeris_reference_circuit.py L26 L27 C141`)

Item	Value	Source
AVDD decoupling	10 µF + 100 nF	Figure 22 (bulk) and p.10 (*"as close to the chip as physically possible"*)
DVDD decoupling	100 nF	p.10

The symbol is new. KiCad's `Video:AD9708AR` has the right numbers, but it leaves out the NC pins and its layout forced crossings around the reference pins. The project symbol is transcribed from the datasheet's pin table (Rev. B). It agrees with KiCad's on all 21 pins they share; the 7 NC pins are marked as settled in `_work/crosscheck_pinouts.py`. The footprint is the stock `SOIC-28W_7.5x17.9mm`, which matches R-28 (body 17.70–18.10 × 7.40–7.60 mm).

3. How the drawing was verified

Check	Result
`_work/check_sheet.py dac_radar`: 23 nets exact, 7 NC pins alone, every pin of the 20 parts accounted for	**PASS**
`_work/crosscheck_pinouts.py`	AD9708AR against KiCad's own symbol: 21 of 21 shared pins agree
KiCad ERC on the sheet	9 × `pin_not_driven` (the 8 data inputs and the clock, until CONTROL drives them); 2 × `power_pin_not_driven` (`+3V3_A`, `+3V3_D`, until POWER exists)

4. How to review this sheet

About 20 minutes, with `AD9708.pdf` from the AERIS-10 component folder.

1. **§1's decisions**, the reference above all. It is the one place this sheet departs from AERIS-10 on purpose.
2. **U701's pins against the Pin Function Descriptions** (p.4).
3. **The filter against AERIS's schematic**, part by part, with the script above.
4. **T701**: the ADT2-1T+ pin mapping above, against its datasheet.

```
py _work/check_sheet.py dac_radar
```

Source: docs/DAC_SDR_SPEC.md

DAC_SDR sheet: specification and review guide

25 September 2026 · `sheets/DAC_SDR.kicad_sch` · *drawn by* `_work/sheets/dac_sdr.py` *from the connection list in* `_work/sheets/dac_sdr_spec.py`

The SDR transmit DAC: the dual 14-bit AD9767 in interleaved mode, each DAC through the same output network as **DAC_RADAR** (loads, AERIS-10's filter, balun).

```
DACS_D0..13 + IQWRT/IQSEL/IQCLK/IQRESET ──► U801 AD9767 ─┬─ DAC1 ──► filter ──► T801 ──► IF_TX_A
(FPGA, 3.3 V CMOS, one 14-bit port)       interleaved    └─ DAC2 ──► filter ──► T802 ──► IF_TX_C
```

Datasheet: AD9763/AD9765/AD9767 Rev. G, `_work/datasheets/AD9767.pdf`.

1. Decisions this sheet makes, for your approval

Decision	Evidence	Alternative
Interleaved mode (MODE low)	The interface already carried one 14-bit bus plus `IQWRT`, `IQSEL`, `IQCLK` and `IQRESET`, which is what interleaved mode uses (p.25, *Interleaved Mode Timing*). It needs 18 FPGA lines instead of 32	Dual-port mode: two 14-bit buses, 14 more FPGA lines
Port 2's data pins tied to ground	Unused in interleaved mode; CMOS inputs should not float. The datasheet doesn't say either way	n/a
Independent gain (GAINCTRL low), one full-scale network per DAC	p.22, *Gain Control Mode*. Each DAC can then be trimmed on its own; identical values here	Master/slave (GAINCTRL to AVDD): one RSET for both
10 mA full scale, RSET 3.83 kΩ	p.24: *"optimum distortion performance ... when the maximum full-scale signal at IOUTA and IOUTB does not exceed 0.5 V"*. 10 mA on 49.9 Ω is 0.5 V. Keeps the loads, filter and balun of DAC_RADAR	20 mA (1.91 kΩ): 6 dB more output, more distortion
The 256 Ω + 22 nF network on each FSADJ	p.22: *"To ensure that the AD9763/AD9765/AD9767 performs properly, connect a 22 nF capacitor and 256 Ω resistor network ... from the FSADJ1 terminal to ground and from the FSADJ2 terminal to ground"* (Figure 59). The note under Figure 58 says it isn't needed with RSET = 2 kΩ; the text is the stronger statement, and the network costs two parts	Leave it out
The same filter as the radar DAC	The 100 Ω Butterworth of **DAC_RADAR** §1 (13 Nov; AERIS-10's values sagged 2 dB in this termination): C811/C812 and C831/C832 22 pF, C813/C833 8.2 pF, L811–L814 and L831–L834 270 nH, C814/C834 62 pF, C815/C835 20 pF. Flat to 30 MHz, −3 dB at 50 MHz, the right place for a DAC clocked up to 125 MSPS; one design for both. The SDR's own band plan may want its own later	A filter for the SDR transmit band
SLEEP tied low	It has an active pull-down (p.25); FPGA control not needed	An FPGA line

T801 and T802 are ADT2-1T+, wired as T701 on **DAC_RADAR**.

2. Other values

Item	Value	Source
REFIO, C801	100 nF	p.22: *"simply decouple the REFIO pin to ACOM with a 0.1 µF capacitor"*
AVDD, DVDD1, DVDD2 decoupling	100 nF per pin, 10 µF per rail	As the other converters
Supplies	AVDD on `+3V3_A`, DVDD on `+3V3_D`	Table 1: AVDD 3.0–5.5 V, DVDD 2.7–5.5 V
Footprint	`LQFP-48_7x7mm_P0.5mm`	48-lead LQFP

A symbol layout was added for the AD9767, like the others: port 1 and the IQ controls at the top of the left side, every tied-low pin in one block under them (grounded by one bus), and each DAC's outputs 15.24 mm apart on the right. The pin numbers are unchanged.

3. How the drawing was verified

Check	Result
`_work/check_sheet.py dac_sdr`: 40 nets exact, every pin of the 37 parts accounted for	**PASS**
KiCad ERC on the sheet	18 × `pin_not_driven`: the 14 data lines and 4 IQ controls, until CONTROL drives them

4. How to review this sheet

About 25 minutes.

1. **§1's decisions**: interleaved mode and the 10 mA full scale.
2. **U801's pins against the Pin Function Descriptions** (p.10): port 1 on 1–14, the IQ controls on 17–20, MODE 48, GAINCTRL 42, the outputs 46/45 and 39/40.
3. **The FSADJ networks against Figure 59** (p.22).
4. **One output chain against DAC_RADAR's.** The other is identical.

```
py _work/check_sheet.py dac_sdr
```

Source: docs/ROUTING_SPEC.md

ROUTING sheet: specification and review guide

25 September 2026 · `sheets/ROUTING.kicad_sch` · *drawn by* `_work/sheets/routing.py` *from the connection list in* `_work/sheets/routing_spec.py`

Four M3SWA2-34DR+ SPDT switches between the converters and the SMAs. Each converter port goes by default to its own chain, and on command to the other one. The second SDR channels go straight to their SMAs.

Switch	Converter	RF1 (control low, default)	RF2 (control high)	What RF2 enables
SW1 (U901)	`IF_RX_A`, AD9253 ch A	`SDR_RX_A`	`AERIS_IF_A`	Radar IF sampled at 14 bits
SW2 (U902)	`IF_RX_B`, AD9484	`AERIS_IF`	`SDR_RX_WB`; since Rev08 the VHF/UHF front end (§1.2)	Wideband SDR at 400/500 MSPS, 8 bits
SW3 (U903)	`IF_TX_A`, AD9767 DAC1	`SDR_TX_A`	`AERIS_TX_A`	Chirp from the 14-bit DAC
SW4 (U904)	`IF_TX_B`, AD9708	`AERIS_TX`	`SDR_TX_WB`	SDR transmit from the fast 8-bit DAC
n/a	`IF_RX_C`, AD9253 ch B	`SDR_RX_C` (J951)	n/a	n/a
n/a	`IF_TX_C`, AD9767 DAC2	`SDR_TX_C` (J952)	n/a	n/a

1. Decisions this sheet makes, for your approval

Decision	Evidence	Alternative
The switching plan above	ARCHITECTURE §7.4 asked for switches that *"let each converter channel be reassigned between the SDR chain and the radar chain"*, without naming the ports. This is the reading that gives each converter both uses and keeps each one's home chain as the default	A different pairing; it's only labels and SMA names
Ten edge SMAs	Every switch throw and every direct channel gets its own connector	U.FL for internal links. Ten SMAs need edge length the board may not have (INTERFACE_SPEC §5.3)
The interface is single-ended, `SW_CTRL0..3` one label per line	Single-ended, because that is how the M3SWA2 and the SMAs carry it (ADC_RADAR_SPEC §1.2). The control lines come one per label, as on the other sheets	n/a
Pull-down on each control (10 kΩ)	Keeps every switch on its default (RF1) while the FPGA is unconfigured. Control current is below 1 µA low (DC Electrical Specifications)	Pull-up, if the other chain should be the default
DC block on every SMA (100 nF)	Electrical Specifications, note 3: *"All RF-ports must be DC blocked or held at 0 V DC"*. The converter side is already at 0 V: the ADC inputs are terminated to ground and the DAC baluns' secondaries are grounded. The SMA side is whatever is plugged in. 100 nF into 50 Ω gives a 32 kHz corner, below the SDR's 100 kHz	n/a

1.1 Rev07: an anti-alias low-pass on `IF_RX_C` (15 November)

`SDR_RX_C` (J951) is the board's HF receive input: it reaches the AD9253 (channel B) with no RF switch in its path. Between C951 and the sheet's `IF_RX_C` output there is now a 7th-order elliptic low-pass for 50 Ω, flat to 30 MHz and at least 60 dB down from 50 MHz (C953–C959, L951–L953; values and response in SIGNAL_INTEGRITY §9.9, design in `_work/sim/aaf_lpf.py`, drawn by `_work/rev07_aaf.py`). C951's side of the filter is the local net `IF_RX_C_AAF`. `IF_RX_A` stays unfiltered: SW1's RF2 throw brings the radar IF to the same ADC.

1.2 Rev08: the VHF/UHF front end on SW2's second throw (16 November)

SW2's RF2 throw (`U902` pin 10) has two 0402 footprints: `C926` to `J922` (`SDR_RX_WB`) and `C927` to `IF_VU`, the output of the VHF/UHF front end (**RX_VU_SPEC**), which comes in on its own SMA, `J961`, on the back wall. **As built `C927` is fitted and `C926` is not**, so `J922` is unconnected; swapping the two capacitors restores it. `IF_VU` runs 142.3 mm on L6 as stripline (REV08_PLAN §11.6).

2. Every value, and where it comes from

The supply and control parts for each switch are the datasheet's **Figure 2, "Characterization and Application Circuit"** (M3SWA2-34DR+, Rev. B, p.10), part for part:

Item	Value	Datasheet
VDD series R, R9n1	11.5 Ω	R1
VDD decoupling	0.1 µF + 100 pF	C1, C2
VDD zener	5.6 V, SOD-123	D1 (SZMMSZ5232BT1G)
VEE series R, R9n2	11.5 Ω	R2
VEE decoupling	0.1 µF + 100 pF	C4, C3
VEE zener	5.6 V, reversed	D2
VCTRL series R, R9n3	100 Ω	R3
NC pads 1, 12, 13	to ground	*"Not used internally. Connected to ground on test board"*

Truth table (p.3): VCTRL low connects RFC to RF1, high to RF2. Logic high is 1.8–3.6 V, so a 3.3 V or 1.8 V FPGA bank drives it directly.

Footprint: Mini-Circuits' 3×3 mm QFN (case DG1677, suggested layout PL-768), not stocked by KiCad. It gets drawn at layout from PL-768.

3. How the drawing was verified

Check	Result
`_work/check_sheet.py routing`: 43 nets exact, every pin of the 64 parts accounted for	**PASS**
KiCad ERC on the sheet	1 × `power_pin_not_driven` on `-3V3`, until POWER exists. The local VDD/VEE nodes behind the 11.5 Ω resistors carry PWR_FLAGs

4. How to review this sheet

About 20 minutes, with `M3SWA2-34DR+.pdf` from the AERIS-10 component folder.

1. **The switching plan and the SMA count** (§1). Those are your call.
2. **One switch block against Figure 2** (p.10). The other three are identical.
3. **U901's pads against the Pad Description** (p.10): RFC 15, RF1 3, RF2 10, VDD 8, VEE 5, VCTRL 6.

```
py _work/check_sheet.py routing
```

Source: docs/CONTROL_SPEC.md

CONTROL sheet: specification and review guide

25 September 2026, housekeeping devices added 2 October, Ethernet option 13 November · `sheets/CONTROL.kicad_sch` *(A1)* · *drawn by* `_work/sheets/control.py` *from the connection list in* `_work/sheets/control_spec.py`

The front-end FPGA, **U1101 XC7A50T-2FTG256I** (AERIS-10's own part), with everything it needs to boot and everything it talks to that is not on another sheet:

- the configuration flash, JTAG, the reset and DONE circuits;
- the Pmod cable from the KV260;
- the ribbon to AERIS-10's ADAR1000 beamformers;
- the LVDS terminations of every pair the FPGA receives, and the 22 Ω series resistors on every DAC line;
- the housekeeping devices on the HK bus: a temperature sensor and the board ID EEPROM.

The FPGA is drawn as its four KiCad units, and it reads by net name: every ball has a short stub and a name. A **hierarchical label** at a ball means the net leaves the sheet; a **plain label** means it stays on it. The circuits sit nearby as small wired blocks.

The Xilinx documents behind every value are now on disk, fetched through the Internet Archive by `_work/fetch_datasheets.py`: UG470 (configuration), UG471 (SelectIO), UG480 (XADC), UG483 (PCB design), DS181 (Artix-7 data sheet), DS593 (JTAG cable), UG908 (Vivado programming), UG475 (packages and pinout), Xilinx's ball list for the exact device (`xc7a50tftg256pkg.txt`) and the Micron MT25QL128 datasheet. For the housekeeping devices: TI's TMP1075, ST's M24C02 (DS9398) and Microchip's AT24CS02, the EEPROM considered first.

---

1. Bank voltages: the plan changed on reading the package

The first plan put 42 signals at 1.8 V on bank 34. **In the FTG256, bank 34 has only 20 I/O and no clock-capable pin** (the symbol's ball names show it). So:

Bank	VCCO	Carries	Why this bank
14	3.3 V	AD9484 on **AERIS-10's own balls**, CLK_FPGA on AERIS's `FPGA_ADC_CLOCK` balls, AD9253, the two link pairs the FPGA receives, flash	The flash pins live in bank 14. LVDS_25 **inputs** are allowed in a 3.3 V bank with `DIFF_TERM` off (UG471 Table 1-44 note 1, DS181 Table 11 note 1), so each pair gets an external 100 Ω, as AERIS does
15	3.3 V	AD9708 on **AERIS's own balls**, `DACR_CLK` on AERIS's `FPGA_DAC_CLOCK`, AD9767, Pmod, `SW_CTRL0-3`, `CLK_SEL`, XO I²C	The DACs, switches and XO are 3.3 V parts
34	2.5 V	Only the three link pairs the FPGA **drives**	LVDS_25 outputs need VCCO = 2.5 V (UG471). The other 14 balls stay unused
35	1.8 V	8 × ADAR1000 control + SPI (35 lines), converter SPI, `HK_SCL/SDA`, `FPGA_IRQ`, `HK_ALERT` (ball K2)	AERIS drives the ADAR1000s at 1.8 V; the ADCs' SPI is 1.8 V; the carrier's lines are **`1.8 V [V]`**: I2C, reset and the interrupt input all sit on `PL_1V8` on the carrier (XTP682, INTERFACE_SPEC §4.3)

The pin table is in `control_spec.py`. On import it **proves itself against the symbol's own ball names**:

- every ball is in the bank it is listed under;
- every `_P` net is on a `P` ball, with its `_N` on the same pair;
- the five clocks are on MRCC/SRCC balls: AD9484 DCO, AD9253 DCO, CLK_FPGA, the link receive clock and the Pmod SPI clock;
- all 256 balls are accounted for.

ADCR_DCO is wired inverted (12 November 2026). N14 carries ADCR_DCO_N and P14 ADCR_DCO_P (the `INVERTED` set in `control_spec.py`; the check above expects the swap). The AD9484 has DCO's P pin west of N, so a pair from the FPGA arrived with its legs crossed and had to go round the chip (51 mm against 39). **The gateware must invert the clock:** `IS_CLK_INVERTED` on the ISERDESE2 (or `IS_C_INVERTED` on an IDDR), or capture on the opposite edge.

Pin swap for routing (7 October 2026). Bank 35 as a whole, and the AD9767 (DACS) lines within bank 15, were re-assigned at layout: each net to the ball nearest its far end, by a minimum total-length matching, so no two lines of either bus cross. The AERIS-10 balls (DACR, ADCR, CLK_FPGA), every pair and every clock-capable ball kept their place. The new tables are an override block in `control_spec.py`, after the original ones, and the self-check above runs on them. Nothing in

bank 35 or among the DACS lines needs a particular ball, so the swap only changes the FPGA's constraint file.

2. Decisions this sheet makes, for your approval

Decision	Evidence	Alternative
The bank allocation of §1	FTG256 ball names; UG471 on LVDS in other-voltage banks	A larger package (CSG324) with more 1.8 V I/O
CLK_FPGA through a matched attenuator: 24.9 Ω series plus 24.9 Ω to +1V2 on each leg	The ADCLK948 swings 610–960 mV (its Table 1, V_O). LVDS_25 accepts at most 600 mV (DS181 Table 11). The pad halves that to 305–480 mV and still looks like 50 Ω to the line. +1V2 sets V_{ICM}, which must be 0.3–1.5 V	Plain 100 Ω, as for the ADCs, which would overdrive the input
FPGA_PROG_B through a 74LVC1G07 open-drain buffer powered at 1.8 V	A 2N7002 level shifter with its gate at 1.8 V is not guaranteed to turn on: $V_{GS(th)}$ is up to 2.5 V. The LVC1G07 has V_{IH} = 0.65 × V_{CC} at 1.8 V and its output tolerates 5.5 V (SN74LVC1G07 datasheet)	BSS138 shifter
Configuration exactly as UG470 Figure 2-14 (master SPI x4)	M[2:0] = 001 through 1 kΩ; INIT_B and PROGRAM_B 4.7 kΩ; FCS_B 2.4 kΩ; W and HOLD 4.7 kΩ; CFGBVS to VCCO_0; push button on PROGRAM_B (Table 2-4)	n/a
PUDC_B high through 1 kΩ (I/O pull-ups off while configuring)	Table 2-4: *"tied either directly, or via a ≤ 1 kΩ"*. **AERIS uses 4.7 kΩ, outside that limit.** High is AERIS's choice; AERIS's own pull resistors hold the ADAR lines meanwhile	PUDC_B low: pull-ups on, which would raise LOAD and TR during configuration
Flash MT25QL128ABA1ESE (128 Mb, SO8W)	In Vivado's configuration-memory list (UG908, `mt25ql128`). The Winbond W25Q128 that KiCad ships is not. AERIS uses a 1 Gb BGA; 128 Mb holds a 50T bitstream (about 17 Mb) several times over	AERIS's MT25QL01G
XADC on its on-chip reference: VP, VN, VREFP, VREFN to GNDADC; VCCADC and GNDADC through ferrites (UG480 Figure 1-2, right)	UG480 Table 1-1: *"This pin should always be connected to GNDADC if an external reference is not supplied."* **AERIS ties VREFP to +1V0: that is wrong**, confirmed now that UG480 is on disk	An external 1.25 V reference
VCCBATT to GND	DS181: *"If battery is not used, connect VCCBATT to either ground or VCCAUX"*; UG470 Figure 2-14 grounds it	n/a
DXP/DXN to GND	UG475 Table 1-12: *"When not used, tie to GND."* The XADC's own sensor reads the die temperature	An external thermal-diode monitor
JTAG on the Xilinx 2 × 7, 2 mm header	DS593 Figure 14: 2 VREF, 4 TMS, 6 TCK, 8 TDO, 10 TDI; 3–11 GND, 13 PGND; 1, 12, 14 unused. Direct to the FPGA, as UG470 Figure 2-14	Digilent 1 × 6
The AERIS ribbon: an IDC 2 × 20. Pins 1–32 carry CS, TX_LOAD, RX_LOAD and TR for each of the 8 ADAR1000s. Pins 33/35/37 carry the SPI (SCLK, SDIO, SDO), each next to a ground. 34, 36 and 38–40 are grounds	ARCHITECTURE §7.2, sized for 8 chips. **Only five grounds for 35 lines**: acceptable for static control lines and a few-MHz SPI, with `SLEW = SLOW` in the constraints	A 2 × 25 with a ground beside every signal
No pull resistors on the ADAR lines here	AERIS keeps them next to the chips (4.7 kΩ on LOAD, 22.1 kΩ on TR and SPI, 22.1 kΩ up on CS). **The AERIS end of this cable does not exist yet**: its Main Board has no such connector, because its own U42 drives these nets	Duplicate them here
Pmod pinout	Pmod pins 1–4 CS, MOSI, MISO, SCLK (INTERFACE_SPEC §4.2); 7 BEAM_STROBE, 8 PPS_SYNC, 9–10 spare (the debug UART since Rev08, section 9). GND 5/11. The KV260's 3.3 V (6/12) is left open: the adapter takes no power from the Pmod. On an odd/even header Pmod pin k is pad $2k$−1 and pin k+6 is pad $2k$	n/a
HK I²C pull-ups 10 kΩ to 1.8 V, fitted (4.7 kΩ until 2 October)	The carrier already has 2.21 kΩ to `PL_1V8` (XTP682 sheet 8). With both, the bus sees 1.81 kΩ: 1.0 mA at 1.8 V. That is what the EEPROM must sink, and the M24C02 is specified at 0.7 mA for 0.2 V at 1.8 V (DS9398 Table 14); scaling that up gives about 0.3 V, under the 0.54 V (0.3 × V_{DD}) a 1.8 V input reads as low. 4.7 kΩ would ask 1.2 mA. Kept so the bus idles high on the bench without a carrier: 10 kΩ alone is fast enough for 100 kHz	4.7 kΩ; or none, relying on the carrier
FPGA_IRQ on J8 pin 15, active high, 47 kΩ pull-down (R1133)	Pin 15 is the only single-ended pin that goes **into** the SOM, through the carrier's SN74AVC4T245 at 1.8 V. The pin first allocated, 32, is the carrier's 48 MHz camera clock (INTERFACE_SPEC §4.3). With PUDC_B high the FPGA's pin floats until configured; the pull-down holds the translator's input at "no interrupt"	Pin 32, which would fight the carrier's clock
The HK bus's addresses are free	The carrier's TCA9546A channel 1 reaches only J8: `IAS1_I2C_SCK/SDA` appear on XTP682 sheets 8 (the switch) and 13 (J8) and nowhere else. So 0x48 and 0x50 are this board's	n/a

Decision	Evidence	Alternative
Temperature sensor TMP1075DR (U1104), SOIC-8, I²C **0x48**	1.7–5.5 V, ±1 °C max from −40 to 110 °C, LM75-compatible registers (TMP1075 datasheet). A2..A0 to GND gives 0x48 (its Table 7-2). The FPGA's XADC already reads the die; this one reads the board	VSSOP-8 (DGK): its 0.65 mm pitch does not fit the Power class's 0.2 mm clearance, with V+ next to A0 (GND)
`HK_ALERT`: the sensor's ALERT to the FPGA, ball K2 (a free bank-35 ball; H3 until the pin swap below), 10 kΩ pull-up (R1134)	ALERT is open-drain (Table 5-1). The FPGA can fold it into `FPGA_IRQ`, the one line into the SOM	Leave ALERT unconnected and poll
Board ID EEPROM M24C02-FMN6TP (U1105), SOIC-8, I²C **0x50**	The -F grade runs from 1.7 V. Its output low is specified at **1.8 V: 0.2 V at 0.7 mA** (DS9398 Table 14). It holds the board's revision and serial number, written once	**AT24CS02**, which has a factory-programmed 128-bit serial number. Rejected: at 1.7 V its output low is specified for **0.15 mA** only (its Table 4-2), and this bus needs about 1 mA
Write protection: WC pulled up (R1135, 10 kΩ), solder jumper JP1101 to GND	WC high disables writes; floating, the M24C02 enables them (DS9398 §2.4). Closed, the jumper allows writing. JP1101 is copper only: not in the BOM or the placement file	WC to GND: writable from Linux at any time

3. Every value, and where it comes from

Part	Value	Source
R1101–R1114	100 Ω across each received pair	UG471: no DIFF_TERM in a 3.3 V bank. AERIS R2–R12 for the AD9484
RN1101–RN1107	4 × 22 Ω arrays, 27 lines, 1 spare	AERIS R23–R30 on the AD9708
R1115–R1118, C1101	24.9 Ω × 4, 100 nF at the bias	§2
R1119–R1128	see §2	UG470 Table 2-4, Figure 2-14; CCLK 22 Ω as AERIS (Figure 2-14 note 4: termination may be needed)
R1129	10 kΩ to +1V8_D	Holds FPGA_PROG_B high while the Kria is not driving it (the carrier also has 10 kΩ, R208)
R1131, R1132	10 kΩ to +1V8_D	HK I²C pull-ups, §2
U1104, C1182, R1134	TMP1075DR, 100 nF, 10 kΩ	§2. TMP1075 §8.3: 0.01 µF typical bypass, more for a noisy supply. R1134 is the ALERT pull-up
U1105, C1183, R1135, JP1101	M24C02-FMN6TP, 100 nF, 10 kΩ, solder jumper	§2
R1133	47 kΩ to GND	FPGA_IRQ pull-down, §2. Stiff enough for a CMOS input: even 10 µA of leakage would leave it under 0.5 V
Q1101, D1101, R1130	2N7002, green LED, 330 Ω	DONE lamp, about 4 mA
Decoupling C1110–C1171	FTG256/XC7A50T row of **UG483 Table 2-2**; types from Table 2-5	VCCINT 330 µF + 3 × 4.7 µF + 5 × 0.47 µF; VCCBRAM 100 µF + 0.47 µF; VCCAUX 47 µF + 2 × 4.7 µF + 3 × 0.47 µF; VCCO_0 47 µF; per other bank 2 × 4.7 µF + 4 × 0.47 µF, and one 47 µF per group of banks at one voltage
FB1101, FB1102, C1175, C1176	ferrites, 100 nF, 470 nF	UG480 Figure 1-2

4. Power sequencing: the open point from POWER, now answered

DS181 (*Power-On/Off Power Supply Sequencing*):

- The order VCCINT → VCCBRAM → VCCAUX → VCCO is **recommended**, *"to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on"*. It is not a requirement.
- The **one hard limit** is on 3.3 V banks: VCCO − VCCAUX must not exceed 2.625 V for longer than $T_{VCCO2VCCAUX}$, which is **300 ms per power cycle at T_J = 125 °C** (800 ms at 85 °C).
- Here VCCAUX (+1V8_D) is an LDO fed from +3V3_D. So that window only lasts while the LDO soft-starts (10 nF on NR/SS): milliseconds, not hundreds.
- The power-on currents of DS181 Table 6 (ICCINTQ + 120 mA, and so on) are far inside the 2 A the regulators give.

The POWER sheet's "no sequencing" is therefore acceptable. What is lost is the minimum inrush current and tri-stated I/Os during the ramp. PUDC_B high keeps the I/Os floating anyway.

5. How the drawing was verified

Check	Result
`control_spec.py` self-check: every ball against the symbol (bank, pair, clock capability, all 256 covered)	passes on import
The KiCad symbol against **Xilinx's own ball list** (`xc7a50tftg256pkg.txt`), all 256 balls by name	**identical**. Now part of the self-check, which fails if they ever differ (mutation-tested)
`_work/check_sheet.py control`: 184 nets exact, 47 no-connects alone, every pin of the 108 parts accounted for	**PASS**
KiCad ERC	7 warnings on this sheet, all `pin_to_pin`. KiCad's symbol types CFGBVS, VP, VN, VREFP, VREFN, DXP and DXN as bidirectional, and here they are tied to power nets on purpose (§2). Design total: 660 (was 672)
Pin tables	New project symbol MT25QL128ABA1ESE from the Micron datasheet Figure 6, cross-checked against KiCad's MT25QU (same family): agrees apart from pin 7's name (HOLD# vs RESET# variant) and the W-PDFN's exposed pad. SN74LVC1G07 pinout checked against TI's Pin Functions table (DBV)

The generator needed **multi-unit symbols**: `_work/schgen.py` now reads which unit each pin belongs to and places a unit by number. The sheets already drawn regenerate byte-identical.

For the housekeeping devices it learned two more things (2 October): **derived symbols** (KiCad's `extends`, as M24C02-FMN is of M24C01-FMN) are flattened the way KiCad embeds them, and a symbol the library keeps out of the BOM (the solder jumper) stays out of it. DRC checks that the footprint agrees.

6. How to review this sheet

About 50 minutes.

1. **§1's bank allocation**, and the pin table in `control_spec.py` against AERIS-10's U42 for the AD9484 and AD9708 balls (`py _work/aeris_reference_circuit.py U42`).
2. **§2's decisions**: the CLK_FPGA pad, the ADAR ribbon pinout and the missing AERIS end above all. Then the housekeeping block: the EEPROM chosen for its 1.8 V drive, and the HK pull-ups now 10 kΩ.
3. **The configuration block against UG470 Figure 2-14**, value by value.

```
py _work/sheets/control_spec.py     # the pin table's self-check
py _work/check_sheet.py control
```

7. Gigabit Ethernet, an assembly option (13 November 2026)

> **Rev05.** On Rev06 Ethernet has its own FPGA pins and IAS1 keeps all its lanes: section 8.

Added by `_work/add_ethernet.py`, a text edit of this sheet like the ESD arrays (`_work/add_esd.py`). `control_spec.py` and `check_sheet.py` do not know these parts: no FPGA ball changed.

Why. IAS1 is the board's only link to the Kria, and it is not proven until the first boards are up (IAS_LINK_SPEC §6). An Ethernet port lets a laptop, or the KV260's own port, reach the FPGA without it, fast enough to validate the radar or the SDR, one at a time. 100 Mb/s is not enough for either, so it is gigabit.

Why it shares the IAS1 pairs. RGMII needs 14 FPGA balls and SGMII two LVDS pairs. The FPGA has 39 free balls, but none of them can still be routed out on the signal layers. Every route that reached the edge balls (T2, P1, R1) did it through a GND plane, and bank 14's T12 and R12 are boxed in by the ADCR_D3 pair and the bank's +3V3_D feed. So the PHY's SGMII **shares two of the link's pairs, chosen by fitting parts**:

Mode	Fitted	Removed	What runs
IAS1 (as built)	C101, C102, C107, C108	n/a	the link as before; C1218–C1221 are DNP
Ethernet	C1218–C1221 (100 nF 0402)	C101, C102, C107, C108	LINK_RX_D0 → PHY input, PHY output → LINK_TX_D0

LINK_RX_D0 is an FPGA `LVDS_25` output: C1220/C1221 take it to HSIP/HSIN, which the PHY terminates and biases. The PHY's HSOP/HSON reach LINK_TX_D0 through C1218/C1219. That pair is an FPGA input, already terminated (R105) and biased to +1V2 (R101/R102). The other link pairs are not used in Ethernet mode: the gateware should hold LINK_RX_D1 static, since it runs beside the PHY's input pair for 5 mm (below).

Part	What	Source
U1201 RTL8211FSI-CG	Copper (10/100/1000Base-T) ↔ SGMII PHY, −40 to 85 °C, QFN-48 6 × 6 mm. LCSC C2904132	RTL8211FS(I)(-VS) datasheet Rev. 1.8
J1201 HR911130C	RJ45 with gigabit magnetics and two LEDs, on a tab off the board's east edge (LAYOUT §1). **0–70 °C**: no industrial gigabit magjack had stock; the KV260 itself is a 0–70 °C kit. LCSC C50933	HanRun drawing; footprint by `_work/make_rj45.py`
Y1201	25 MHz crystal, 20 pF, ±20 ppm (X322525MOB4SI), with 2 × 27 pF	datasheet: ±50 ppm
L1201	2.2 µH power inductor (Murata DFE201210U-2R2M, 1.2 A) for the PHY's 1.0 V switching regulator; its output feeds only DVDD10/AVDD10	datasheet §6.8
R1201	RSET 2.49 kΩ 1 %	Realtek's reference schematics

Straps (4.7 kΩ). `CFG_MODE` = 011 selects UTP ↔ SGMII: RXD1 and RXD2 high, RXD3 low. The PHY address is 1: LED0 is pulled high. RXC and RXCTL need no resistor for their 0, because both have an internal pull-down at power-on (datasheet table 6); nothing else drives them in SGMII mode. RXDLY is 0. `CFG_LDO` = 01, so the PHY's own LDO makes 2.5 V for its I/O pads, and DVDD_RG is that LDO's output (decoupled, not fed).

The LEDs follow their straps. LED1 (strap 1) is active low and lights the green LED from +3V3_D. LED2 (strap 0) is active high and lights the yellow one.

Management: none from the FPGA. MDC/MDIO could not be routed to any free ball either (above). The PHY does not need them: its straps set it up, and it auto-negotiates both its copper side and its SGMII side, which is what the SGMII core expects. MDC (pulled down by R1211) and MDIO (pulled up by R1213, 1.5 kΩ to DVDD_RG) end on test pads **TP14** and **TP15** beside the PHY. Use them to read its registers with a probe, or to wire them to a spare I/O for bring-up.

Reset and power. PHYRSTB has a 10 kΩ / 4.7 µF power-on reset. VDD_REG, DVDD33 and AVDD33 (the last behind a ferrite) take +3V3_D. The datasheet asks for a 3.3 V supply that can give 1 A with a rise time over 0.5 ms. U1002 is a 2 A part carrying 1.16 A, and the PHY adds about 0.15 A.

What the shared pairs cost the IAS1 link, measured. All figures are from a lumped-line simulation like `lvds_eye.py`'s (SIGNAL_INTEGRITY §9.7) at 1.25 Gb/s, on the legs as routed. The eye is the vertical opening; jitter is the spread of the zero crossings.

Pair	Before	With the DNP branch	Branch
LINK_TX_D0	518 mV, 21 ps	477–484 mV, 18–23 ps	P: C1218 on the top face just below the notch, at (178.9, 98.3), with a via in each pad; the branch is 0.9 mm of L3 and the via to L1, about 14 mm from the connector. N: 1.0 mm from R102's bias branch, about 10 mm from it
LINK_RX_D0	609 mV, 93 ps	601–607 mV, 109 ps	4.3 mm (P) and 5.2 mm (N, 2 vias) to C1220/C1221, near the connector

C1218 went through three places. Beside R101 on the top face it left a 6.6 mm branch (461 mV). On the bottom face, on R101's own via, it cost least (489–499 mV), but there it sits over the carrier, 0.8 mm above it, where nothing may be fitted (LAYOUT §1). Where it is now, the only free top-face spot near the leg, it costs 10–15 mV more than on the bottom and stays off the underside. The RX_D0 branches could not be shortened: the space around C101/C102 and J101 is full.

Ethernet mode, measured the same way. The path runs from the FPGA to the PHY's input, and from the PHY's output to the FPGA, branch and PHY run included:

Path	Eye	Jitter	PHY-side pair
LINK_RX_D0 → PHY	350 mV	50 ps	ETH_SGTX_PHY: 53.3 / 52.2 mm, 53 % coupled, P−N +6.5 ps; alone 640 mV
PHY → LINK_TX_D0	637 mV	53 ps	ETH_SGRX_PHY: P on L8 with a 3.2 mm bump, N on L6: P−N +20.9 ps on the PHY side, which cancels the −21.7 ps of C1218's tap sitting 3.2 mm further down LINK_TX_D0_P than C1219's on N; alone 637 mV

The PHY's SGRX legs are matched in **delay**, not length, and end to end, PHY to FPGA. L8 microstrip is faster than L6 stripline: a meander that matched their lengths left 41 ps of skew. The PHY's input pair runs beside LINK_RX_D1_N on L1 for 5.2 mm at 0.17 mm.

Gateware. Xilinx's 1G/2.5G Ethernet PCS/PMA or SGMII core (PG047), in its "SGMII over LVDS, asynchronous

oversampling" form (XAPP523), which supports 7-series −2 parts. 1.25 Gb/s is also the ceiling of these HR-bank pins (IAS_LINK_SPEC §7), so there is no margin in rate.

8. Rev06: Ethernet on its own pins, IAS1 complete (14 November 2026)

`_work/rev06_eth.py` *and* `_work/rev06_vcm.py` *(text edits of this sheet), branch* `rev06`*.*

Why. In Rev05 the PHY borrowed two IAS1 pairs, so Ethernet and the full link excluded each other. The owner wanted both: IAS1 with its two uplink lanes and its downlink, and Ethernet on top, so that either path works alone and both together carry about 3 Gb/s (fpga/eth/REDUNDANCY.md, mode 6). C1218–C1221 become in-line AC capacitors on the PHY's own pairs; C101/C102/C107/C108 stay fitted.

Pins, chosen by what the board can escape. Section 7 found no free ball that could still be routed out. Re-checking every free bank-14/15/34 ball for a via in its pad: R2/R1 were clear; R3 was blocked only by a skew meander of LINK_RX_D0_N under the corner, which moved out of the BGA (that leg was re-matched: the pair is back to 0 ps P−N); T4/T3 and N1 are walled in by matched LVDS legs; P5 sits on a +3V3_D run that feeds ball L6 where the L4 plane has a void.

Signal	Ball	Standard	Notes
ETH_SGTX_FPGA_P/N	R2 / R1 (IO_L7P/N_T1_34)	LVDS_25	→ C1220/C1221 (bottom, by the PHY) → HSIP/HSIN
ETH_SGRX_FPGA_P/N	R3 / T2 (IO_L8P/N_T1_34)	LVDS_25, DIFF_TERM	← R1215/R1216 ← C1218/C1219 ← HSOP/HSON
ETH_MDC	P1 (IO_L4N_T0_34)	LVCMOS25	the PHY's I/O run at 2.5 V (CFG_LDO = 01); R1211 holds it low during configuration
ETH_MDIO	M15 (IO_L3N_T0_DQS_EMCCLK_14)	LVCMOS33, **open-drain**	the gateware only pulls it low; R1213 (1.5 k) pulls it up to the PHY's 2.5 V, which bank 14 reads as high (V_IH 2.0 V). The bitstream must not use EMCCLK
ETH_RSTN	K13 (IO_L5P_T0_D06_14)	LVCMOS33	R1214/C1216 power-on reset stays; the FPGA can hold the PHY in reset
INTB	n/a	n/a	open, as before: the gateware polls MDIO

Vivado place-and-route of the full Artix top with these pins closes timing (WNS +0.039 ns).

Receiver bias, made at the PHY. The FPGA's DIFF_TERM terminates but does not bias an AC-coupled input. R1215/R1216 (10 k) give each SGRX leg a common mode. They first went to +1V2, which exists only near J101 and on a few vias 30 mm from the PHY: placed by those vias they hung off the legs as 23 / 11 mm branches (157 / 75 ps stubs), which resonate near 1.6 GHz. Now they sit **on** the legs, in series with the trace between each capacitor and the line, and their common node ETH_VCM is made locally: R1212 10 k from +3V3_D, R1217 5.6 k to ground, C1222 100 nF → **1.18 V** (LVDS_25 input common mode 0.3–1.5 V).

Routing (lvds_skew.py, end to end across the capacitors).

Pair	P / N delay	P − N	Stubs	Notes
ETH_SGTX (FPGA → PHY)	404 / 402 ps	+2 ps	9 / 9 ps	51 / 49 mm, two 50 Ω legs, vias in the balls
ETH_SGRX (PHY → FPGA)	464 / 468 ps	−4 ps	7 / 6 ps	a 3.9 mm meander on P
LINK_RX_D0	773 / 773 ps	+0 ps	3 / 3 ps	as Rev05

The legs are uncoupled, like ten of the board's LVDS pairs, because the BGA's south-east corner leaves no room for a coupled pair to leave it. To make room, the slow nets in the corner (JTAG, flash, XADC, converter SPI, housekeeping I²C, ADAR SPI) and part of bank 34's VCCO feed were ripped and re-routed. **Known compromise:** two of bank 34's VCCO balls (R4, M3) are now fed through a 0.1 mm × 13.7 mm +2V5 track (about 0.15 Ω); the bank's other VCCO balls keep their wide connection. DRC: 0 errors, 0 unconnected, schematic parity 0.

Eyes at 1.25 Gb/s (lvds_eye.py's model, both legs end to end across the AC capacitors, PRBS7, LVDS driver 3.5 mA / 300 ps, 100 Ω and 2 pF at the receiver; the capacitors and the 10 k bias are not modelled):

Path	Routed	Ideal 50 Ω legs	Jitter	Rev05 (shared pairs)
FPGA → PHY (SGTX)	**616 mV**	616 mV	52 ps	350 mV
PHY → FPGA (SGRX)	**521 mV**	564 mV	58 ps	637 mV

Both are far above the 200 mV a receiver needs. The legs were widened to each layer's 50 Ω width (0.183 mm outside,

0.151 mm inside) wherever the clearances allow; a few short sections where they leave the balls and the capacitors stay at 0.1–0.117 mm (57–64 Ω).

Supplies after the rework (current through each track every path to the loads must cross): the bank-34 VCCO feed's drop to the FPGA went from 11 mV (Rev05) to 19 mV after widening the reworked corner, inside +2V5's ±5 % (125 mV). Two older necks were found on the way and checked: +1V8_A to the ADC drivers' ferrites had a 0.49 mm piece of 0.1 mm on L3 carrying 0.5 A (IPC long-track chart: +242 °C, a short neck runs far cooler but it was still the worst spot on the board): replaced by a 1.0 mm L-shaped jog, the rail's drop is now 64 mV. The +3V3_D feed to FB401 (the clock section, 0.48 A) has four 0.1 mm necks, 0.2–0.5 mm long, between the PHY's pads, inherited from Rev05: 10 mV of drop; left as they are (no room, and short necks spread their heat into the planes).

Analogue neighbours (analogue and clock nets within 0.3 mm for more than 2 mm, against Rev05): two new pairings. ETH_MDIO beside CLK_FPGA_P on L3 for 2.3 mm at 0.17 mm (MDIO is a 2.5 MHz line: harmless). ETH_SGTX_FPGA_N beside CLK_ADCS_P on L6 for 2.2 mm at 0.17 mm: by SIGNAL_INTEGRITY §3.5's stripline figures (14.5 % 2D NEXT saturated at 25 mm, about 3.5 × less in 3D) that is about 0.4 % of a 175 mV leg, 0.3 mV on the clock pair, under 0.3 ps at its edge: negligible next to the AD9253's aperture jitter. Moving the leg would need the gap between a Y401 via and ETH_MDC, which is too narrow.

Also on Rev06: J1002, a 5 V fan header for enclosure v2 (POWER sheet; docs/ENCLOSURE.md section 6).

9. Rev08: what changed around this sheet (16–17 November 2026)

The CONTROL sheet itself kept its parts; Rev08 added two sheets that hang off it (**REV08_PLAN**):

What	Where	Effect on CONTROL
Debug UART (G-1)	`PMOD_SPARE1` (Kria to FPGA, `G15`) and `PMOD_SPARE2` (FPGA to Kria, `G11`), the Pmod's two spare lines, renamed in phase 4	The two lines' old soft functions moved to register bits. The STATUS sheet's CH340X drives `PMOD_SPARE1` through 1 kΩ, so the Kria wins when the Pmod cable is fitted; `PMOD_SPARE2` also lights the heartbeat LED
Two TCA6416A expanders on the Si549's I²C (`XO_SCL`, `XO_SDA`, G-2)	`U1313` at 0x20 (`RX_VU`: switches, bias tee, converter control), `U1501` at 0x21 (`STATUS`: the nine status LEDs)	`hk_xo_ctrl` became a shared I²C master; no traffic while receiving except on request
The VHF/UHF front end's IF	`IF_VU` into `SW2`'s second throw (**ROUTING_SPEC** §1.2)	`SW_CTRL1` now selects between AERIS's IF and the front end

Every connector, LED and chip of the board, with its use: **BOARD_MANUAL**.

Source: docs/POWER_SPEC.md

POWER sheet: specification and review guide

25 September 2026 · `sheets/POWER.kicad_sch` *(A2)* · *drawn by* `_work/sheets/power.py` *from the connection list in* `_work/sheets/power_spec.py`

The whole power tree on one sheet. Every regulator circuit is its datasheet's typical application, with the values read from the datasheet's own table. The loads and the regulator sizing are in **POWER_AND_STACKUP.md** §1, recomputed by `_work/power_budget.py` for the tree as drawn.

```
J1001 (12 V, 5 A) -> L1004 (6 A CMC, both lines) -> VIN_J
  |-- F1001 PTC -> SMCJ33CA -> Q1001/Q1003 (LM74502-Q1 U1009, OVP 18.3 V) -> SMBJ18CA -> +12V  (adapter, 1.12 A worst)
  +-- Q1010 (DMT10H015LFG) -> U1010 (TPS26631, OVP 14.4 V, ILIM 3.0 A) -> SS34 -> +12V_KV -> J1004 (§1.4)
+12V   – U1001 LMR33630  buck –▸ +5V0    2410 mA   (3 A part)
+5V0   – U1002 TPS563201 buck –▸ +3V3_D  1891 mA   (3 A part; a 2 A TPS562201 until the Rev08 audit)
       – U1003 TPS562201 buck –▸ +2V5     601 mA   FPGA LVDS banks, and feeds +1V8_A
       – U1004 TPS562201 buck –▸ +1V0     735 mA   FPGA VCCINT, at 1.017 V (R1031 3.24 k)
       – U1007 TPS7A8300 LDO  –▸ +3V3_A   100 mA   DACs' AVDD
+2V5   – U1005 TPS7A8300 LDO  –▸ +1V8_A   500 mA   ADCs' AVDD, at 1.85 V
       – divider              –▸ +1V2       1 mA   link termination bias
+3V3_D – U1006 TPS7A8300 LDO  –▸ +1V8_D   629 mA   FPGA VCCAUX, ADCs' DRVDD, at 1.85 V (50 mV pin grounded)
       – U1008 LM2663         –▸ –3V3       8 mA   RF switches' VEE
       – U1315 LP5907-2.8 LDO –▸ +2V8_RF  180 mA   Rev08 VHF/UHF front end (RX_VU sheet)
```

Input at `+12V` (adapter only, 70 °C, maximum process, bias tee at its limit, CAN dominant, fan on): 1.12 A at 12 V, 13.4 W; typical 0.97 A, 11.7 W. The FPGA rails come from Vivado's power report, which the budget lacked until the Rev08 audit of 18 November; four loads were also added then (Ethernet PHY, CAN transceiver, fan and bias tee, **AUDIT_Rev08.md** §2.1). With the single power entry feeding the KV260 through `J1004` (§1.4; KV260 0.92 A idle, 3.0 A brick rating, `U1010` 2.98 A nominal / 2.77 to 3.19 A at ±7 % with `R1043` 6.04 kΩ), **`J1001` and `L1004` carry 1.89 A typical, 4.12 A at the KV260 rating, and 4.31 A worst case** within `J1001`'s 5 A rating.

1. Parts, and where each circuit comes from

Block	Part	Circuit from	Datasheet
+5V0	**LMR33630ADDA**, 400 kHz	Figure 9-1, Table 9-2, row *400 kHz, 5 V*: L 8 µH, COUT 4 × 22 µF, RFBT 100 k, RFBB 24.9 k, CIN 10 µF + CHF 220 nF, CBOOT 100 nF, CVCC 1 µF. EN tied to VIN (*"Can be connected directly to VIN"*), PG left open (*"Can be left open when not used"*)	SNVSAN3F, from ti.com (`_work/fetch_datasheets.py`)
+3V3_D	**TPS563201**, 580 kHz (3 A; was TPS562201 until the Rev08 audit, P5)	Figure 7-1 and Table 7-2: same pin-out and 0.768 V reference; R2 10 k, R1 33.2 k, L 3.3 µH (SRP7028A), COUT 2 × 22 µF, CIN > 10 µF + 0.1 µF	SLVSCI8 / SLVSD91D
+2V5, +1V0	**TPS562201**, 580 kHz (2 A)	Figure 7-1 and Table 7-2: R2 10 k; R1 22.6 k (`+2V5`) / **3.24 k** (`+1V0` at `1.017 V`; was `3.09 k` before the Rev08 audit, P7); L 3.3 / 2.2 µH; COUT 2 × 22 µF; CIN > 10 µF + 0.1 µF; VBST 0.1 µF; EN pulled up by 10 k (Figure 7-1's R3)	SLVSD91D, AERIS-10 folder
+1V8_A, +1V8_D, +3V3_A	**TPS7A8300RGR**	Figure 51, ANY-OUT: SNS to OUT, 10 nF feed-forward OUT→FB, 10 nF on NR/SS, EN to IN, BIAS open (*"VIN ≥ 1.4 V ... BIAS pin can be left floating"*). CIN 10 µF, COUT 22 µF (Pin Functions). Voltage set by grounding pins (Table 2): `+1V8_A` = 1.85 V (50 mV + 200 mV + 800 mV pins, 12 Nov: copper/ferrite drop); **`+1V8_D` = 1.85 V** (50 mV pin grounded too since the Rev08 audit, P4: keeps VCCAUX at 1.714–1.873 V at the balls); `+3V3_A` = 100 mV + 800 mV + 1.6 V pins	SBVS197F, AERIS-10 folder
−3V3	**LM2663M**	Pin Functions: SD to GND for normal operation, LV to GND below 3.5 V in, OSC open. 47 µF flying and output capacitors, as its Electrical Characteristics are measured with	SNVS002E, AERIS-10 folder
+1V2	Divider, 1.10 k / 1.02 k, 1 µF	2.5 V × 1.02 / 2.12 = 1.203 V	none

The four regulator symbols are new, each transcribed from its datasheet's pin table. KiCad has an LMR33630 symbol, but it inherits from another one (`extends`), which the generator doesn't support.

1.1 Input protection for a vehicle supply (Rev05, 13 Nov)

The RF review of 13 November (finding B1) was right: the old chain was jack, PTC, a −30 V P-MOSFET and only then the TVS. ISO 7637-2 pulse 1 (−150 V from 10 Ω, LM74502-Q1 datasheet §10.2.3) puts its whole amplitude across that MOSFET before anything clamps. The input is now TI's 12 V battery design (LM74502-Q1 datasheet SNOSDE0A, Figure 10-1), oversized where the board allows it:

Part	Value	Why
F1001	PTC **2.0 A hold**, 24 V, mSMD200-24V (1.5 A until the Rev08 audit, P3: that one tripped above 60 °C at the audited load)	Ahead of everything. It holds 1.32 A at 70 °C, against 1.12 A worst case at 12 V and 1.28 A at 10.5 V (**AUDIT_Rev08.md** §2.3). Only a sustained input above the TVS breakdown (36.7 V) can trip it: an abnormal fault, see the limits below
D1003	**SMCJ33CA**, bidirectional, 1500 W, at VIN_F	Breakdown ≥ 36.7 V: above the 24 V jump start and the 35 V suppressed load dump (ISO 16750-2 test B), as §10.2.3 requires; ≥ 16 V reverse battery. Clamps pulse 1 to about 47–53 V at 15 A. TI's design uses the 600 W SMBJ33CA; the SMC part doubles its energy rating
Q1001, Q1003	**DMT10H015LFG**, 100 V, 13.5 mΩ at 10 V, PowerDI3333-8	Back to back, common source. With the TVS clamping pulse 1 at −53 V and the output held at +12 V by its capacitors, the blocking FET sees about 65 V: TI's 60 V example would have no margin. VGS(max) ±20 V > the 13.9 V gate drive (§10.2.2.2). Q1001 keeps its footprint
U1009	**LM74502-Q1** (SOT-23-8)	3.2–65 V, −65 V reverse (Features), charge pump 12.4 V, 60 µA gate source, 2 A sink
R1004, R1005	100 k / 7.32 k (0603)	Overvoltage cut-off. V_{OVR} = 1.165 / 1.25 / 1.333 V (§7.5) gives **17.1 / 18.3 / 19.5 V**. That is above the 14.8 V a charging alternator gives and below D1001's 20.0 V minimum breakdown, so D1001 never conducts steadily. 171 µA in the divider against 110 nA OV leakage
C1090	100 nF 100 V at VS	Pin Functions: "Connect a 100-nF capacitor across VS and GND"
C1091	220 nF 25 V, VCAP to VS	§10.2.2.4: ≥ 10 × C_{ISS} of the two FETs; TI's value
D1001	**SMBJ18CA** on +12V (was SMBJ15CA)	Catches the microseconds before the OV comparator opens the FETs, at ≤ 29 V: inside the 36 V of the LMR33630 and a brief overshoot for the 25 V input capacitors. Its 20 V minimum breakdown keeps it off below the cut-off

EN/UVLO is tied to VS (always on). The +12V rail now sees at most about 19.5 V steady state; anything above opens both FETs and the board resets, which is the intended response to a load dump or a 24 V jump start.

Layout. Q1001 stays where it was on the top side. U1009, Q1003, D1003, C1090 and C1091 are on the bottom under the jack, outside the KV260's outline (y > 117.25 mm), where the bottom was empty; R1004 and R1005 take D1002's and R1001's place on the top. DRC with zones refilled and schematic parity: 0 errors, 0 unconnected, 0 parity issues (one warning: D1003's flipped footprint differs from the library copy in its silkscreen only).

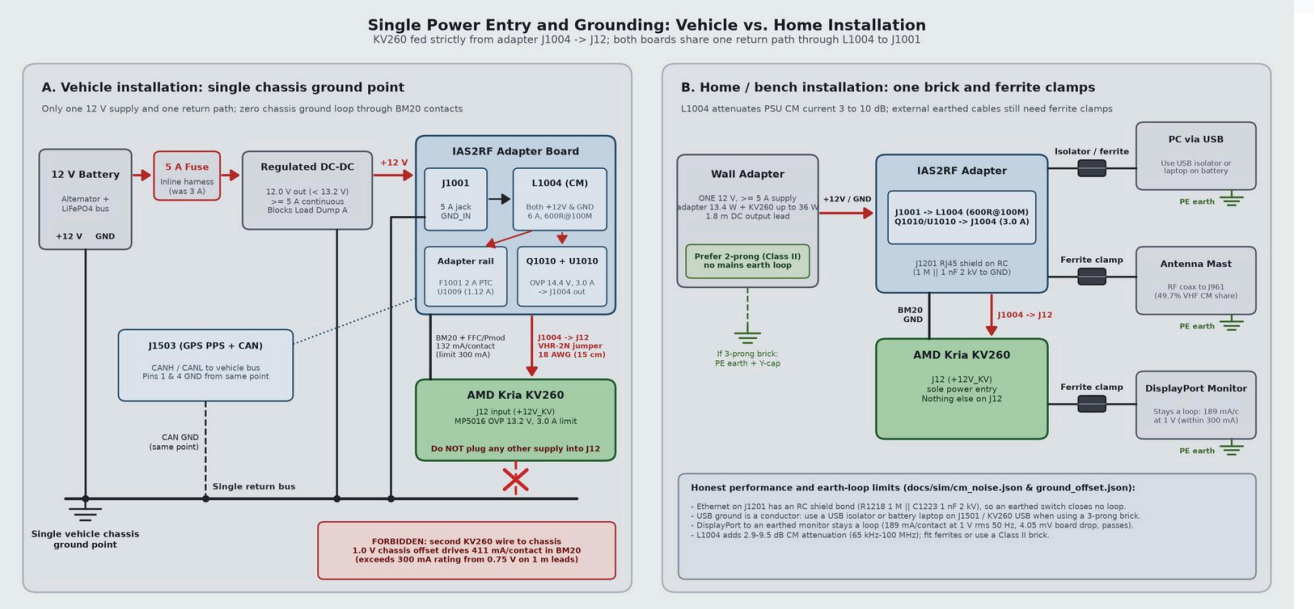
Limits, said plainly.

- A sustained input above 36.7 V (an unsuppressed load dump, or a 24 V system's alternator fault) makes D1003 conduct; the PTC then trips with more than its 24 V rating across it. An 1812 PTC rated 60 V at 2.0 A does not exist (the 1812 `mSMD200-24V` is 24 V). Fit the vehicle harness with a **5 A** inline fuse (updated from 3 A for the single power entry in §1.4) in any case.
- The new parts are not in **JLCPCB_QUOTE.md** yet; LCSC stock of the DMT10H015LFG was not confirmed (alternative: any 80–100 V N-FET, ≤ 20 mΩ at 10 V, VGS ±20 V, in PowerDI3333-8).
- The enclosure's tray honeycomb must be pocketed under the new bottom parts (D1003 is 2.3 mm tall) before printing: see **ENCLOSURE.md**.

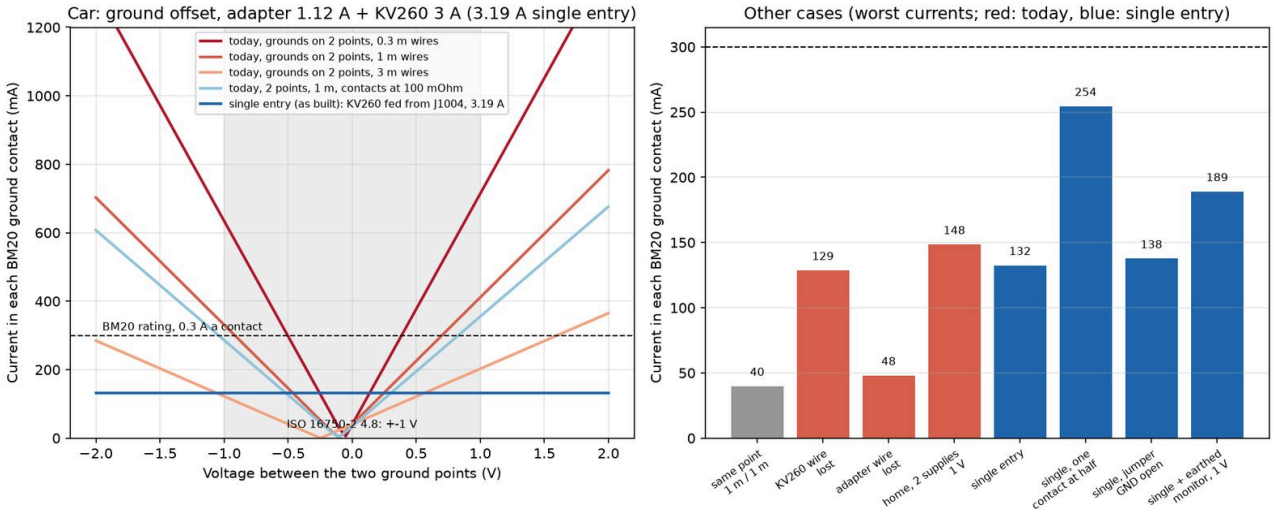
1.2 Fan header for enclosure v2 (Rev06, 14 Nov)

`_work/rev06_fan.py`. **J1002** (JST PH 2-pin, vertical, LCSC C131337): pin 1 FAN_5V, pin 2 GND, for a 50 × 50 × 10 mm 5 V fan (docs/ENCLOSURE.md section 6). **F1002**, a 0.5 A-hold 1206 PTC (SMD1206P050TF, C43379), keeps a shorted fan lead from pulling +5V0, and the whole board, down; **C1092** 10 µF holds the motor's commutation current at the header. Always on: the FPGA has no escapable ball left for PWM or tach, and HK_ALERT (TMP1075) would leave the fan off at power-up, the wrong failure. Placed near the input section, through-hole, outside the carrier's footprint (LAYOUT §1). The fan's ~0.1 A adds about 2 % to +5V0's load (LMR33630, 3 A).

1.4 Single power entry and the KV260 output (Rev08, 19 Nov)



Power and grounding wiring



Ground offset and earth loops

Why (`_work/power/ground_offset.py`, `docs/sim/ground_offset.json`). With the KV260 and the adapter on separate vehicle grounds, their boards are bridged by the 22 ground contacts of the two BM20 connectors (`J101`/`J102`), the FFC and the Pmod cable: 1.29 mΩ typical total (3.79 mΩ with contacts at 100 mΩ maximum), with the BM20 contacts carrying 94.3 % of any link current (83.3 % at max contact resistance) against a 0.30 A per-contact rating. At the ISO 16750-2 section 4.8 ground offset of 1.0 V, the inter-board loop drives 411 mA per BM20 contact on 1 m leads (exceeding 0.30 A from 0.75 V), 355 mA at max contact resistance (from 0.85 V), 714 mA on 0.3 m leads (from 0.40 V) and 203 mA on 3 m leads (from 1.60 V). Even grounded to the same point, unequal wire lengths (0.3 m / 2.0 m) drive 84 mA per contact (40 mA on 1 m / 1 m), and losing the KV260 ground wire puts 129 mA per contact (3.00 A on the link) across the BM20s. The KV260's own input eFuse (`MP5016`, XTP682 p. 3) also cuts off above 13.2 V, below the adapter's 18.3 V OVP.

With single-entry power, **the KV260's own DC return runs through the BM20 ground contacts by design**: the BM20 link is 1.3 mΩ (1.29 mΩ) against the 150 mm 18 AWG jumper's 33 mΩ (33.1 mΩ), so 96 % of the KV260's return crosses the BM20 link. That is why `U1010` limits the KV260 to its brick's 3 A rating (2.98 A nominal, 2.77 to 3.19 A at ±7 % with `R1043` 6.04 kΩ; at 3.6 A, one contact at half resistance carried 305 mA, over the 300 mA rating):

Case (`docs/sim/ground_offset.json`)	Inter-board link	Per BM20 contact	Against 0.30 A rating
Separate grounds, same point (1.0 m / 1.0 m)	-0.93 A	40 mA	Pass
Separate grounds, same point (0.3 m / 2.0 m)	-1.96 A	84 mA	Pass
Separate grounds, 1.0 V offset (1 m typ / max R)	10.2 / 9.9 A	411 mA / 355 mA	**Fail** (from 0.75 V / 0.85 V)

Case (`docs/sim/ground_offset.json`)	Inter-board link	Per BM20 contact	Against 0.30 A rating
Separate grounds, 1.0 V offset (0.3 m / 3.0 m typ)	17.7 / 5.0 A	714 mA / 203 mA	**Fail** on 0.3 m (from 0.40 V) / Pass on 3 m (1.60 V)
Separate grounds, KV260 ground wire lost	3.00 A	129 mA	Pass (surviving jack 4.12 A)
Single entry, typical KV260 load (0.92 A)	-0.89 A	38 mA	Pass
Single entry, at `U1010` limit (3.19 A)	-3.09 A	132 mA	Pass
Single entry, contacts at 100 mΩ maximum	-2.88 A	109 mA	Pass
Single entry, one contact at half resistance (3.19 A / 0.92 A)	-3.09 A / -0.89 A	254 mA / 73 mA	Pass
Single entry, one contact at a third of the others' resistance (2 A)		219 mA	Pass
Single entry, one contact at a third (3.19 A; the other 21 typical / at 100 mΩ max)	-3.09 A	352 mA / 306 mA	Over 0.30 A, pass on heat: 1.86 mW / 3.13 mW in that contact
Single entry, jumper ground contact open (typ / max R)	-3.21 A	138 mA / 122 mA	Pass
Home, single entry, earthed monitor 50 Hz (1.0 V / 0.1 V)	3.27 A / 0.33 A loop	189 mA / 133 mA	Pass (4.05 mV / 405 uV adapter drop)

The 0.30 A rating is a heating limit: Hirose derives its ratings from the temperature rise under current, and the BM20's operating range includes that rise. One contact carries more than its share only because its resistance is low, so its heat (I^2R) is the figure to check: 3.13 mW at worst, against 9.0 mW for a contact at its 100 mΩ maximum at 0.30 A (2.7 mW for a typical one), and 25 mW in all 22 against 59 mW (**AUDIT_Rev08.md** §6.3, `single_entry.heat` in the JSON).

Topology (`KVPWR` sheet). `J1001` passes both +12 V and return through `L1004` (`VIN_JACK` to `VIN_J`, `GND_IN` to `GND`; `F1001` keeps carrying only the adapter). From `VIN_J`, the KV260 branch runs through reverse-blocking N-FET `Q1010` (source on `VIN_J`) and `U1010` (`TPS26631PWPR` eFuse, 4.5 to 60 V, -60 to +67 V abs max on `IN_SYS`, 75 V for 10 ms, 31 mΩ typical integrated FET) to `+12V_KV` and right-angle header `J1004`. Reference: TI TPS2663x datasheet SLVSE94G (revised June 2024).

Part / Setting	Value and formula	Margin and datasheet reference
`L1004`	`ZEGMCM9070-501T` (C53154905, Coilmaster SMM9070-501 equiv.): 600 Ω at 100 MHz (450 Ω min), 6 A, 2 x 8 mΩ max (16 mΩ total), 80 V	Carries 1.89 A typ / 4.12 A rated / 4.31 A worst vs 6 A (0.057 W / 0.272 W / 0.297 W both windings). Pads 1-2 `GND`, 3-4 `+12V`, dotted ends on jack side
`Q1010`, `Q1011`	`DMT10H015LFG` (100 V, 13.5 mΩ, source on `VIN_J`) + `2N7002` (>= 15 V VDS, Ciss <= 50 pF, VGS 20 V)	Reverse polarity to -60 V (SLVSE94G §8.3.5, §9.2.2.6). `Q1010` sees 57.3 V peak VDS in pulse 1 (0.011 W at 0.92 A, 0.122 W at 3.00 A, 0.137 W at 3.19 A)
`U1010`	`TPS26631PWPR` (C2866319): `MODE` = `GND` (auto-retry), `SHDN` open (2.7 V internal enable), `PGTH` = `GND`, `IMON`/`FLT` open	Active current limit with 2x IOL pulse support (SLVSE94G §8.3.7.1.2). 0.026 W at 0.92 A, 0.279 W at 3.00 A, 0.315 W at 3.19 A
`R1040`, `R1041`, `R1042`	316 kΩ / 24.9 kΩ / 30.9 kΩ (Rsum = 371.8 kΩ): OVP 14.44 V rising / 13.50 V falling (±2 %), UVLO 8.00 V rising / 7.48 V falling	SLVSE94G §8.3.3 requires R1 >= 300 kΩ (316 kΩ) between `IN_SYS` and `UVLO` with reverse polarity. Equations 9-10 (§9.2.2.2) keep `+12V_KV` under KV260's 16 V `SMAJ16A`
`R1043`	6.04 kΩ (0603, 1 %): IOL = 18 kΩ·A / 6.04 kΩ = 2.98 A (2.77 to 3.19 A at ±7 %)	SLVSE94G §8.3.7.1 Equation 5. Caps KV260 at its 3.0 A brick rating while 1.12 + 3.19 = 4.31 A stays within `J1001`'s 5 A rating
`C1093`	22 nF (0603) on `dVdT`: t_dVdT = 20.8e3 x 12 V x 22 nF = 5.49 ms	SLVSE94G §8.3.1 Equation 2: controlled soft-start slew into KV260 bulk capacitance
`C1094`, `C1095`	1 uF 100 V 1206 X7R (`IN_SYS`), 10 uF 25 V 1206 X7R (`+12V_KV` at `J1004`)	High-voltage ceramic buffer (>= 67 V abs max on `IN_SYS`) + output decoupling at jumper
`D1004`	`SS34` (C8678, 40 V, 3 A SMA Schottky) on `+12V_KV` to `GND`	Clamps inductive negative kick on the KV260 jumper when `U1010` opens on fault (SLVSE94G §9.5.1)
`J1004`	`JST B2PS-VH` (C158007, right-angle, 10 A): pin 1 `+12V_KV`, pin 2 `GND`	Mates with `VHR-2N` / 18 AWG (15 cm) to 5.5 x 2.5 mm centre-positive barrel plug for KV260 `J12`
`R1218`, `C1223`	1 MΩ 0603 in parallel with 1 nF 2 kV X7R 1206 on `J1201` RJ45 shield to `GND`	Breaks the DC / 50 Hz earth loop to an earthed PC or switch while keeping the RF / ESD bond (`CONTROL` sheet)

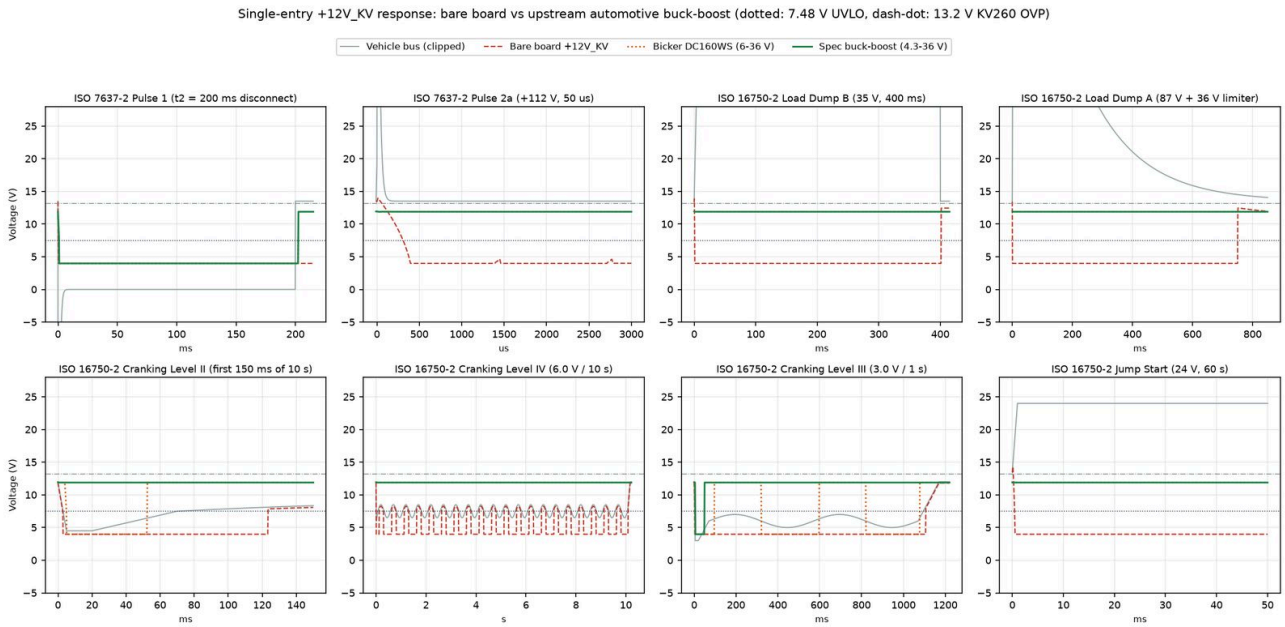
Transients (`_work/power/power_audit.py`, `docs/sim/power_transients.png`, `docs/sim/power_audit.json`). The 4-node backward-Euler solver models `J1001 -> L1004 -> VIN_J -> F1001/LM74502 (+12V)` in parallel with `Q1010/U1010 (+12V_KV)` (`D1003` SMCJ33CA clamping through `F1001`'s 40 mΩ and `L1004`'s 16 mΩ):

Pulse / Fault	VIN_J min..max	Q1010 VDS max	+12V_KV min..max	U1010 OVP / SMAJ16A	Result
ISO 7637-2 Pulse 1 (-150 V, 10 Ω, 2 ms)	-44.4..+13.4 V	57.3 V (< 100 V)	4.00..13.34 V	No trip / 0 J	**PASS**
ISO 7637-2 Pulse 2a (+112 V, 2 Ω, 50 us)	+11.4..+58.8 V	34.6 V	7.60..13.88 V	OVP at 11.7 us / 0 J	**PASS**
ISO 7637-2 Pulse 3a (-220 V, 50 Ω, 0.1 us)	+13.3..+13.4 V	0 V	13.29..13.34 V	No trip / 0 J	**PASS**
ISO 7637-2 Pulse 3b (+150 V, 50 Ω, 0.1 us)	+13.3..+13.4 V	0 V	13.29..13.34 V	No trip / 0 J	**PASS**
ISO 16750-2 Load Dump B (suppressed 35 V)	+6.4..+35.0 V	31.0 V	3.99..14.45 V	OVP at 480 us / 0 J	**PASS**
ISO 16750-2 Load Dump A (87 V unsuppressed)	+12.6..+55.8 V	52.0 V	3.78..14.55 V	OVP at 275 us / D1003 116.5 J (> 29.7 J)	**FAIL** (D1003 energy)
Jump start (24 V, 60 s, first 50 ms)	+13.4..+24.0 V	20.0 V	4.00..14.49 V	OVP at 116 us / 0 J	**PASS**
Reverse battery (-14 V, first 50 ms)	-30.3..+12.9 V	43.3 V	4.00..13.19 V	Reverse blocked / 0 J	**PASS**
ISO 16750-2 Cranking Level II (4.5 V, 15 ms)	+4.3..+13.4 V	5.4 V	3.93..13.34 V	Survives sag / 0 J	**PASS**

In every fault, +12V_KV peaks at or below 14.55 V (never reaching the KV260 SMAJ16A clamp) and VIN_J stays inside U1010's -60 to +67 V (75 V for 10 ms) limits. PASS means nothing is damaged, not that the KV260 keeps running: in every case but pulses 3a and 3b, U1010 opens or the input falls away and the KV260 resets (ISO 16750-2 functional status C). The 4 V floor of +12V_KV in the plots is where the model's loads stop drawing, not a regulated level.

Ride-through in the vehicle

The bare adapter protects both boards from damage (except unsuppressed 87 V Load Dump A), not from reset. To see whether local capacitors could keep the system running or whether an upstream pre-regulator is required, _work/power/ride_through.py (docs/sim/ride_through.json) evaluates every vehicle event against the KV260 and adapter cut-off limits:



Vehicle ride-through with upstream converter

1. Standards and fault waveforms evaluated [V]:
2. ISO 16750-2:2012 Clause 4.6.3 Table 5 starting profiles (as reproduced in TI TIDUC53 Table 8): Level I (Us = 8.0 V, Ua = 9.5 to 11.5 V, tf = 5 ms, t6 = 15 ms, t7 = 50 ms, t8 = 1.0 s, tr = 40 ms), Level II (Us = 4.5 V, Ua = 6.5 to 8.5 V, t8 = 10 s, tr = 100 ms), Level III (Us = 3.0 V, Ua = 5.0 to 7.0 V, t8 = 1.0 s, tr = 100 ms), and Level IV (Us = 6.0 V, Ua = 6.5 to 8.5 V, t8 = 10 s, tr = 100 ms).
3. ISO 16750-2:2012 Tables 6 and 7 Load Dump Test A (87 V from 79 to 101 V, Ri = 1 Ω, td = 400 ms) and Test B (35 V suppressed, Ri = 0.5 Ω, td = 400 ms); Clause 4.3.1.2 Jump Start (24 V, 60 s); Clause 4.7 Reverse Battery (-14 V, 60 s).
4. ISO 7637-2:2011 Table 2 / Figure 5 Pulse 1 (-150 V, Ri = 10 Ω, td = 2 ms, with supply disconnected for t2 = 200 ms; load dump migrated from ISO 7637-2:2004 Pulse 5a/5b into ISO 16750-2) and Table 3 Pulse 2a (+112 V, Ri = 2 Ω, td = 50 us), Pulse 3a (-220 V, Ri = 50 Ω, td = 0.1 us), and Pulse 3b (+150 V, Ri = 50 Ω, td = 0.1 us).

1. Operating floors (Vmin) and rail loads:
2. KV260 (XTP682 p. 3, XTP713, DS986, DS987): U41 (MP5016H) UVLO falls at 2.33 V [V] and the downstream MP8772GQ-Z 5 V buck (700 kHz, toff_min = 100 ns -> Dmax = 0.930, R_HS = 16 mΩ, L1 = 9.7 mΩ) drops out at 5.48 V for 11 W [E] or 5.62

V at 36 W [V] (5.32 V at the 4.75 V DS987 VCC_SOM floor). U1010 cuts off higher at 7.476 V [V] (7.48 V), setting Vmin_KV = 7.48 V with 11 W [E] typical load and 23.84 W [V] (3.189 A x 7.476 V) worst-case U1010 current-limit bound. Note that MP5016H OVP (R134 = 274 kΩ) opens above 13.2 V [V], so even a steady 13.5 V [V] alternator bus drops the KV260 without upstream regulation.

3. Adapter (SNOSDE0A, SNVSAN3F): LM74502-Q1 (Q1001/Q1003) VS POR falls at 3.2 V [V] (3.9 V rising) and has no reverse-current blocking comparator. Downstream LMR33630ADDA (+5V0 = 5.016 V, Dmax = 0.98, R_HS max = 160 mΩ, L DCR = 30 mΩ) drops out at Vmin_adp = 5.59 V [V] worst case at 2.409 A [V] (5.39 V typ; 5.06 V at the TPS56x 4.5 V floor), drawing 11.7 W typical / 13.4 W worst case [V].

1. Hold-up energy (E = P x t), capacitance (C = 2 x E / (V0^2 - Vmin^2)), U1010 start-up check, and Nichicon UHE 25 V radial bank sizing (CAT.8100M: UHE1E102MHD6 1000 uF 25 V, 12.5 x 20 mm, 35 mΩ, 1.90 A rms; UHE1E472MHD 4700 uF 25 V, 16 x 40 mm, 13 mΩ, 4.08 A rms; -40 to +105 C, 10,000 h at 105 C / 40,000 h at 85 C):

Event (V0 -> Vmin)	E_KV typ / bnd	C_KV typ / bnd (7.48 V)	C_ADP typ / wst (5.59 V)	U1010 recharge	UHE 25 V cans (typ..bnd)	Fits case
Pulse 2a (+112 V, 1.35 ms)	0.015 / 0.032 J	0.24 / 0.51 mF	0.02 / 0.02 mF	5.5 ms (**PASS**)	1..1 x UHE1E102MHD6 (3.1 cm3)	Yes (above PCB)
Pulse 1 spike alone (2 ms, unrealistic)	0.022 / 0.048 J	0.35 / 0.75 mF	0.31 / 0.35 mF	5.5 ms (**PASS**)	1..1 x UHE1E472MHD (10.2 cm3)	No
Pulse 1 disconnect (t2 = 200 ms)	2.22 / 4.82 J	35.17 / 76.22 mF	30.99 / 35.50 mF	141.6 ms (**FAIL**)	16..24 x UHE1E472MHD (163.8 cm3)	No
Load Dump B (35 V, 400 ms)	4.41 / 9.56 J	69.82 / 151.31 mF	61.99 / 70.99 mF	281.1 ms (**FAIL**)	30..48 x UHE1E472MHD (307.2 cm3)	No
Load Dump A (87 V, 757 ms > OVP)	8.33 / 18.05 J	131.80 / 285.64 mF	75.16 / 86.08 mF	530.7 ms (**FAIL**)	47..80 x UHE1E472MHD (481.3 cm3)	No
Jump Start (24 V, 60 s)	660.0 / 1430.4 J	10.45 / 22.64 F	9.30 / 10.65 F	42.1 s (**FAIL**)	4489..7083 x UHE1E472MHD (46.0 L)	No
Reverse Battery (-14 V, 60 s)	660.0 / 1430.4 J	10.45 / 22.64 F	9.30 / 10.65 F	42.1 s (**FAIL**)	4489..7083 x UHE1E472MHD (46.0 L)	No
Cranking Level I (8.0 V min, 1 s)	0 / 0 J	0 / 0 mF	0 / 0 mF	0 ms (**PASS**)	0 cans	Yes (stock C)
Cranking Level IV (6.0 V, 10 s)	111.32 / 241.26 J	2527 / 5476 mF	0 / 0 mF	10.2 s (**FAIL**)	538..1166 x UHE1E472MHD (5.51 L)	No
Cranking Level II (4.5 V, 10 s)	111.32 / 241.26 J	2527 / 5476 mF	7.89 / 9.03 mF	10.2 s (**FAIL**)	540..1168 x UHE1E472MHD (5.53 L)	No
Cranking Level III (3.0 V, 1 s)	12.43 / 26.94 J	282.15 / 611.49 mF	234.51 / 268.59 mF	1.14 s (**FAIL**)	118..188 x UHE1E472MHD (1.21 L)	No

1. Why bulk hold-up fails thermal start-up, enclosure fit, and back-feed checks:
2. U1010 thermal SOA (SLVSE94G): C1093 = 22 nF [V] sets a 2.19 V/ms ramp (5.49 ms to 12 V), hitting the 2.98 A IOL knee above 1.36 mF. Larger banks charge under current limit at 18 W average FET dissipation (12 V x 2.98 A triangular average). At 70 C (RthetaJA = 32.2 C/W [V], steady thermal regulation power 2.33 W), t(Treg_timeout) min = 2.30 s sets a no-load hard ceiling of 74.4 mF, while SLVSE94G Fig 6-18 18 W thermal shutdown trips at about 150 ms (25 C) to 45 ms (85 C) ahead of tCL_PLIM min = 129 ms. In practice, only small glitch banks around 1 mF start cleanly through U1010.
3. Enclosure pockets (_work/mech/build_case.py): tray cavities beneath the adapter are at most 7.6 mm deep (pk_kvpwr is 15.9 x 24.8 x 2.8 mm) and headroom above the adapter is 16.35 mm under the v2 fan or 25.85 mm outside the fan envelope. Only 1 x UHE1E102MHD6 (12.5 x 20 mm, Pulse 2a) fits vertically outside the fan envelope; UHE1E472MHD (16 x 40 mm) and 16 to 1168-can banks cannot fit in the enclosure.
4. 4-node solver bank checks (ride_through.json): Pulse 2a with 1 mF on +12V_KV + 0.1 mF on +12V holds 10.70 to 13.54 V / 10.95 to 17.83 V. For Pulse 1 (t2 = 200 ms), the closed-form 8 x 4.7 mF = 37.6 mF per rail still drops to 7.39 V on +12V_KV and 5.47 V on +12V because of IR drop and U1010's 1.83 ms turn-on delay; 9 x 4.7 mF = 42.3 mF per rail is needed to hold 8.28 V / 6.83 V. Load Dump B (400 ms) holds with 16 x 4.7 mF = 75.2 mF per rail (8.06 V / 12.53 V), and Cranking Level I rides through on stock 47 uF / 28.6 uF (7.73 V / 7.67 V). Because LM74502-Q1 lacks reverse-current blocking, an unmodified adapter bank back-feeds into the 4.5 V Level II cranking bus and drops +12V to 4.06 V; adding upstream reverse blocking lets 2.70 F (KV260) + 12 mF (adapter) hold 7.89 V / 5.93 V across Level II, and 300 mF + 282 mF hold 7.76 V / 6.25 V across Level III.

1. Upstream automotive buck-boost converter specification (single external module before J1001):
2. **Feed J1001 from a 4-switch automotive buck-boost converter (4.3 to 36 V continuous input, regulated 12.0 V +-2 % output strictly below KV260's 13.2 V MP5016H OVP, >= 5 A / 60 W) preceded by an active 36 V surge limiter for unsuppressed 87 V Load Dump A.**
3. Required parameters: 11.76 to 12.24 V output (<= 12.4 V max transient overshoot), -14 V for 60 s reverse-polarity

protection, and a monotonic 2 to 20 ms rise into `U1010`'s 5.49 ms `dVdT` ramp with no dwell inside the 7.48 to 8.00 V hysteresis window. A passive `SM8S33A` TVS alone reaches 43.8 V and absorbs 141.7 J during 87 V Load Dump A, exceeding its 130.7 J Wunsch-Bell limit, so unsuppressed 87 V transients require an active surge stopper that clamps rather than cuts off, such as Analog Devices `LT4363` (4 to 80 V, adjustable output clamp; its DC2062A demo limits a 100 V, 500 ms load dump to 25 V). Its fault timer and MOSFET must be sized to clamp for the whole 400 ms of Load Dump A; if the timer cuts off first, the module resets (Class C) but nothing is damaged. An over-voltage cut-off controller (`LM5060-Q1` and similar) disconnects instead and gives Class C as well. Reference buck-boost designs: `LM5118-Q1` (3 to 75 V; TI `TIDA-01179` keeps a regulated output through ISO 16750-2 Level III cold crank) and the `LTM4607` module (4.5 to 36 V, so it meets Level II at 4.5 V with no margin for the harness drop).

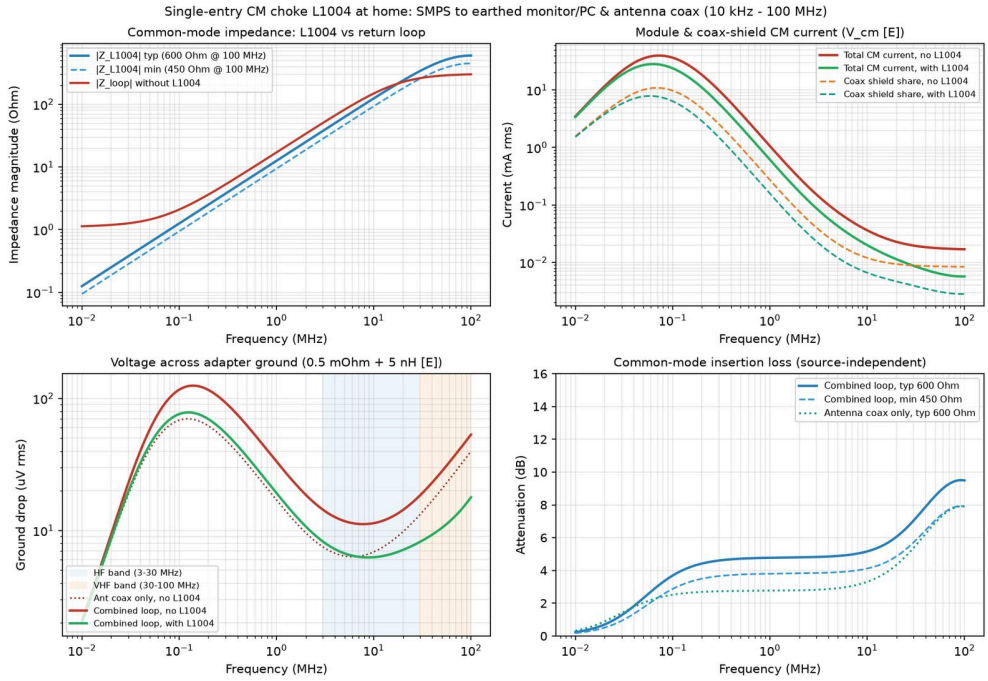
4. Never fit a 13.6 V or 13.8 V automotive battery stabiliser: KV260 `MP5016H` OVP opens permanently above 13.2 V.
5. Comparison with real COTS DC-DC modules (every gap stated honestly):
6. `Bicker Elektronik DC160WS` (`https://www.bicker.de/en/dc160ws`): 6.0 to 36.0 V in, 12.0 V +-3 % out (11.64 to 12.36 V, 120 mVpp), 8.3 A free air / 13.3 A chassis, -20 to +70 C, reverse polarity protection. Misses 4.5 V Level II and 3.0 V Level III cranking (runs Level I and IV), needs an external 36 V limiter for 87 V Load Dump A, stops at -20 C rather than -40 C, and does not specify start-up rise time.
7. `Mini-Box DCDC-USB-200` in J7 Dumb Mode (`https://resources.mini-box.com/online/PWR-DCDC-USB-200/PWR-DCDC-USB-200-manual.pdf`): 6.0 to 34.0 V in (electronic shutdown at 34 V, clamps 34 to 36 V), 12.0 V +-2.5 % out (11.70 to 12.30 V), 6 A at 6 V / 9 to 12 A at 9 to 18 V, -40 to +85 C open (-20 to +65 C cased). Misses 4.5 V Level II and 3.0 V Level III cranking, trips 1 V below 35 V Load Dump B and fails 87 V Load Dump A without an external 36 V limiter, and lists fuse-only rather than active reverse blocking.

1. 4-node solver re-run with upstream converters (`docs/sim/ride_through.json`):

Event	Bare board (no converter)	Spec 4.3 to 36 V + 36 V limiter	`Bicker DC160WS` + 36 V limiter	`Mini-Box DCDC-USB-200` (no ext. limiter)
ISO 7637-2 Pulse 1 (t2 = 200 ms disconnect)	Class C (reset)	Class C (reset)	Class C (reset)	Class C (reset)
ISO 7637-2 Pulse 2a (+112 V, 50 us)	Class C (reset)	**Class A** (runs)	**Class A** (runs)	**Class A** (runs)
ISO 7637-2 Pulse 3a (-220 V, 0.1 us)	Class A at 12 V (13.5 V > 13.2 V OVP)	**Class A** (runs)	**Class A** (runs)	**Class A** (runs)
ISO 7637-2 Pulse 3b (+150 V, 0.1 us)	Class A at 12 V (13.5 V > 13.2 V OVP)	**Class A** (runs)	**Class A** (runs)	**Class A** (runs)
ISO 16750-2 Load Dump B (35 V, 400 ms)	Class C (reset)	**Class A** (runs)	**Class A** (runs)	Class C (reset at 34 V)
ISO 16750-2 Load Dump A (87 V, 400 ms)	**FAIL** (`D1003` burns, 116.4 J)	**Class A** (runs)	**Class A** (runs)	Class C (reset)
ISO 16750-2 Jump Start (24 V, 60 s)	Class C (reset)	**Class A** (runs)	**Class A** (runs)	**Class A** (runs)
ISO 16750-2 Reverse Battery (-14 V, 60 s)	Class C (reset, protected)	Class C (reset)	Class C (reset)	Class C (reset)
ISO 16750-2 Cranking Level I (8.0 V, 1 s)	**Class A** (runs)	**Class A** (runs)	**Class A** (runs)	**Class A** (runs)
ISO 16750-2 Cranking Level IV (6.0 V, 10 s)	Class C (reset)	**Class A** (runs)	**Class A** (runs)	**Class A** (runs)
ISO 16750-2 Cranking Level II (4.5 V, 10 s)	Class C (reset)	**Class A** (runs)	Class C (reset)	Class C (reset)
ISO 16750-2 Cranking Level III (3.0 V, 1 s)	Class C (reset)	Class C (reset)	Class C (reset)	Class C (reset)

With the specified 4.3 to 36 V converter and upstream 36 V surge limiter, every continuous and over-voltage vehicle event including Level I/II/IV cold cranking, Jump Start, and Load Dump A/B stays Class A (no reset). Without external energy storage, disconnecting the supply for 200 ms (`ISO 7637-2` Pulse 1), prolonged -14 V reverse battery connection, and aged-battery Level III cranking down to 3.0 V still drop `+12V_KV` cleanly and restart once power returns (Class C).

Common-mode noise at home (`_work/power/cm_noise.py`, `docs/sim/cm_noise.png`, `docs/sim/cm_noise.json`).



Common-mode noise attenuation

With an earthed SMPS brick (120 mV peak switching factor across 50 to 150 kHz, 5 mV VHF floor, 1.0 Ω PE bond `[E]`, 1.8 m DC cord) and earthed external cables (1.5 m monitor/PC lead, 5.0 m coax, board ground 0.5 mΩ + 5 nH `[E]`):

Frequency	`	Z_L1004	` (typ)	Icm combined (no -> with L1004)	Combined IL (min 450 Ω corner)	Coax shield share	Vgnd (no -> with L1004)
65 kHz	0.82 Ω	39.44 -> 28.30 mA	2.9 dB (2.2 dB)	27.6 %	82.9 -> 59.5 uV		
100 kHz	1.26 Ω	36.58 -> 23.93 mA	3.7 dB (2.9 dB)	26.7 %	116.4 -> 76.1 uV		
1 MHz	12.57 Ω	1.06 -> 0.61 mA	4.8 dB (3.8 dB)	25.7 %	33.3 -> 19.2 uV		
10 MHz	124.2 Ω	36.2 -> 20.0 uA	5.2 dB (4.1 dB)	33.1 %	11.4 -> 6.3 uV		
30 MHz	340.9 Ω	19.6 -> 8.7 uA	7.0 dB (5.7 dB)	45.0 %	18.5 -> 8.2 uV		
100 MHz	600.0 Ω	16.9 -> 5.7 uA	9.5 dB (7.9 dB)	49.7 %	53.2 -> 17.9 uV		

Mains 50 Hz Y-capacitor leakage (230 V across 2.2 nF `[E]` = 159.0 uA rms) meets `|Z_L1004(50 Hz)|` = 4.05 mΩ and leaves 0.0795 uV across the board's ground.

Limits, said plainly.

- `L1004` adds 3 to 10 dB across 65 kHz to 100 MHz (2.9 dB at 65 kHz, 9.51 dB peak at 92 MHz), useful for cleaning switching CM current on the DC cord, and `R1218`/`C1223` isolate Ethernet `J1201`'s shield at DC/50 Hz, **but USB (`J1501` or KV260 USB to an earthed PC) and DisplayPort (to an earthed monitor) still close ground loops**: prefer a two-prong (Class II) bench brick, use a USB isolator or battery laptop on USB, and fit clip-on ferrites on earthed leads.
- **In a vehicle, feed `J1001` from a 4.3 to 36 V automotive buck-boost converter (12.0 V +-2 % output strictly below 13.2 V, >= 5 A / 60 W, with an upstream 36 V active surge limiter and a 5 A inline fuse to `J1001`)**: unsuppressed Load Dump A (87 V) exceeds `D1003`'s 29.7 J rating (116.5 J) on a bare board, and alternator voltages above 13.2 V trip KV260 `MP5016H` OVP. With that converter, only disconnecting the supply (`ISO 7637-2` pulse 1, 200 ms off), prolonged -14 V reverse polarity, or aged-battery 3.0 V Level III cranking still resets the module.

1.5 The PSU board: the converter section 1.4 asks for, feeding both boards (19 Nov)

No off-the-shelf module met the specification above (none starts below 6 V), so the project has its own: **PSU_SPEC**, KiCad project `psu/`. An LTC4364 surge stopper (Load Dump A clamped at 48 V, reverse input to -40 V) ahead of an LM5177 four-switch buck-boost (12.0 V from 2.9 to 60 V), and one TPS26631 eFuse per output. It feeds the adapter's `J1001` and the KV260's `J12` by two cables from one ground, so each board's return stays in its own cable: 38 mA a BM20 contact at the worst load against 132 mA through `J1004` (`ground_offset.py`, `vfe_two_cables`). With it the adapter's KV260 branch (`Q1010` to `J1004`) is not needed and can stay unfitted; that also removes `U1010`, whose two versions (TPS26631PWPR `C2866319`, and the same part on a 250-piece reel, TPS26631PWPT `C2832195`, a drop-in alternative) both showed no LCSC stock on 19

November.

2. Decisions this sheet makes, for your approval

Decision	Evidence	Alternative
These regulator parts	All TI, all with datasheets on hand, and three of the four already used by AERIS-10's own boards	A multi-rail PMIC
No pre-regulator for +3V3_A	Since the AD8352s moved to 5 V, +3V3_A carries 100 mA. Its LDO straight off +5V0 dissipates 0.17 W	n/a
+2V5 feeds both the FPGA's LVDS banks and the +1V8_A LDO	The FPGA's link bank must be at 2.5 V (IAS_LINK_SPEC §3); the rail already existed. The analogue 1.8 V gets there through a low-noise LDO	A separate 2.5 V LDO for the FPGA
+1V2 is a resistor divider	Its only load is the bias of two AC-coupled terminations, with no DC current. The planned "+1V2 LDO for the IAS bank" was based on the wrong bank voltage	An LDO
No power sequencing	Every regulator comes up as soon as its input does. Xilinx recommends an order for the 7 series (VCCINT, then VCCAUX, then VCCO) to minimise inrush current. **Checked in DS181 since (CONTROL_SPEC.md §4)**: the order is a recommendation; the one hard limit, VCCO − VCCAUX > 2.625 V for at most 300 ms per cycle, is met because +1V8_D is an LDO fed from +3V3_D	An EN chain, or an RC delay on each EN
Switching frequencies 400 and 580 kHz	The datasheets' own designs. Their harmonics fall in the HF band the SDR receives. The layout has to keep the switchers away from the SDR front-end inputs, and the ADCs have ferrite-filtered rails	2.1 MHz LMR33630 version: fewer harmonics in HF, a little less efficient
LM2663 gives about −3.25 V	ROUT 3.5 Ω typ × 8 mA pulls it about 30 mV below −3.3 V in magnitude. The M3SWA2 quotes VEE −3.3 V typical, −3.6 V minimum, and no maximum	A regulated negative rail
Bidirectional TVS (SMBJ15CA, now SMBJ18CA on +12V and SMCJ33CA at the input)	Superseded by §1.1	n/a

Chosen at layout (25 Sep; LAYOUT.md §5), each against its datasheet:

- **Inductors:** Bourns SRP7028A. The 8R2M has Isat 7.5 A, above the LMR33630's 5.05 A current limit. The 3R3M and 2R2M have Isat 12 A and 14 A, above the 3.5 A needed.
- **P-MOSFET:** Diodes DMP3013SFV (−30 V, −12 A, 9.5 mΩ, VGSS ±25 V), with numbered pins that match its PowerDI3333-8 footprint. **Replaced on 13 Nov (§1.1).**

The TPS7A8300's stock footprint has a 2 × 2 mm pad; check it against the RGR drawing.

3. How the drawing was verified

Check	Result
`_work/check_sheet.py power`: 38 nets exact, 19 no-connects alone, every pin of the 71 parts accounted for	**PASS**
KiCad ERC across the design	Every Rev03 rail is now driven: the `power_pin_not_driven` errors on the other sheets are gone. The 8 left belong to the old Rev01 IAS0/IAS1 sheets, which go when the root is wired

4. How to review this sheet

About 30 minutes, with the four datasheets.

1. **§2's decisions**, sequencing above all.
2. **Each regulator block against its datasheet's figure and table** (§1).
3. **The TPS7A8300 program pins**: which are grounded on each of the three.

```
py _work/check_sheet.py power
```

Source: docs/PSU_SPEC.md

PSU board: vehicle and bench power for the adapter and the KV260

A separate 110 x 70 mm board that takes the car's battery, or any 6 to 36 V bench supply, and feeds both boards of the module: the adapter through its `J1001`, the KV260 through its `J12`, each by its own cable from one ground. It replaces the regulated DC-DC converter that **POWER_SPEC** section 1.4 asked for in a vehicle: no module on the market met that specification (section 9), so this board does.

Every number below comes from the scripts in `_work/psu/` and their outputs in `docs/sim/psu_*.json`. `[V]` marks a data-sheet or standard figure, `[E]` an estimate; where an input can only be estimated, the result is also given at its bound.

1. What it does

Input	`J1` (XT30), 6.0 V to start, runs from 2.9 to 48 V (the surge clamp), 60 V on the converter
Output	12.0 V (11.68 to 12.36 V worst case), 5.3 A at most: the adapter's 2.0 A eFuse plus the KV260's 3.0 A one
To the adapter	`J2` (JST VH): 2.0 A limit (1.84 to 2.12 A), OVP 14.4 V, UVLO 8.0 V, to its `J1001`
To the KV260	`J3` (JST VH): 3.0 A limit (2.77 to 3.19 A), OVP 14.4 V, UVLO 8.0 V, to its `J12`
Efficiency	96.8 % (typical load) to 97.3 % (worst) at 13.5 V; 92 to 94 % at 6 V
Vehicle events	Runs through ISO 7637-2 pulses 2a, 3a, 3b, ISO 16750-2 Load Dump A (87 V) and B, jump start, cranking Levels I, II and IV (section 5)
Board	4 layers, 1.6 mm, 2 oz outer, 110 x 70 mm, all three connectors on one edge

```
J1 -> D1 SMCJ100A + D2 SMCJ24A (in series, opposed: +111 V / -27 V clamp)
   -> U1 LTC4364-2: Q1 IPB048N15N5 (150 V pass FET, clamps B0 at 48 V), Q2 BSC040N10NS5 (ideal diode)
   -> B0 (47 uF + 2 x 4.7 uF) -> L3 0.47 uH -> B (2 x 4.7 uF) -> L2 1.0 uH -> R2 3 mOhm (input current limit)
   -> VIN (4 x 4.7 uF + 2 x 100 uF, the filter's damping)
   -> U2 LM5177 four-switch buck-boost: Q3/Q4 BSC0805LS, R1 2 mOhm, L1 2.2 uH, Q5/Q6 BSC026N04LS -> +12V
   -> U3 TPS26631 (2.0 A) -> J2 -> the adapter's J1001
   -> U4 TPS26631 (3.0 A) -> J3 -> the KV260's J12
```

2. Why it feeds both boards by their own cables

The adapter's own single entry (KVPWR, **POWER_SPEC** section 1.4) sends the KV260's whole return current across the BM20 ground contacts, because the link (1.3 mOhm) is far lower than the jumper (33 mOhm). With two cables from this board, both returns meet on its ground and each cable carries its own board's return; the BM20 link carries only the difference of the two cables' drops (`_work/power/ground_offset.py`, `vfe_two_cables`):

Case, worst currents (adapter 1.12 A, KV260 3.19 A)	Per BM20 contact	Against 0.3 A
Cables 0.5 m / 0.5 m	36 mA	Pass
Cables 1.0 m / 1.0 m	38 mA	Pass
Cables 0.3 m to the adapter, 2.0 m to the KV260	66 mA	Pass
The same, one contact at a third of the others' resistance	178 mA	Pass
The KV260 cable's ground open (all its return across the link)	138 mA	Pass
The adapter cable's ground open	48 mA	Pass
At home, an earthed monitor on DisplayPort, 1 V between the earths	71 mA	Pass

The single entry through the adapter gave 132 mA in the first case, 352 mA with one contact at a third and 189 mA with the earthed monitor (**AUDIT_Rev08** section 6.3). With this board, the adapter's KV260 branch (`U1010`, `J1004` and their parts) is not needed: section 8.

3. Parts, and why each one

Ref	Part (LCSC)	Why
U2	TI LM5177DCPR (C7425536)	Four-switch buck-boost, 3.5 to 60 V, down to 2.8 V once its BIAS runs from the output, 85 V absolute; 2 A drivers; input average current limiter

Ref	Part (LCSC)	Why
Q3, Q4	Infineon BSC0805LS (C534374)	Input half bridge: 100 V, 8.5 mOhm at 4.5 V gate drive (the LM5177 drives at 5 V)
Q5, Q6	Infineon BSC026N04LS (C3039672)	Output half bridge: 40 V, 3.6 mOhm at 4.5 V
L1	KOHERelec MDA1870-2R2M (C3015590)	2.2 uH, saturation 35 A against a 29.3 A worst peak limit, 1.8 mOhm, AEC-Q200
R1, R2	2 mOhm, 3 mOhm 2512	Peak current 19.3 / 25 / 29.3 A; input current 16.3 / 16.7 / 17.2 A
U1	Analog Devices LTC4364HMS-2 (C580875)	Surge stopper with ideal diode: 4 to 80 V, -40 V reverse, regulates its output during a load dump instead of absorbing it
Q1	Infineon IPB048N15N5 (C536509)	150 V, 4.8 mOhm, D2PAK: the pass device; SOA at 40 V about 2.5 A DC at 25 C case [V]
Q2	Infineon BSC040N10NS5 (C534334)	100 V, 4 mOhm: reverse input and no back-feed while cranking
D1, D2	SMCJ100A, SMCJ24A (C42371542, C310039)	In series and opposed (as TI's TIDA-01179): clamp at +111 V and -27 V, so the load dump (87 V) is not absorbed and the reverse battery (-14 V) does not conduct
U3, U4	TI TPS26631RGER (C1850273)	Per-output eFuse, 60 V: a converter fault cannot reach either board; same settings as the adapter's own U1010
C17, C18	Panasonic EEE-FK1J101P (C128460)	100 uF 63 V, 0.35 ohm at 100 kHz: the damping that keeps the input filter stable (section 4.3)

Values from the LM5177 data sheet's own equations (SNVSBU4F section 8.2.2): RT 75 kOhm (400.8 kHz), FB 71.5 k / 6.49 k (12.02 V), SLOPE 54.9 k (eq. 11), CFG 3.83 k (spread spectrum on, hiccup off, current limit on), soft start 47 nF (4.7 ms), EN/UVLO 576 k / 383 k (on at 6.0 V, 5.4 to 6.7 V; off at 3.0 V, 2.9 to 3.1 V), compensation 15.8 k, 15 nF, 120 pF (eq. 3 to 5: 8.6 kHz target against a 25.7 kHz right half plane zero), CSA/CSB filter 2 x 10 ohm and 150 pF (eq. 15). LTC4364: output clamp 374 k / 10 k (48.0 V), UV 140 k / 100 k (3.0 V), timer 4.7 uF. U3 / U4: ILIM 9.09 k and 6.04 k, UVLO/OVP 316 k / 24.9 k / 30.9 k, dVdT 22 nF.

4. Electrical simulations

4.1 Steady state (psu_design.py, docs/sim/psu_design.png)

VIN	Mode	Worst load 51.7 W: efficiency, loss	Input current	Inductor peak
6.0 V	boost	91.7 %, 4.69 W	9.44 A	11.2 A
9.0 V	boost	95.5 %, 2.42 W	6.04 A	7.3 A
12.0 V	buck-boost	95.8 %, 2.26 W	4.52 A	7.9 A
13.5 V	buck	97.3 %, 1.46 W	3.96 A	5.1 A
24 V	buck	96.8 %, 1.70 W	2.24 A	7.7 A
36 V	buck	96.1 %, 2.10 W	1.50 A	8.9 A
48 V (load dump clamp)	buck	95.3 %, 2.54 W	1.09 A	9.5 A

Output ripple 2.6 mV at 13.5 V, 26 mV at 6 V (boost). Cranking at the board, with 1 m of 16 AWG each way and the input path's resistance: Level I (8.0 V) 7.6 V and 7.7 A at the worst load; Level II (4.5 V) 3.7 V and 15.8 A (under the 16.3 A limit); Level IV (6.0 V) 5.5 V and 10.8 A; Level III (3.0 V) leaves 2.5 V, under the LM5177's 2.9 V floor.

4.2 Loop stability (psu_loop.py, docs/sim/psu_loop.png)

Peak current mode, Ridley's model as TI's design equations use it, at 4.3 to 48 V and 1 W to the worst load: the lowest phase margin is 57.7 degrees and the lowest gain margin 8.5 dB (4.3 V, boost, worst load). Crossover 9 to 18 kHz in boost, 23 kHz in buck. The slope ramp is modelled as half the buck dead-beat slope [E]; the transition region near VIN = VOUT is the LM5177's own and is not modelled.

4.3 Input filter (Middlebrook)

The filter's output impedance seen by the converter peaks at 0.148 ohm (8.7 kHz, the harness and L3 + L2 against the input capacitors, damped by C17/C18). The converter's negative input impedance, V^2 / P, is 0.32 ohm at 4.3 V and the worst load: 6.7 dB of margin there, 12.5 dB at 6 V, 26.6 dB at 13.5 V. Without the two 100 uF dampers the first layout had -7 dB at 4.3 V (an oscillator during cranking).

4.4 Vehicle events (psu_transient.py, docs/sim/psu_transient.png)

Averaged time-domain model of the whole chain, both boards as constant-power loads that stop below their own cut-off (the adapter 5.59 V, the KV260 5.48 V), each standard's own waveform and source resistance (`_work/power/ride_through.py`). A board "runs" (functional status A) if its input never fell below that.

Event	Typical load: KV260 / adapter	Worst load: KV260 / adapter	Input (A) min..max	After U1 max	+12V min..max	Stress (worst load)
ISO 7637-2 pulse 1 (-150 V, 10 ohm, then 200 ms disconnected)	resets / resets	resets / resets	-30.6..13.9 V	13.7 V	7.45..12.03 V	D1+D2 365 W, 0.19 J
ISO 7637-2 pulse 2a (+112 V, 2 ohm, 50 us)	runs / runs	runs / runs	13.2..23.2 V	22.6 V	12.00..12.03 V	none
ISO 7637-2 pulse 3a (-220 V, 50 ohm, 0.1 us)	runs / runs	runs / runs	12.8..13.3 V	13.3 V	12.00..12.03 V	none
ISO 7637-2 pulse 3b (+150 V, 50 ohm, 0.1 us)	runs / runs	runs / runs	12.8..13.3 V	13.3 V	12.00..12.03 V	none
ISO 16750-2 Load Dump A (87 V, 1 ohm, 400 ms)	runs / runs	runs / runs	12.0..85.8 V	48.2 V	12.00..12.03 V	Q1 42 W, 2.5 J; timer 0.23 of 1.35 V
ISO 16750-2 Load Dump B (35 V suppressed)	runs / runs	runs / runs	12.2..34.2 V	34.1 V	12.00..12.03 V	none
Jump start (24 V)	runs / runs	runs / runs	13.2..23.8 V	23.8 V	12.00..12.03 V	none
Reverse battery (-14 V)	resets / resets	resets / resets	-14.0..13.2 V	13.2 V	7.48..12.03 V	none
Cranking Level I (8.0 V)	runs / runs	runs / runs	7.4..11.6 V	11.6 V	12.00..12.03 V	Q1 1 W, 0.5 J
Cranking Level II (4.5 V, then 6.5 V for 10 s)	runs / runs	resets / resets	3.5..11.6 V	11.6 V	7.43..12.03 V	Q1 4 W, 18.9 J
Cranking Level III (3.0 V)	resets / resets	resets / resets	3.0..11.6 V	11.6 V	7.38..12.03 V	Q1 4 W, 3.3 J
Cranking Level IV (6.0 V, 6.5 V for 10 s)	runs / runs	runs / runs	5.0..11.6 V	11.6 V	12.00..12.03 V	Q1 2 W, 11.6 J
A short on the KV260 output (`J3`)	resets / runs	resets / runs	13.3..13.3 V	13.3 V	12.00..12.01 V	none

Notes: ISO 7637-2's generator resistance (Ri) is applied while its pulse lasts; the supply's own (10 mOhm) outside it. For Load Dump A the alternator's 1 ohm is applied while the dump is above 20 V: a 55 W load cannot be fed through 1 ohm from 13.5 V at all (13.5^2 / 4 = 45 W at best), in any design. Cranking Level II at the worst load resets both boards because the input current limit (16.3 A) then leaves about 46 W; at the typical load (22.7 W) they run.

5. Thermal (`psu_thermal.py`, `docs/sim/psu_thermal.png`)

The board as placed, a 2-D plate with its copper's conductance, convection and radiation from both faces to 70 C case air (the hot car), each part's loss over its pads and its data-sheet junction-to-board resistance:

Case	Loss	Hottest parts (limit)
13.5 V, worst load, continuous	2.0 W	U4 88 C (125), U2 87 C (125), Q3 86 C (150)
24 V jump start, worst load, continuous	2.2 W	Q3 90 C, U2 89 C, Q4 88 C
6.0 V weak battery, worst load, continuous	5.2 W	Q3 106 C (150), U2 103 C (125), Q5 and Q6 100 C
Cranking Level IV, 10 s at 6.5 V from 13.5 V	4.6 W	Q3 90 C, U2 88 C

These are for 70 C air around the board. In its enclosure (**PSU_ENCLOSURE.md**) at 70 C ambient the board warms its own air: 82 C seen by the board at 13.5 V (U2 99 C, Q3 98 C, C17 92 C), 97 C at 6.0 V (U2 130 C, over its 125 C). The vented case holds U2 to 125 C at 6.0 V and the worst load up to 65 C ambient; the car running (13.5 V) stays within every rating to 85 C ambient.

6. Conducted noise (`psu_emi.py`, `docs/sim/psu_emi.png`)

Into the vehicle harness, CISPR 25 voltage method, Class 5 peak limits as TI SLLA569B (April 2025) Table 3 gives them (check them against the edition the vehicle maker asks for), with the LM5177's spread spectrum:

Band	13.5 V in: level, margin	24 V in: level, margin
MW 0.53 to 1.8 MHz (54 dBuV)	34.2 dBuV, 19.8 dB	40.5 dBuV, 13.5 dB
SW 5.9 to 6.2 MHz (53)	27.2, 25.8 dB	33.4, 19.6 dB
CB 26 to 28 MHz (44)	21.2, 22.8 dB	26.5, 17.5 dB
VHF 30 to 54 MHz (44)	31.7, 12.3 dB	36.9, 7.1 dB
VHF 68 to 87 MHz (38)	23.8, 14.2 dB	29.3, 8.7 dB

Band	13.5 V in: level, margin	24 V in: level, margin
FM 76 to 108 MHz (38)	22.1, 15.9 dB	27.4, 10.6 dB

Above 30 MHz the common mode dominates: the switch nodes' capacitance to the test bench's ground plane, 0.5 pF [E]. At 2 pF it reaches 43.7 / 48.9 dBuV, at the 44 dBuV line. The average limits (about 20 dB below the peak ones) are not assured: in the MW band this peak estimate sits on the average line (34 dBuV) before any credit for the spread spectrum, and above 30 MHz it is over it. That needs the bench. `R13` to `R16` (0 ohm) slow the switching edges if it asks for it.

Onto the two boards' supply: the switching ripple at the adapter's and the KV260's input is 42.9 dBuV (140 uV) at 400 kHz from 13.5 V and 56.7 dBuV at 6 V (boost); in the HF band (3 to 30 MHz, the adapter's `J951` input) its harmonics are under -29 dBuV from 13.5 V and under 6.5 dBuV (2 uV) from 6 V, far below what the adapter's own regulators make.

7. The board (`psu/`, `_work/psu/psu_pcb.py`)

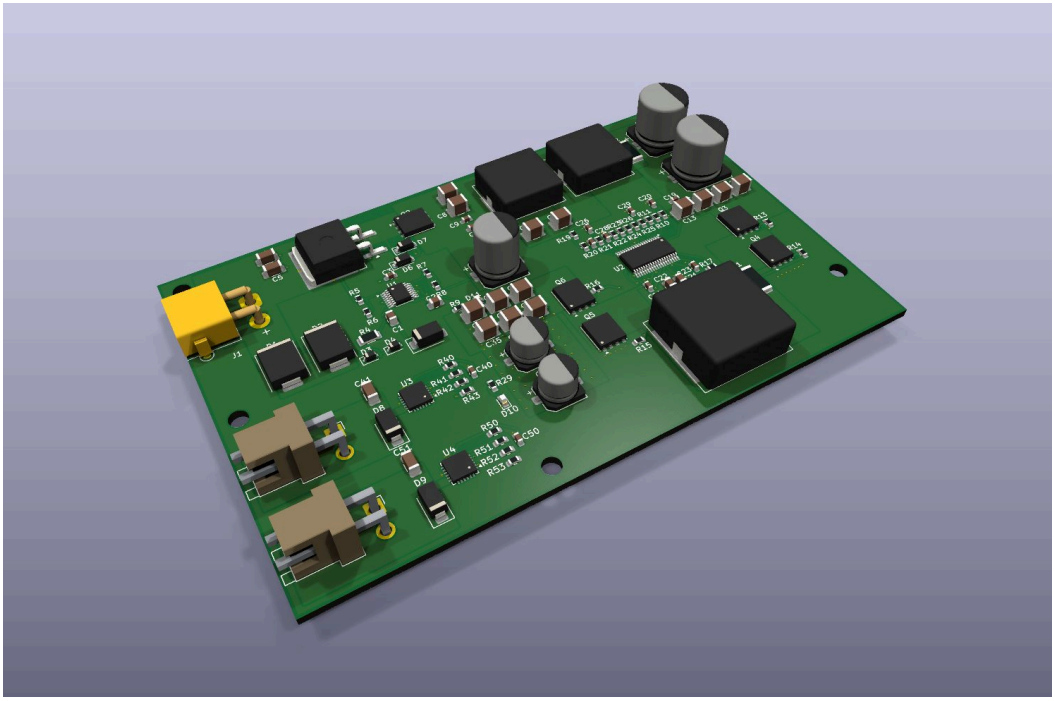
Schematic: KV260-IAS2RF_PSU_schematic.pdf (vector, one A1 sheet); layout: KV260-IAS2RF_PSU_layout.pdf (vector, the four copper layers and their overlay). Both are assets of the release.

4 layers: F.Cu the parts and the power pours, In1.Cu ground, In2.Cu the +12V plane, B.Cu ground and short signal links. The power runs in a U: `J1` top left, protection and filter along the top, the power stage along the bottom from right to left, the outputs bottom left, so the three cables leave one edge. The input loop (VIN capacitors, `Q3`, `Q4`) is closed within 10 mm, the output loop (`Q6`, the output capacitors, `Q5`) likewise; the gate drives run 15 to 20 mm from `U2`. The three connectors open on the left edge: `J1`'s XT30 and the two VH sockets, whose plugs (`VHR-2N`) leave the board edge-on.

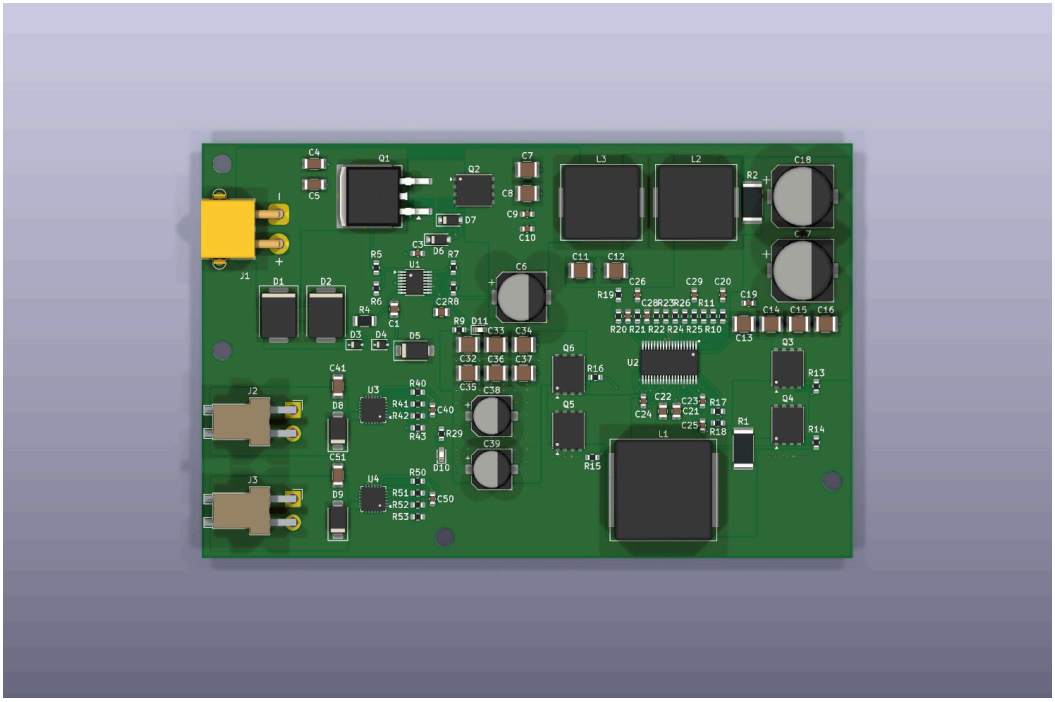
DRC with the zones refilled and schematic parity: 0 errors, 0 unconnected (the warnings left are silkscreen clipped at the edge and the mounting holes' library copy). ERC 0. Fabrication: `_work/psu/psu_fab.py` (Gerbers, drill, BOM of 65 lines and 102 parts, every one with an LCSC code, CPL) into `fab/`.

3-D bodies: KiCad's own where its library ships them. `J1` is a stand-in built from its footprint's outline (`_work/mech/xt30pw_model.py`), `J2`/`J3` the adapter's VH model, and the SON-8 MOSFETs and the electrolytics use copies of KiCad's models with their near-white metal toned to grey (`psu_pcb.py`, `tone_models`).

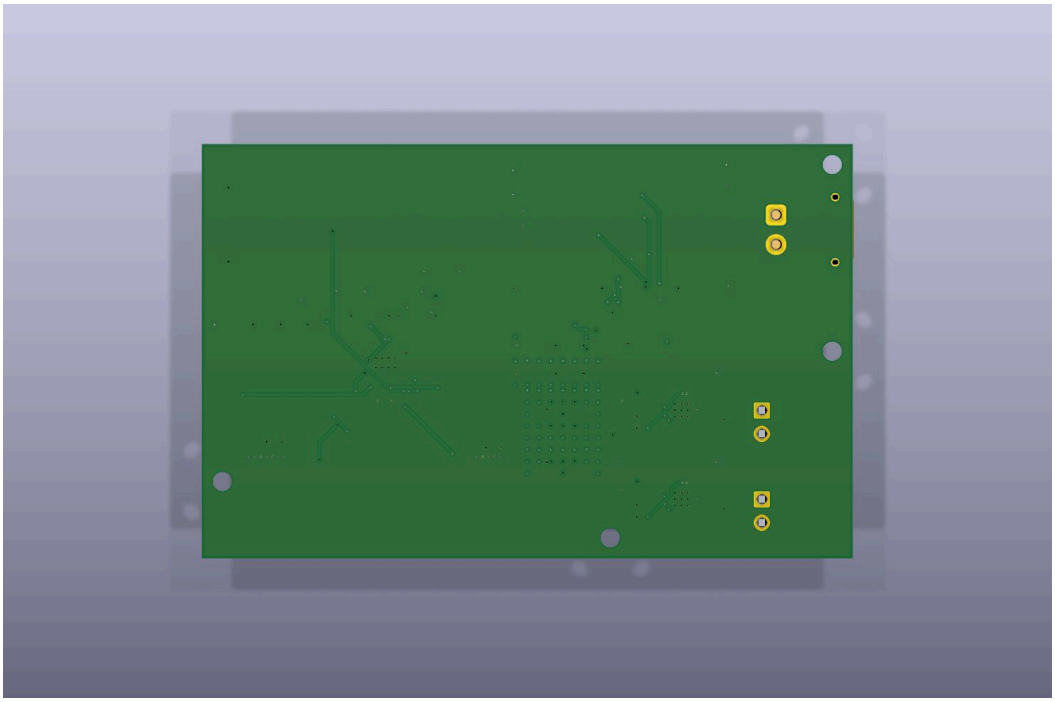
Reference designators are on the top silkscreen, placed clear of every pad and courtyard by `_work/psu/psu_silk.py` (C27 and R12 have no room and stay on the assembly drawing); the solder mask is a green that lets the pours show through. `_work/psu/psu_render.py` renders these views from a refilled copy, and `_work/psu/psu_site.py` puts the board, its nets and its analysis in the site's 3-D explorer.



PSU board

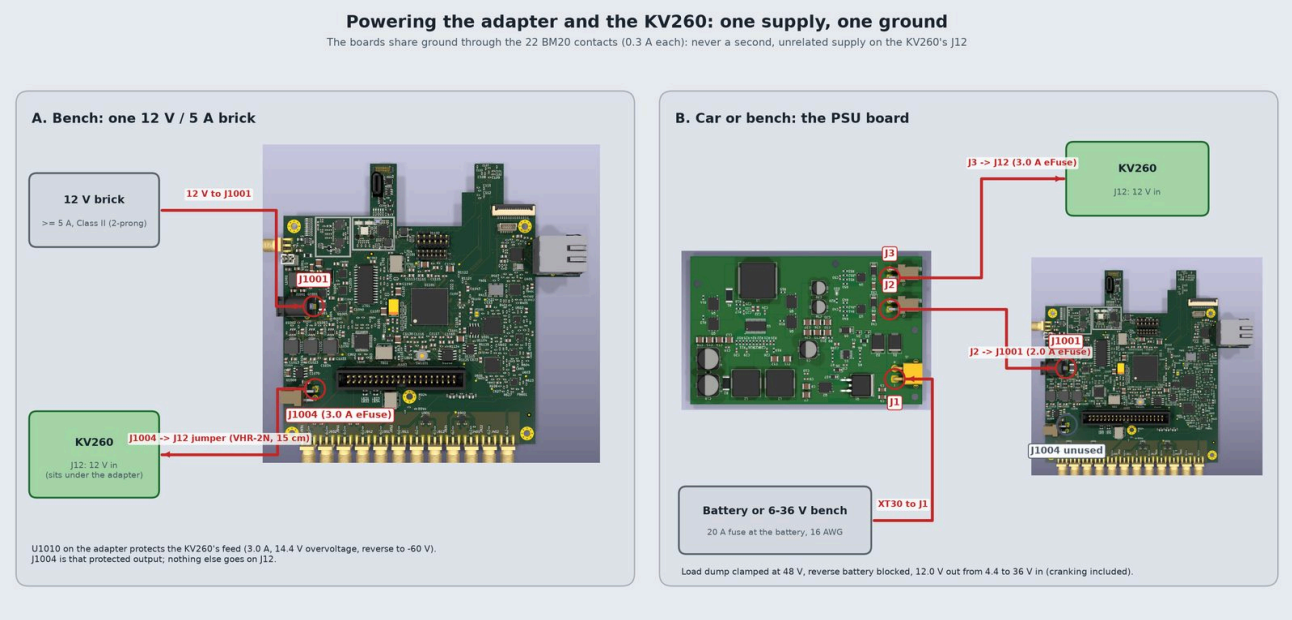


PSU board, top



PSU board, bottom

8. Installation



The two ways to power the boards

- **Vehicle:** `J1` to the battery by 16 AWG, a 20 A fuse at the battery, the ground to the same chassis point as the CAN cable's ground (`J1503`). `J2` to the adapter's `J1001` and `J3` to the KV260's `J12`, each by its own 18 AWG cable (1 m or less, the two about the same length), nothing else on `J12`.
- **Bench:** any 12 to 24 V supply of 60 W on `J1`, preferably two-prong (Class II); the same two cables.
- **Enclosure:** the printed ASA case in **PSU_ENCLOSURE.md**: four M3 x 25 screws hold the board and close it, four ears with M5 slots mount it floor down, so the vents in its long walls stay vertical.
- **The adapter's KV260 branch** (`U1010`, `Q1010`, `Q1011`, `R1040` to `R1043`, `C1093` to `C1095`, `D1004`, `J1004`) is not needed with this board and can be left unfitted. It stays on the board for use with a plain brick and the jumper. `U1010` is TPS26631PWPR (LCSC C2866319); the same part on a 250-piece reel, TPS26631PWPT (C2832195), is the drop-in alternative. Both showed no stock at LCSC on 19 November 2026; the RGE (VQFN) version this board uses (C1850273) had 314.

9. Limits, said plainly

- In the vented enclosure, a battery held at 6.0 V with both boards at their worst draw takes U2 past its 125 C at ambients above 65 C (53 C sealed). At 13.5 V the limit is not reached below 85 C; the input electrolytics' life is then the measure: 2.5 times their rating at 70 C ambient, 0.9 times at 85 C (**PSU_ENCLOSURE.md**).
- Disconnecting the battery (ISO 7637-2 pulse 1, 200 ms), a reverse battery and cranking Level III (3.0 V) still reset both boards: there is nothing to run from. Nothing is damaged.
- Cranking Level II at both boards' worst draw at once resets them (section 4.4); the typical load runs.
- Held below 4.4 V at the worst load and 70 C air, the hottest MOSFET passes its 150 C rating (156 C at 4.3 V, from `psu_design.py`'s steady-state model; 122 C at 5.0 V, 101 C at 6.0 V). Cranking is that low for milliseconds (Level II holds 4.5 V for 15 ms), far shorter than the parts' thermal time constants; a battery that stays that low does not start the car.
- The averaged models do not show the switching ripple, the LM5177's transition region or the parasitics of the layout. The loop compensation and the IMON loop (`R25`/`C29`) are the data sheet's starting values, to be checked on the bench; so are the emissions above 30 MHz.
- Off-the-shelf modules checked before this board: Bicker DC160WS (6 to 36 V), Mini-Box DCDC-USB-200 (6 to 34 V), DFRobot 5 A buck-boost (6 to 35 V), Analog Devices DC1198B-B (6 to 36 V as built); none starts below 6 V, so none holds the module through cranking Level II.

10. Audit (`psu_audit.py`, `docs/sim/psu_audit.json`)

Checked on 19 November 2026, against the data sheets and the simulated extremes:

- **Every IC pin against its data sheet's pin table** (93 pins: LTC4364-2 MS16, LM5177 HTSSOP-38, two TPS26631 VQFN-24). Each pin left open is one its data sheet allows open: the LM5177's `HO1_LL`/`HO2_LL` ("make no external connection"), the TPS26631s' `B_GATE`, `DRV`, `IMON`, `FLT` and `PGOOD`, their `SHDN` (open-circuit 2.48 to 3.3 V, above its 2 V threshold), the LTC4364's `ENOUT` and `SHDN` (an internal current source to a 4 V clamp; the board's leakage there must

stay under 1 uA, so keep it clean of flux). The pins that must not float are tied as their data sheets say: `DTRK` to ground, `SYNC` and `MODE` (forced PWM) to `VCC`, `OV` to ground (the OV comparator unused), `IN_SYS` to `IN`.

- **Every pin's absolute maximum against its net's worst voltage**: the LTC4364's `VCC` (100 V) sees at most D5's 62.7 V breakdown; its `SOURCE` and `OUT` the 48 V clamp (52 V with tolerances); the LM5177's `VIN`, `SW1`, `CSA`/`CSB` (85 V) the same 52 V, its `BIAS` (50 V) 14.4 V; the TPS26631s' `IN` and `OUT` (67 V) 14.4 V.
- **Every part's voltage against its rating** (ceramics at 80 %, electrolytics at 85 %): the highest are `C6`, `C17`, `C18` (63 V electrolytics, 52 V for the 400 ms of a load dump: 83 %), `C1` and `C3` (100 V, 63 %), `Q1` (150 V, 77 V across it in the clamp: 51 %), `Q2` (100 V, 54 V in a negative pulse: 54 %).
- **Every resistor's dissipation**: the shunts `R1` (2 W part) 0.43 W and `R2` (3 W) 0.89 W at their worst currents; the dividers under 40 mW.
- **The simulation** (section 4.4): after `U1` the bus never passes 48.2 V; `Q1` takes at most 18.9 J (cranking Level II, within its SOA averaged over 1 ms); the TVS pair at most 0.19 J (rated 1500 W for 1 ms); no part is overstressed in any event.

Changed by this audit:

- **`R4`** (`U1`'s `VCC` feed): in Load Dump A, `D5` clamps `VCC` and `R4` takes 0.88 W at the peak, 23.5 mJ over 92 ms, over a plain 1206's 0.25 W. It is now an anti-surge 1206, Panasonic ERJ-P08F1001V (0.66 W, LCSC C4261071). It stays 1 kohm: more would stop `U1` starting from 6 V (its `VCC` needs 4 V at 750 uA).
- **`J2`, `J3`**: turned so that their openings face the board edge, with the plugs leaving edge-on (they first faced inwards; the 3-D render showed it).

Left for the bench: the loop with the real layout, the `IMONOUT` compensation (`R25`, `C29`), conducted emissions above 30 MHz and the CISPR 25 average limits, and the switching nodes' ringing (`R13` to `R16` are there to slow them).

Source: docs/PSU_ENCLOSURE.md

PSU board enclosure

A printed case for the **PSU board**, in the main enclosure's honeycomb (10 mm cells, 1.6 mm walls): a tray and a lid, four M3 screws that hold the board and close the case at once, honeycomb vents in the long walls, and four ears with M5 slots. The simulations below answer whether it needs vents (it does), what it should be printed in (ASA, not PETG-CF), and whether it holds the board through shocks, cable pulls and a knee on the lid.



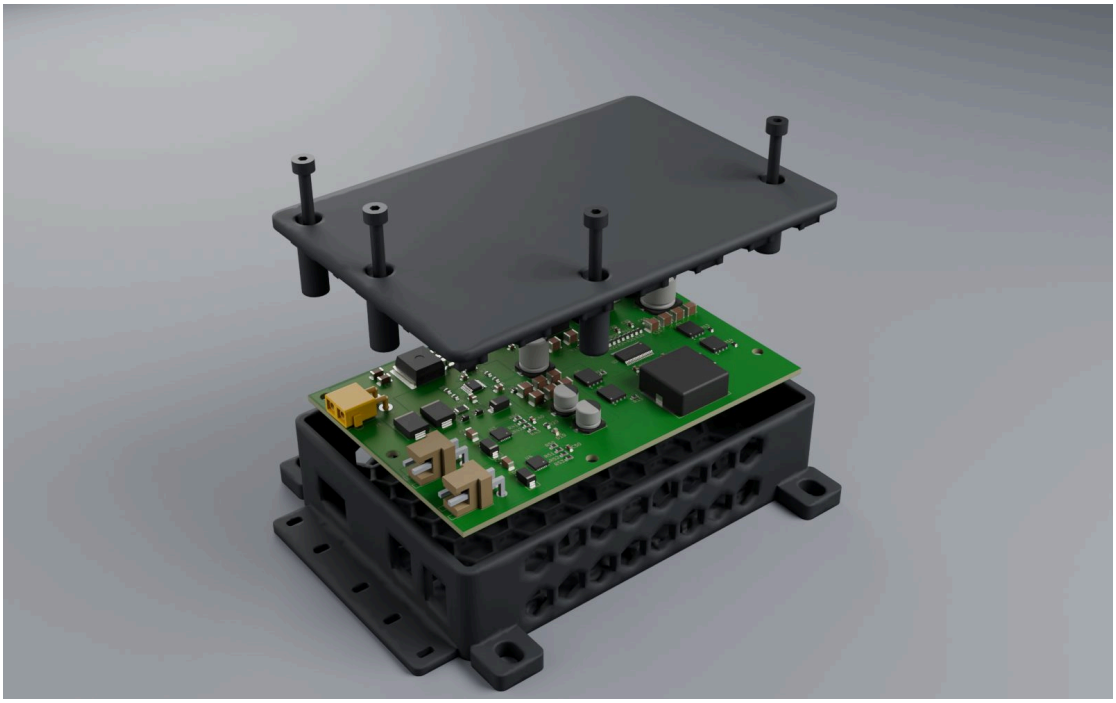
The PSU enclosure, closed

`[E]` marks an engineering estimate, `[I]` a typical or inferred value, `[C]` a textbook correlation.

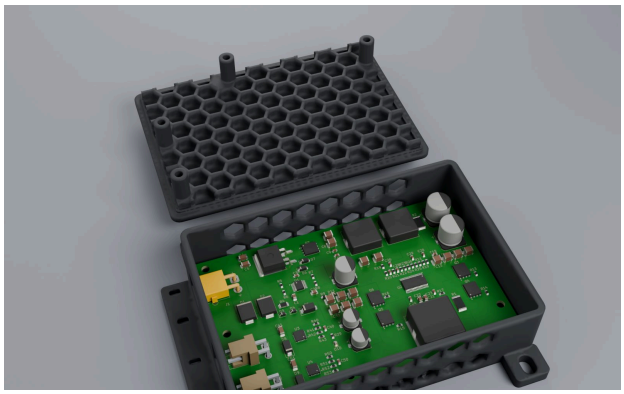
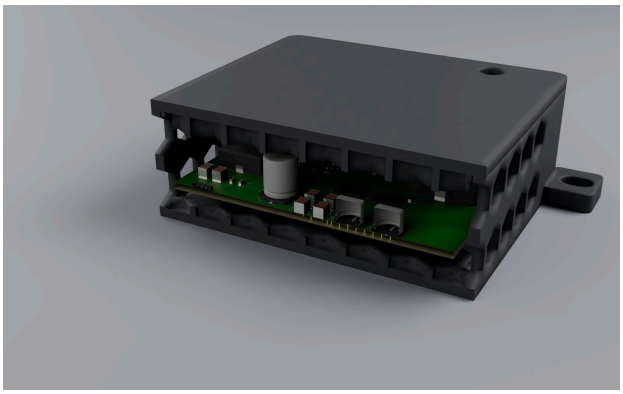
1. The design (`_work/psu/psu_case.py`)

Outside	117 x 80 x 30 mm (ears and cable shelf excluded); 129 x 104 mm over the ears and the shelf
Board	6.0 mm above the floor on four stand-offs with M3 x 5.7 heat-set inserts (4.0 mm hole, 7 mm deep), clamped from above by four posts in the lid; six rests under its bare underside carry it between the holes
Screws	four M3 x 25 DIN 912 (A2 stainless or black-oxide steel), through lid, post and board into the inserts; the heads sit in 6.5 mm counterbores
Tray	2.5 mm walls and floor; honeycomb ribs 2 mm high over the whole floor; a conical foot under each stand-off and rest
Lid	2.5 mm, closed on top; honeycomb ribs 5 mm deep underneath, 2.4 mm clear of the tallest parts (C6, C17, C18); a 1.2 mm lip locates it in the tray
Connectors	`J1` (XT30, battery), `J2` (to the adapter's `J1001`) and `J3` (to the KV260's `J12`) through openings in the left wall, 0.8 mm round each mating face
Cable shelf	12 mm under the openings, five slots for cable ties (up to 3.6 mm wide) either side of each cable
Vents	in each long wall, two rows of eight honeycomb cells (8.4 mm across flats, vertex up so they print without support): 978 mm2 low, 978 mm2 high, 13.8 mm apart
Mounting	four ears with M5 slots at the floor, as the main case's
Mass	about 96 g of ASA (tray 56 g, lid 39 g, solid)

The board's mounting holes decide everything above: they are not at the corners, so the posts that clamp the board also carry the lid, and no screw goes into the walls. The lid's honeycomb keeps a flat 2.5 mm plate stiff; the floor's carries the stand-offs. The first FEA of this design (3 mm lid ribs, no rests) failed twice, and the two fixes came from it: a 300 N press bent the lid 2.1 mm, to 0.4 mm from C6, so the ribs went to 5 mm; a 50 g shock bent the board's far corners round its four holes (730 microstrain), so it now lies on six rests.



Exploded: tray, board, lid and screws

The lid's honeycomb and posts	Section at x = 148 mm through a vent column
	
Lid underside	*Section*



The vented long wall and the ears

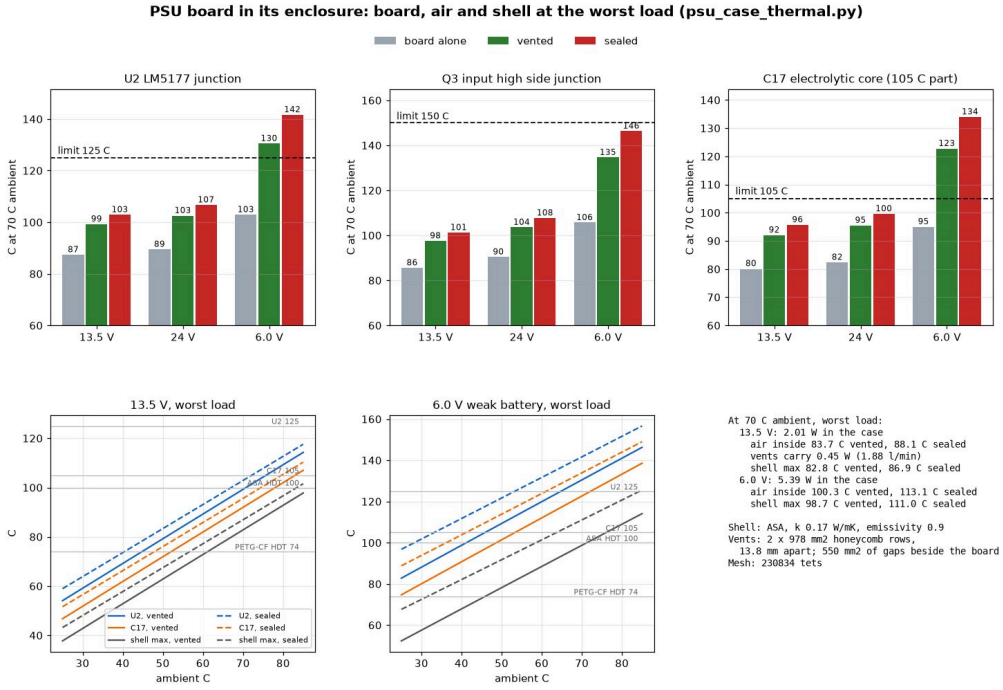
2. Printing and assembly

- **Material: ASA.** With the car running the shell's hottest spot is 13 C above ambient (section 3): 83 C at 70 C ambient, past PETG-CF's 74 C heat deflection temperature and well within ASA's 100 C. PETG-CF is fine below 61 C ambient with the car running.
- **Orientation:** the tray on its floor, the lid on its top face. Nothing needs support: the vents are hexagons standing on a vertex, the connector openings bridge 9 to 13 mm.
- **Settings:** 0.2 mm layers, 4 walls, 40 % infill; the walls, ribs and posts are thin enough to print solid.
- **Assembly:** press the four inserts into the stand-offs with a soldering iron; lay the board in, connectors to the openings; put the lid on and drive the four M3 x 25 screws to snug (about 0.5 N m: the joint is plastic).
- **Mounting:** floor down on the four ears, M5 screws with washers, on rubber isolators as the main case. Keep the long walls clear by 10 mm so the vents breathe. Tie each cable to the shelf.

3. Thermal: does it need vents? (`_work/psu/psu_case_thermal.py`)

Model. Coupled steady state:

- **The board: PSU_SPEC §5**'s 2-D model, its losses recomputed at the temperature it sees in the case (the MOSFETs' resistance rises with it).
- **The shell:** 3-D conduction in the tray and lid as meshed (231 k tetrahedra, ASA k = 0.17 W/mK [I]).
- Outside: natural convection on each face by its orientation [C] and radiation, emissivity 0.9 [E].
- Inside: convection to one well-mixed air node.
- The board's radiative share lands on the lid and floor under it, spread by its own temperature map.
- **The vents:** stack flow through the low row, up the 2.5 mm gaps beside the board and out of the high row, Cd 0.6 for the cells and 0.8 for the gaps [E].
- **Sealed:** the same case with the vents closed.
- The loop runs until the temperature the board sees settles. The board alone at 70 C air (**PSU_SPEC §5**) is the reference.



Board, air and shell at the worst load

At 70 C ambient, both boards at their worst draw:

Case	In the case	Air inside, vented / sealed	U2 (125 C)	Q3 (150 C)	C17 core (105 C part)	Shell max
13.5 V, car running	2.0 W	84 / 88 C	99 / 103 C	98 / 101 C	92 / 96 C	83 / 87 C

Case	In the case	Air inside, vented / sealed	U2 (125 C)	Q3 (150 C)	C17 core (105 C part)	Shell max
24 V jump start	2.3 W	85 / 90 C	103 / 107 C	104 / 108 C	95 / 100 C	84 / 89 C
6.0 V weak battery	5.4 W	100 / 113 C	**130** / **142** C	135 / 146 C	**123** / **134** C	99 / 111 C
Cranking Level IV, 10 s at 6.5 V		(the case frozen at its 13.5 V state)	100 / 104 C	102 / 106 C	93 / 96 C	

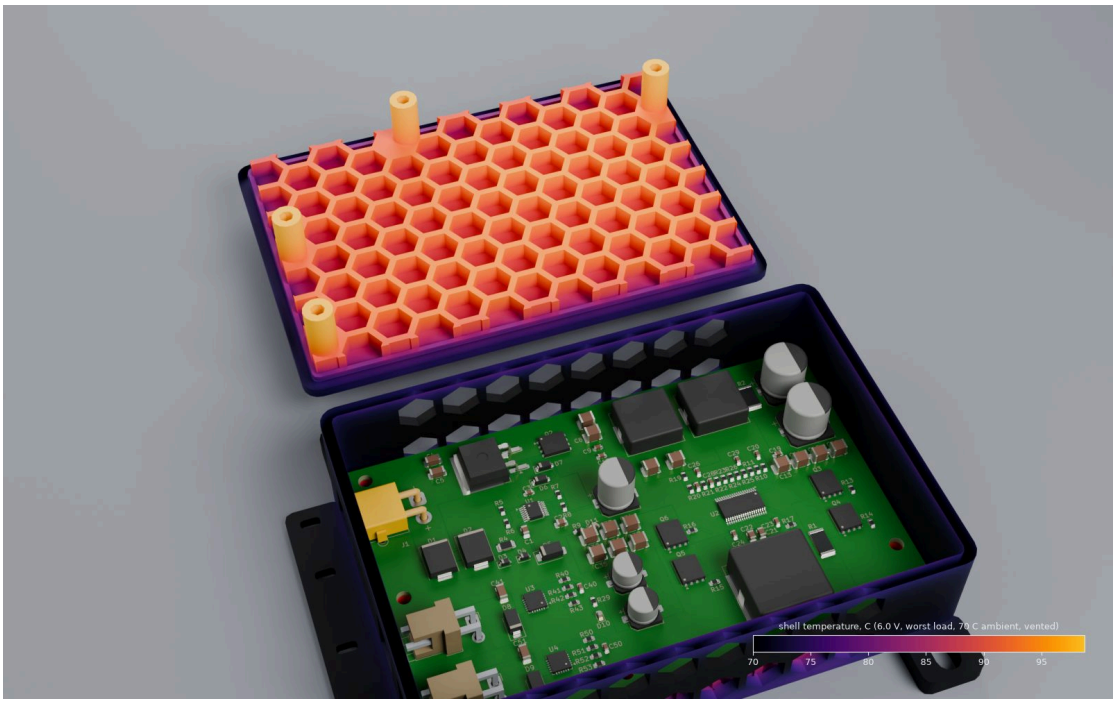
Highest ambient for each limit (vented / sealed):

Limit	13.5 V, car running	6.0 V weak battery
U2 junction 125 C	above 85 / above 85 C	65 / 53 C
Q3 junction 150 C	above 85 / above 85 C	84 / 73 C
C17 at its 105 C rating	83 / 80 C	53 / 41 C
ASA shell at its 100 C HDT	above 85 / 83 C	71 / 59 C
PETG-CF shell at its 74 C HDT	61 / 57 C	46 / 32 C

What this says:

- **The case adds 12 C** to what the board sees at 13.5 V (82 C at 70 C ambient instead of PSU_SPEC's 70 C air), and 27 C at 6.0 V. The board in 70 C air was the optimistic view.
- **The vents are needed.** They carry a fifth to a quarter of the heat (0.45 W of 2.0 W at 13.5 V, 1.5 W of 5.4 W at 6.0 V, 1.9 to 2.8 l/min) and take 3.5 C off U2 with the car running and 11 C at 6.0 V. Sealed, the weak-battery case loses U2 above 53 C ambient; vented, above 65 C.
- **With the car running** every part stays within its rating to 85 C ambient. The input electrolytics (C17, C18, Panasonic FK, 105 C) set the life: at 70 C ambient they run at 92 C, 2.5 times their rated life (life halves each 10 C); at 55 C, 7 times; at 85 C, 0.9 times.
- **A battery held at 6.0 V with both boards at their worst draw** is the case that does not pass at 70 C ambient. It takes a battery too weak to start the car, held there while both boards draw their maximum; even in open 70 C air U2 was 22 C from its limit there.
- **Lid vents** would add little: the lumped estimate made before drawing the case put an exhaust in the lid (twice the area, 19 mm of chimney) 1 to 3 C below these side rows, and the closed lid keeps drips and dust out.

The shell at the weak-battery case (lid turned over beside the tray; the hot spots face up):



Shell temperature

The lid runs hottest over the switching stage, where the board radiates most, and at its posts, which touch the board.

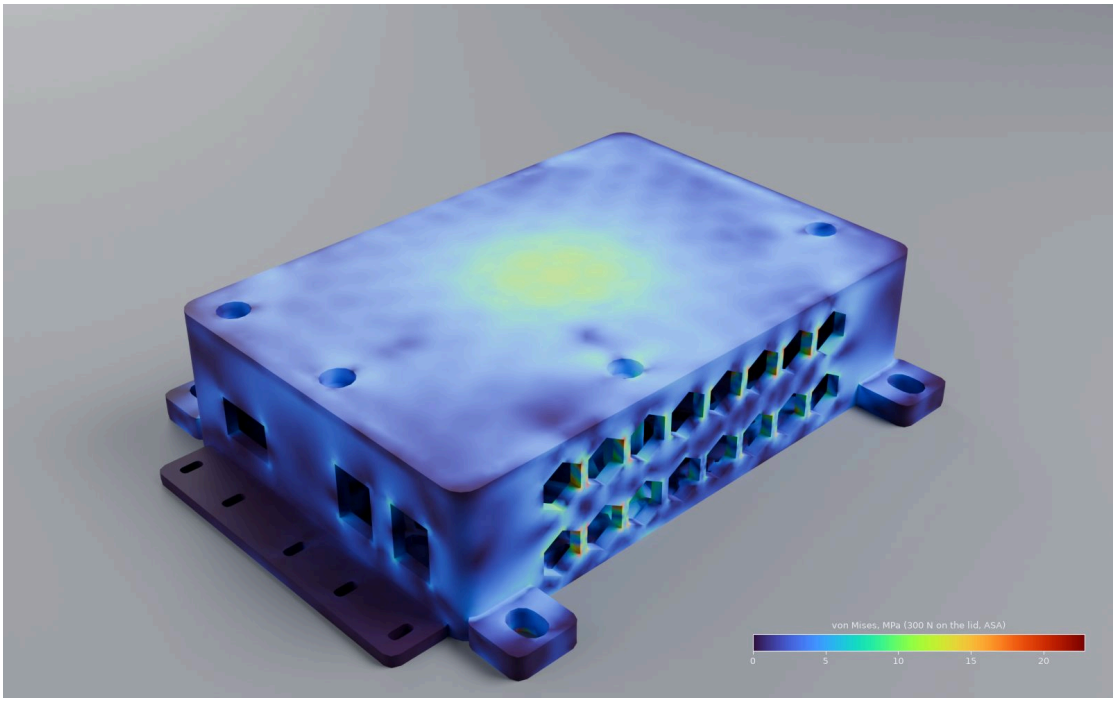
4. Structural FEA (`_work/psu/psu_case_fea.py`)

Model (the main case's method, **ENCLOSURE.md §5.3**):

- **Bodies:** tray, lid and board meshed together in CalculiX, 10-node tetrahedra (254 k tets, 1.4 M degrees of freedom). The board is FR-4 carrying its 50 g of parts [E] as density.
- **Bonding:** the board is bonded to the stand-offs, the rests and the lid's posts (the screws clamp that stack). The lid is bonded where it sits on the walls, exact for loads that press it on, slightly stiff for any that would lift it (the screws carry those).
- **Supports:** the four ears held at their M5 washers.
- **Materials:** ASA and PETG-CF, each at 23 C and at 70 C, with the main case's modulus and strength factors. The shell's von Mises stress (99.7th percentile, as for the main case, and the peak) is checked against the across-layer strength: ASA 25 / 20 MPa, PETG-CF 29 / 17.4 MPa. The board's largest principal strain is checked against the 500 microstrain guide.
- **Loads:**
- 50 g quasi-static shocks down, sideways and fore-aft;
- a cable pulled at 50 N out of `J1`, and at 30 N out of `J2` and `J3` together;
- 300 N on a 30 mm disc at the lid's centre: a knee, or luggage;
- the first natural frequency.

ASA (the material this case is for), 23 C / 70 C:

Load	Shell, 99.7th pct / peak	Safety factor, 99.7th pct	Board strain, 99.7th pct / peak	Max displacement
50 g down	1.5 / 3.3 MPa	16 / 13	208 / 339 microstrain (242 / 399 at 70 C)	0.06 mm
50 g sideways	0.5 / 1.7 MPa	49 / 39	74 / 124	0.01 mm
50 g fore-aft	1.1 / 2.9 MPa	23 / 18	109 / 165	0.02 mm
`J1` cable, 50 N	0.6 / 1.9 MPa	39 / 31	141 / 218	0.02 mm
`J2` + `J3` cables, 30 N each	0.7 / 2.8 MPa	34 / 27	164 / 311	0.04 mm
300 N on the lid	18.3 / 27.1 MPa	1.4 / 1.1	1117 / 2008 (1376 / 2475 at 70 C)	1.2 mm (1.5 at 70 C)
First mode				552 Hz (500 at 70 C)



300 N on the lid, ASA

What this says:

- **Shock, vibration and cable pulls are easy.** The shell's safety factors are 13 or more, and the board stays under half

the 500 microstrain guide (it has no BGA; the guide is the main case's, kept for comparison). With a first mode above 500 Hz, rubber isolators decouple the case as cleanly as the main one's.

- **300 N on the lid** passes at the 99.7th percentile (1.4 cold, 1.1 hot). Its peak is at the foot of the `H3` stand-off where it meets the wall (133.8, 172.5 mm), a re-entrant corner where the linear model's stress grows with mesh refinement; it reaches the across-layer strength there (0.92 cold, 0.74 hot). The lid sags 1.2 mm (1.4 hot) and stays 1.4 mm (1.2 hot) clear of `C6`, the tallest part under it, so nothing presses on the board's parts; the board itself takes 1100 to 1400 microstrain round the post. Do not stand on it; a knee or a bag is the limit.
- **PETG-CF at 70 C** (already above its heat deflection temperature in section 3): the lid sags 2.6 mm under 300 N, to 0.25 mm from `C6`, and the board's shock strain doubles. ASA it is.

Raw results: **`sim/psu_case_fea.json`**.

5. Limits, said plainly

- The thermal model is steady state with one mixed air node, natural convection correlations and an estimated orifice coefficient; sun on the case, a hot panel under it or a closed glovebox are not in it. Ratings in section 3 are for still air at the stated ambient.
- The FEA is linear and quasi-static: no contact at the lid's seat (it only rests there, so it was left free), no layer orientation (one modulus, the mean of in-layer and across-layer), the screws' preload not modelled.
- The board's 50 g is an estimate spread over its volume; the parts' own masses (L1, the electrolytics) are not lumped where they sit.
- Not tested in print yet: fit of the connectors' mating plugs through the openings, and the inserts' pull-out in ASA.

6. Files

File	What
`mech/psu_case_tray.stl`, `mech/psu_case_lid.stl`	the parts to print
`_work/psu/psu_case.py`	the geometry (gmsh/OpenCASCADE); STEP of each part in `_work/psu/cache/`
`_work/psu/psu_case_thermal.py`	section 3; `docs/sim/psu_case_thermal.json`, `.png`
`_work/psu/psu_case_fea.py`	section 4; CalculiX in WSL; `docs/sim/psu_case_fea.json`
`_work/psu/psu_case_render.py`	the renders (Blender Cycles, the main case's studio and materials)
`site/assets/psu_case.glb`	the case in the 3-D explorer (`node site/scripts/build_assets.mjs --psu-case`), beside the PSU board, following the Closed / Open Lid / No Case buttons

Source: docs/SYMBOLS.md

Symbol libraries

Updated: 23 September 2026 (clock parts added the same day)

A symbol whose pins are all `unspecified` makes ERC blind. That is exactly what produced the 48 uninterpretable `pin_to_pin` conflicts in the Rev01 work (**history/AUDIT_Rev01.md** §2.2), and it is why this work exists: **every pin the design uses has to carry a real electrical type**, or the verification story is theatre.

1. KiCad official libraries, used as-is

Not rebuilt. They ship with KiCad 10, are maintained, and copying them into a project library would only create a second version to drift.

Part	Library	Notes
XC7A50T-FTG256	`FPGA_Xilinx_Artix7`	The front-end FPGA. 256 pins, 4 units, 188 bidirectional + 68 `power_in`. Exactly the package AERIS-10 uses
~~AD9708AR~~	`Video`	Radar DAC. Replaced on 24 Sep by a project symbol from the datasheet: the stock one omits the NC pins and forced crossings. It stays the second source
ADF4351	`RF`	SDR synthesiser for the front-end board

That the hardest symbol in the design, a 256-ball BGA, was already available and correctly typed was the single biggest saving in this phase.

2. Project library: `symbols/kv260-ias2rf.kicad_sym`

Generated by `_work/make_symbols.py`, registered in `sym-lib-table` as `kv260-ias2rf`. **Eighteen symbols, sixteen of them from the manufacturer's datasheet.**

Symbol	Pins	Source	Electrical types	Role
`AD9484BCPZ-500`	57	**datasheet**	21 output, 18 power_in, 9 no_connect, 7 input, 2 bidirectional	radar ADC (drawn, sheets/ADC_RADAR)
`AD9253BCPZ-125`	49	**datasheet**	21 output, 15 input, 10 power_in, 2 bidirectional, 1 passive	SDR ADC
`AD9767ASTZ`	48	**datasheet**	35 input, 6 power_in, 4 output, 2 passive, 1 bidirectional	SDR DAC
`ADCLK948BCPZ`	33	**datasheet**	18 output, 7 power_in, 5 input, 2 passive, 1 no_connect	clock select + fan-out (drawn, sheets/CLOCK)
`Si549_PinoutC`	8	**datasheet**	2 input, 2 power_in, 2 output, 1 bidirectional, 1 no_connect	master XO (drawn, sheets/CLOCK)
`ADCLK944BCPZ`	17	**datasheet**	9 output, 5 power_in, 2 input, 1 passive	first clock plan; superseded by the ADCLK948
`LMR33630ADDA`	9	**datasheet**	3 power_in, 2 input, 1 open_collector, 1 power_out, 1 passive, 1 output	12 V → 5 V buck (drawn, sheets/POWER)
`TPS562201`	6	**datasheet**	2 power_in, 2 input, 1 output, 1 passive	bucks ×2 (`U1003`, `U1004`; `U1002` upgraded to `TPS563201` in Rev08 audit, drawn sheets/POWER)
`TPS7A8300RGR`	21	**datasheet**	9 passive, 7 power_in, 3 input, 1 power_out, 1 open_collector	LDOs ×3 (drawn, sheets/POWER)
`LM2663M`	8	**datasheet**	3 passive, 2 input, 2 power_in, 1 power_out	−3V3 inverter (drawn, sheets/POWER)
`MT25QL128ABA1ESE`	8	**datasheet**	4 bidirectional, 2 input, 2 power_in	FPGA configuration flash (drawn, sheets/CONTROL). Micron Rev. K Figure 6; cross-checked against KiCad's MT25QU
`AD8352ACPZ`	17	**datasheet**	7 power_in, 4 passive, 3 input, 2 output, 1 bidirectional	ADC driver (drawn ×2, sheets/ADC_RADAR)
`M3SWA2-34DR`	17	**datasheet**	10 power_in, 6 passive, 1 input	RF switch
`LTC5552`	13	**datasheet**	8 power_in, 3 passive, 2 input	mixer (AERIS-10)
`AD9523BCPZ`	73	**datasheet**	33 output, 17 power_in, 16 input, 3 power_out, 3 bidirectional, 1 passive	clock (AERIS-10)

Symbol	Pins	Source	Electrical types	Role
ADAR1000ACCZN	89	Eagle	52 passive, 16 input, 13 output, 8 power_in	beamformer (AERIS-10)
ADF4382A	52	Eagle	20 passive, 13 power_in, 10 input, 8 output, 1 no_connect	synthesiser (AERIS-10)

Every parts-list IC on the adapter itself now has a datasheet-sourced symbol. The two left on Eagle are AERIS-10 parts, used only as reference.

3. Where the data comes from

analog.com will not serve its PDFs to this machine: repeated 60 s timeouts, and the usual mirrors return 403 and 410. Two other sources filled the gap.

3.1 Manufacturer datasheets

Symbol	Datasheet	Table used	Obtained from
AD9484BCPZ-500	AD9484.pdf Rev. A	Table 7	AERIS-10 component folder
AD8352ACPZ	ad8352.pdf Rev. C	Table 4	AERIS-10 component folder
M3SWA2-34DR	M3SWA2-34DR+.pdf	Pad Description	AERIS-10 component folder
LTC5552	LTC5552f.pdf	Pin Configuration, Pin Functions	AERIS-10 component folder
AD9523BCPZ	AD9523.pdf Rev. D	Figure 2, Table 19	Internet Archive
AD9253BCPZ-125	AD9253.pdf Rev. D	Figure 9, Table 8	Internet Archive
AD9767ASTZ	AD9763_9765_9767.pdf Rev. G	Figure 5, Table 6	Internet Archive
ADCLK944BCPZ	ADCLK944.pdf Rev. 0	Figure 2, Table 6	Internet Archive
ADCLK948BCPZ	ADCLK948.pdf Rev. B	Figure 2, Table 7	Internet Archive
Si549_PinoutC	Si549.pdf Revision H (Skyworks)	Pin Assignments, Ordering Guide	Internet Archive

The Internet Archive route is `_work/fetch_datasheets.py`. The Wayback Machine keeps copies of analog.com's own URLs, and with the `id_` suffix it returns the archived bytes unmodified, so the file is what analog.com served on the snapshot date. Two traps, both handled by the script:

- **Downloads on this machine are cut at exactly 1 MiB, without an error.** A larger datasheet arrives truncated but still starts with `%PDF` and half-renders. So files are fetched in HTTP Range chunks, and completeness is checked at the **end**: a whole PDF ends in `%%EOF`.
- **The AD9767 has no datasheet of its own.** It is published jointly as `AD9763_9765_9767.pdf`, and the Archive has no copy of any `AD9767.pdf` URL.

The script prints the snapshot, size and SHA-256 of each file. The PDFs themselves are Analog Devices' copyright and are not in the repository (`_work/datasheets/` is git-ignored).

Every table was read from the rendered page, not from extracted text. Text extraction loses overbars (so `REFA` and `REFA`-bar come out identical) and shuffles table columns. That's a real risk on the AD9523, where 14 of its output pairs differ only by an overbar.

3.2 The AERIS-10 Eagle library, for the remaining two

Eagle records a direction per pin, which maps cleanly onto what KiCad needs:

```
in  -> input     out -> output    io  -> bidirectional    pwr -> power_in
sup -> power_out pas -> passive   oc  -> open_collector   hiz -> tri_state
nc  -> no_connect
```

Those boards were fabricated and measured, so a wrong pinout would have shown up as a dead board. Good evidence, but **second-hand**, and every symbol carries a `SymbolSource` property saying which route it came by.

4. Every datasheet table checked against a second source

A pin table typed by hand can be wrong in ways that stay invisible until the board is built: two pins swapped, a complement on the wrong side of a pair, a supply read as a signal. The defence is an independent second source, and `_work/crosscheck_pinouts.py` checks every datasheet symbol against one where it exists: the AERIS-10 Eagle library, the EasyEDA pin names collected in `_work/pinouts.txt` during the Rev01 work, or a pin-compatible part in KiCad's own

libraries (the Si549 in pinout code C against KiCad's Si570).

The ADCLK948 has no second source: it is in none of the three. The script lists it as such rather than skipping it. Its only check is internal: the datasheet's pin drawing (Figure 2) and pin table (Table 7) agree. That is why **CLOCK_SPEC.md** §5 puts its pin numbers first on the review list.

Symbols drawn on a sheet get a hand-arranged pin layout (`SYMBOL_LAYOUT` in `_work/make_symbols.py`): the ADCLK948, the Si549, the AD9484 and the AD8352 so far. Only the positions change. Pin numbers, names and types still come from the datasheet table, and the script aborts if a layout omits or repeats a pin. The AD8352's left side reads VIP, RGN, RGP, RDP, RDN, VIN so that each external part sits straight across its two pins (**ADC_RADAR_SPEC.md** §4).

```
symbol           2nd source  pins  agree  result
AD9484BCPZ-500   eagle        57     56  AGREE
AD8352ACPZ       eagle        17     16  AGREE
AD9523BCPZ       eagle        73     69  AGREE, 3 settled
M3SWA2-34DR      eagle        17     16  AGREE
LTC5552          eagle        13     11  AGREE, 2 settled
AD9253BCPZ-125   easyeda       49     43  AGREE, 5 settled
AD9767ASTZ       easyeda       48     48  AGREE
ADCLK944BCPZ     easyeda       17     16  AGREE
Si549_PinoutC    kicad          8      7  AGREE, 1 settled
ADCLK948BCPZ     -            33      -  NO SECOND SOURCE
No conflicts.
```

("agree" excludes the exposed pad, which each source names differently.)

Eleven disagreements were looked up and **settled against the datasheet**. They stay in the script's output with the reason, rather than being normalised away:

Symbol	Pad	Ours	Second source	Verdict
AD9523	55	`STATUS1/SP1`	`STATUS1/SPI`	Eagle typo: SP1 is I²C address bit 1
AD9523	69	`NC`	`VDD1.8_PLL2`	Eagle predates Rev. D, which calls it NC but allows 1.8 V "on existing designs". Typed `passive` so either passes ERC
AD9523	72	`PLL1_OUT`	`~PLL_OUT`	Eagle wrong twice: no overbar, and it is PLL**1**
LTC5552	3	`IF-`	`IF`	Eagle lost the superscript minus
LTC5552	EP	pad 13	n/a	Eagle has no exposed pad; the datasheet does
AD9253	37, 38, 47, 48	`VIN±B/C`	`VNI±B/C`	EasyEDA typo
AD9253	40	`RBIAS`	`RBAIS`	EasyEDA typo
Si549	6	`VDD`	`Vcc`	Naming only: KiCad's Si570 calls the supply Vcc

Every one of the disagreements was an error or a naming difference in the second source, not in the transcription. That's the result that makes the transcriptions trustworthy.

5. Errors this work found and fixed

5.1 Exposed pads were numbered to match the datasheet, not the footprint

The datasheets call the exposed paddle **pin 0**. KiCad's stock LFCSP/QFN footprints number it **N+1** (`QFN-56-1EP_8x8mm…` has pads 1–57). A symbol pin has to match a footprint pad, or `Update PCB from Schematic` leaves the paddle unconnected. On the AD9484 that pad is the ADC's **only analogue ground**.

The first build of `AD9484BCPZ-500` used "0". Every symbol now numbers the paddle N+1: 57 on the AD9484, 49 on the AD9253, 73 on the AD9523, 17 on the others. `make_symbols.py` refuses to write the library if a datasheet symbol's pads don't run 1…N without gaps.

5.2 The M3SWA2 was missing its paddle

Found by the cross-check: the Eagle part had 17 pads and ours 16. The datasheet's Pad Description says *"GND: 2, 4, 7, 9, 11, 14, 16* ***& Paddle****"*, and the package is *"DQ3005, exposed paddle"*. A 30 GHz switch with a floating main ground would not have worked. **Eagle was right**; the symbol now has pad 17.

The same review renamed the RF ports to the datasheet's `RFOUT1`/`RFOUT2`, and retyped the three NC pins as `passive`. They are *"not used internally, connected to ground on test board"*, so grounding them is the recommended practice and must not raise an ERC error.

5.3 An erratum in the LTC5552 datasheet

Its Pin Functions section lists pin 3 twice: in *"GND (Pins 1, 3, 4, 6, 8, 10, 12…)"* and in *"IF+, IF− (Pins 2, 3)"*. The Pin Configuration drawing shows pin 3 as IF−, and a differential IF needs it, so the GND list is the error. The symbol keeps IF− on pin 3 and the code says why, so that nobody "corrects" it back and grounds one side of the IF port.

5.4 B-03 had been closed wrongly

Retyping the `M3SWA2-34DR` from its datasheet showed that **blocker B-03 had been closed wrongly**. It had been closed on a web search snippet reporting *"supply voltage requirement is 3.3V ~ 3.6V"*, and the charge-pump inverter had been struck from the power tree on that basis. The datasheet requires **VDD +3.3 V* and *VEE −3.3 V; what is positive is the* control logic*. The rail is back; see **BLOCKERS_AND_RISKS.md** B-03.

5.5 The AD9253's DRVDD is 1.8 V

Not a symbol error, but found while reading the same table: the power budget had DRVDD on 3.3 V, above the part's 2.0 V absolute maximum. See **POWER_AND_STACKUP.md** §1.2.

6. What is still not done

`ADAR1000ACCZN` and `ADF4382A` remain Eagle-derived. Their types are plausible and complete, and both are AERIS-10 parts rather than ours, so they are usable as-is. Their datasheets are in the AERIS folder if they ever matter.

7. Validation performed

By KiCad, not by inspection:

```
kicad-cli sym upgrade      parses the library without error
kicad-cli sym export svg   renders all 18 symbols
kicad-cli sch erc          project ERC unchanged after rebuilding the library
```

Plus, in `_work/make_symbols.py`, duplicate-pad detection and pad-sequence completeness. And the second-source comparison of §4, in `_work/crosscheck_pinouts.py`.

Part IV: 8-Layer PCB Layout & Signal/Power Integrity

4 technical document(s)

Source: docs/LAYOUT.md

Layout: board, rules, placement and routing

25 September 2026 · `KV260-IAS2RF.kicad_pcb` · built by `_work/layout/build_board.py` from the schematic's netlist; placement refined and L4 drawn the same day

The Rev03 board exists. It has:

- the outline and the 8-layer stackup (6 layers until 12 November 2026, §6.5);
- design rules and net classes;
- the two ground planes and the split power layer;
- **every one of the 479 parts with its nets**, linked to its symbol (472 until the housekeeping devices were added on 2 October; 771 footprints since Rev08, §6.7);
- the holes and fiducials;
- a placement with every passive at its pin, and a readable silkscreen.

It is fully routed (§6): 0 DRC errors, 0 unrouted connections, 0 schematic-parity problems. The LVDS skew and termination stubs were reviewed and fixed, and the trace widths confirmed in JLCPCB's calculator, on 10 November (§6.2–6.3). **On 11 November an RF/high-speed review** rebuilt the RF band, widened the LVDS legs to 50 Ω, fixed VCCINT's plane and decoupling, and added return vias, exposed-pad vias and an edge fence (§6.4, **SIGNAL_INTEGRITY.md**). **On 12 November it moved to 8 layers** (JLC08161H-2116C): two inner signal layers, L4 for power only, the LVDS pairs re-routed (9 of 19 as coupled 100 Ω pairs, the rest as matched 50 Ω legs), their terminations moved under the FPGA's balls on the bottom face, and LINK_TX terminated at its receiver (§6.5).

The original Allied Vision board is kept, untouched, as `_deprecated/CSI2-KRIA-KV260_Rev01_AlliedVision.kicad_pcb` in the tags up to `rev08` (`git checkout rev08 -- _deprecated`); the Allied Vision Altium sources stay in `PCB/`.

1. Outline: 119 × 132 mm

Kept from the original	The upper, U-shaped part: the two tongues that reach the IAS connectors, and the band over the carrier down to its edge (y 117.25). It is known to clear every part on the KV260 (INTERFACE_SPEC §5.3)
Changed	The IAS0 tongue's right edge moves from x 144.9 to **142.4**, 1.5 mm clear of the carrier's J18 jumper. The original overlapped it by 1.0 mm (INTERFACE_SPEC §5.3)
Removed	The slots for the cameras' flat cables along the old bottom edge
New	Everything from y 127.25 to **y 214.75**, full width. Outward, off the carrier, where the KV260 has nothing at all
Tab (13 Nov 2026)	x 208–229, y 117.5–136 on the east edge, for the Ethernet RJ45 J1201 (CONTROL_SPEC §7). It is off the carrier (y > 117.25) and past its front edge, where INTERFACE_SPEC §5.3 found 25+ mm free. The bounding box becomes **140 × 132 mm**. The GND planes follow the tab

Why 120 mm and not the ~90 estimated before the schematic existed. The parts' courtyards add up to **5,700 mm²**. At 119 × 90 mm they would cover 75 % of a board that is populated on one face only, with nothing left to route between them. At 119 × 120 mm they cover about half. **On 10 October it grew 12 mm more, to 132 mm**, to give the routing room. The overhang past the carrier's edge is now 97 mm, which is why three supports are added at the outer edge.

One face only, and no through-hole parts over the carrier. Below the board there is 0.8 mm to the carrier (the Hirose mated height), so nothing can go on the bottom there, and through-hole pins would hit it. The placement enforces it: no through-hole part above y 118.5. The carrier's edge is drawn on `Dwgs.User`.

2. What is fixed by measurement

Item	Where	Source
J101 (IAS1, the link) and **J102** (IAS0, mechanical)	(186.02, 85.60) and (135.98, 85.60), bottom face, 180°	Copied from the original board: position, face, rotation and pads, checked identical by script. They register the adapter on the KV260
H1, H2, M3 through the KV260's corner holes	(94.0, 112.25), (203.0, 112.25)	The original's holes, within 5 µm of the carrier's (INTERFACE_SPEC §5.3)
H3, H4, H5, supports	(93.0, 209.75), (148.5, 192.5), (204.0, 209.75)	8 mm M3 standoffs to the surface the KV260 stands on (INTERFACE_SPEC §5.3: 7.9 mm)

All five holes are plated and on GND. H3–H5, the fiducials and the holes are *board-only* footprints: they have no symbol. FID1–FID3 are on the top face; FID4–FID6, added on 13 Nov, on the bottom face at (104, 119), (100, 190) and (201, 196) for that face's assembly pass.

Test pads (13 Nov). TP1–TP13 are bare 1.0 mm pads on the top face, board-only as the holes (project footprint `TestPad_D1.0mm_BoardOnly`, the name on F.Fab, no silkscreen), each on a via of its rail or joined to one by a short track:

Pad	Net	At	Pad	Net	At
TP1	+5V0	(174.3, 177.05)	TP8	+1V0	(116.9, 172.6)
TP2	+3V3_D	(151.65, 129.59)	TP9	−3V3	(98.4, 203.8)
TP3	+3V3_A	(128.90, 127.00)	TP10	+3V3_CLK	(184.1, 146.8)
TP4	+2V5	(110.02, 154.53)	TP11	DONE	(138.90, 160.78)
TP5	+1V8_D	(179.87, 184.93)	TP12	GND	(203.5, 182.8)
TP6	+1V8_A	(187.4, 188.8)	TP13	GND	(170.25, 199.75)
TP7	+1V2	(171.99, 130.11)			

+12V has none: J1001's pins and D1001 are reachable.

3. Stackup and rules

The stackup is **JLCPCB's JLC08161H-2116C**: 8 layers, 1.54 mm (6 layers, JLC06161H-2116A, until 12 November 2026: §6.5). Same outer prepreg as before, so the outer 50 Ω width stands.

Layer	Use	Dielectric below
L1 F.Cu	SIG: RF lines, fan-outs, part of the LVDS	2116 prepreg 0.1194 mm, Er 4.29
L2 In1.Cu	**GND plane**	core 0.130, Er 4.17
L3 In2.Cu	SIG: LVDS pairs (LINK, ADCR), slow nets	2116 + 1080 + 2116 prepreg 0.3658, Er 4.29
L4 In3.Cu	**PWR, split** (§3.1); no signal tracks	core 0.130, Er 4.17
L5 In4.Cu	**GND plane** (new)	prepreg 0.3658, Er 4.29
L6 In5.Cu	SIG: LVDS pairs (ADCR, ADCS, LINK_RX_CLK), between two GND planes	core 0.130, Er 4.17
L7 In6.Cu	**GND plane**	2116 prepreg 0.1194, Er 4.29
L8 B.Cu	SIG: slow nets, the 100 Ω terminations under the FPGA, VCCINT caps	none

The rules in the project file are for a standard 8-layer process, with a 0.2 mm drill for fanning out the 1.0 mm-pitch BGA:

Rule	Value
Track / clearance	0.09 mm minimum (the LVDS necks under the FPGA); Default class 0.15 mm track, **0.10 mm clearance**
Via	0.45 mm pad, 0.2 mm drill
Copper to edge	0.3 mm
Zones on L2, L4, L5, L7	0.15 mm clearance; L4 kept 1 mm in from the edge
Custom rules (`KV260-IAS2RF.kicad_dru`)	An RF50 track under 0.18 mm (the 0.15 mm neck at a 0.5 mm-pitch pin) keeps the default clearance; the ESD tuning sections keep 0.24 mm; an LVDS pair's two legs keep 0.10 mm to each other, and inside the FPGA's courtyard an LVDS track keeps 0.10 mm to everything but supply copper (the Power class's 0.15 mm holds: KiCad takes the larger of the two items' rules, so the rules are written for both orders)

Net class	Track	Applies to (patterns in the project file)
LVDS100	Coupled: 0.10 mm, gap 0.15 mm (100.2 Ω on L3/L6), necked to 0.09 / 0.12 mm under the FPGA (98.5 Ω); on L1 0.117 / 0.15. Legs that run apart are 50 Ω each: 0.151 mm on L3/L6, 0.183 mm on L1/L8	Link pairs, ADC data and clock pairs, `CLK_ADC*`, `CLK_FPGA`, `FPGA_CLK`
RF50	0.183 mm (50.4 Ω on L1), 0.2 mm clearance	`IF_RX_*`, `IF_TX_*`, the auto-named switch/SMA nets `Net-(J4*-In)`, `Net-(J9*-In)`, `Net-(U90*-RFOUT*)` and U401's `CLK0`/`Q3`
Power	0.4 mm, 0.15 mm clearance	Every rail, VIN and switch nodes
Default	0.15 mm (0.10 mm in the dense areas), 0.10 mm clearance	The rest

The impedance widths come from a field solver run on this stack, solder mask included (`_work/field_solver8.py`; `_work/field_solver.py` for the 6-layer stack and the solver's checks against exact references, within 1–2.4 %). Order stack

JLC08161H-2116C explicitly (**FABRICATION.md**): 2116A and 2116B were looked at and dropped (the field solver's docstring says why).

3.1 L4, the power layer

+3V3_D is the background plane, over the whole board: it has the most pins (62) and they are everywhere. On top of it, islands at higher priority, 0.3 mm apart, each drawn around its own rail's pads so they follow the placement:

Island	Where	Why a plane
+1V0	Under the BGA, south and west of it under VCCINT's 0.47 µF caps (11 Nov), and a corridor from the buck's inductor L1030 (five vias in its pad)	FPGA VCCINT, 700 mA, the highest current per pin
+5V0	The POWER block	The input of the three bucks and two LDOs: 1.6 A
+3V3_CLK	The CLOCK block	The ADCLK948 and Si549, isolated from the digital 3.3 V
+5V_IFR, +5V_IFS	Around each pair of AD8352 drivers	The drivers' supplies
+1V8_ADCR_A/D, +1V8_ADCS_A/D	Around each ADC	Their analogue and digital supplies, kept apart

Where two islands overlap, the smaller wins. **Everything else is routed as tracks**: +1V8_D, +2V5 (a 0.5 mm trunk where it fits, since 12 Nov), +3V3_A, +1V8_A, +12V, −3V3, +1V2 and the XADC supply. They are either low current or have too few pins in one place for a plane to be worth it.

- **L3 references L2**, 0.13 mm away, far more than L4, 0.37 mm away, so the splits on L4 matter little to L3's signals. **L6 sits between L5 and L7**, both ground. Since 12 Nov L4 carries no signal track, only a few supply stubs.
- The islands are fed by their pads' vias since the routing (§6).

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4. Placement

Anchored by hand:

- **the 12 SMAs**, along the bottom edge at 8.5 mm pitch, **ordered by where each signal comes from**. Left to right:
- TX_A (J931/J932) and TX_B (J941/J942), under the DACs;
- SDR_TX_C (J952) and SDR_RX_C (J951);
- RX_A (J911/J912) and RX_B (J921/J922), under the ADCs;
- the clock in/out (J401/J402) at the right end, nearest the ADCLK948.
- **the DC jack**, opening at the left edge;
- **the AERIS ribbon** (IDC 2×20), in a band under CONTROL, above the RF row. It was along the top of the main area until 10 October; from there its 35 bank-35 lines crossed both DAC buses;
- **the AD9767's five series arrays** (RN1103–RN1107), in a column left of the BGA, on the way to U801. Placed by rule they sat above the BGA, and the DAC lines doubled back;
- **the Pmod and JTAG headers**;
- **the FPGA**, rotated 90°, so bank 15 faces the DACs and bank 14 faces the ADCs and J101. **A 3.5 mm ring around it is kept free of parts** (2.5 mm until 19 Oct), so the outer rows can escape on L1 and the inner rows' fan-out vias have room.
- **the POWER block, along the flow of the power** (below);
- **the FPGA's VCCINT bulk** (330 µF, 100 µF and 3 × 4.7 µF), right after its ring, from the +1V0 ball nearest the edge outward. Those balls are in the middle of the BGA, so about 11 mm is the least these can be; they land at 10.7–12.4 mm. UG483 p.24: *"Bulk capacitors can be placed almost anywhere on the PCB, but the best placement is as close as possible to the FPGA."*

The POWER block follows the flow of the power (POWER_SPEC §1), from the jack's pin 1:

- **Input chain, going up from the jack:** PTC F1001 at the jack's VIN, MOSFET Q1001 above it (drain down, sources up), then the LMR33630 with its inductor L1001 to its left. The switch pin faces the inductor, and the input pins face the MOSFET.
- **+5V0 feeds three buck cells in a row below the jack:** chip, inductor below, output capacitors under the inductor. +1V0 is on the right, nearest the FPGA, where its L4 corridor starts.
- **A column of LDOs on the block's right edge:** +3V3_A at the top, next to the DACs, then +1V8_D, then +1V8_A.

- **The −3V3 charge pump at the bottom,** towards the RF switches that use it.

Each chip's orientation is chosen from its pad map. Every capacitor, inductor and resistor on POWER ends up within 5.9 mm of its pin.

Every other chip goes to its sheet's region, at the relative position it has on its schematic sheet, scaled down:

Region	Sheet
Left	POWER, beside the jack
Centre-left	DAC_RADAR, DAC_SDR
Centre	CONTROL, around the FPGA
Right	CLOCK, ADC_RADAR, ADC_SDR (each ADC next to the FPGA, its front end outboard, since 14 October)
Top-right tongue	IAS_LINK, beside J101
Bottom band	ROUTING. Each RF switch sits right above its own pair of SMAs

Every passive goes next to the pin it belongs to. The script finds that pin from the netlist:

- a decoupling capacitor goes to the supply pin it decouples. Which chip that is, in this order:
- the chip its spec description names ("ADCLK948 p.10: 1 µF bypass", "… at the Si549's VDD");
- the chip whose pin it is drawn next to (under 15 mm on the sheet);
- otherwise, the chip with the most pins on that rail. That is how CONTROL's decoupling block reaches the FPGA, and between two identical chips (the AD8352 pairs) the capacitors are shared out;
- a termination, series resistor, coupling or reference capacitor goes to the pin it connects to. Only chips and connectors on the passive's **own** sheet count: a termination belongs at the receiver on its own sheet, and a 22 Ω series array at the FPGA, which drives it;
- on POWER:
- a buck's inductor goes to its switch pin, first;
- its output capacitors go to the inductor;
- every regulator capacitor, whatever its value, comes before anything else, because the input and output capacitors close the switcher's high-current loop.
- a pull-up or pull-down (≥ 1 kΩ to a rail, outside POWER) goes last: it is DC and can be a few mm further out.

The order is the one a person would follow: a chip, then at once its own passives (small decoupling first), then the next chip. So each chip's pins get their neighbourhood before a neighbour can take it. A legaliser puts each part at the nearest spot where its courtyard, grown to include its own silkscreen, is free, **0.5 mm from every other** (0.2 mm until 10 October, which left no room for tracks between the passives). The spot must be inside the outline, and off the carrier if the part is through-hole.

The silkscreen gets a reference for every part where one fits:

- clear of every pad, of other silk and of other parts' bodies;
- at 1.0 mm, or at the 0.8 mm minimum;
- beside the part, or up to 3 mm away for chips, connectors and inductors.

155 references fit. The other 332 are hidden on the silkscreen, but every one stays on F.Fab, the assembly drawing. Most of them are 0402 passives in dense groups. The Hirose connectors' silkscreen is moved to B.Fab: its 0.5 mm text is below the minimum, its outline runs over its own pads, and it sits mated to the carrier where nobody can read it.

This is a placement to route from, not a finished layout. Expect to move parts in KiCad as the routing is planned.

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5. How it was checked

The figures below are for the first placement (0.2 mm between courtyards, 25 September); the re-placement of 7–19 October moved parts by up to a few millimetres.

Check	Result
`kicad-cli pcb drc --schematic-parity`	**0 parity problems**: every symbol has its footprint, every pad its net. **No shorts, clearance or courtyard violations**
	Before routing, **499 unconnected** listed: a cap on KiCad's list, not the count (the netlist needs about 1,390 connections). No silkscreen warnings. After routing: §6.1

Check	Result
`_work/layout/check_placement.py`: each passive's distance to its pin, from the board file	Decoupling ≤ 1 µF: median **2.9 mm** (first pass: 10 mm). Parts on a signal pin: median 3.4 mm, 90 % within 7.0 mm. Bulk: median 8.6 mm, none over 14 mm. On POWER, everything within 5.9 mm of its pin. The FPGA's 0.47 µF sit further out (median 8.9 mm): VCCINT is in the middle of the BGA and nothing may enter the 2.5 mm escape ring on the top (four more, C1184–C1187, sit on the bottom face inside the footprint on ball vias since 11 Nov). The script's pad positions are checked against the coordinates KiCad prints in its DRC report: 964 pads, 0 µm apart
L4 filled on a copy (`kicad-cli pcb drc --refill-zones`)	All islands fill. The only new reports are the islands' `isolated_copper`, expected until their vias are placed
J101/J102 against the original board	Position, face, rotation and all 38 pads identical. Nets as INTERFACE_SPEC §3–§4 (pin 4/5 `LINK_RX_D0`, 7/8 `LINK_RX_CLK`, 14 `HK_SCL`, 21 `FPGA_PROG_B`, 22 `HK_SDA`, 15 `FPGA_IRQ`: moved from 32 after the check against the carrier, INTERFACE_SPEC §4.3)
Footprints	All 479 exist. Four are new, in `footprints/kv260-ias2rf.pretty` (`_work/make_footprints.py`): ADCLK948 and AD9484 LFCSPs with their datasheets' exposed pads, the M3SWA2's DQ3005 from its Mini-Circuits case drawing, and the Hirose BM20B
TPS7A8300 (U1005–U1007) against TI's RGR0020A drawings (SBVS197, pp. 44–45)	KiCad's `QFN-20-1EP_3.5x3.5mm_P0.5mm_EP2x2mm` fits: 3.5 mm body, pin 1 top-left and the same pin order. Its exposed pad is 2.0 mm against TI's 2.05 mm land, still 0.25 mm clear of the pins. TI's example puts four 0.2 mm vias in the pad: added on 11 Nov (four in each), for the +1V8_D LDO's 0.50 W

Parts chosen for this step, each checked against its datasheet (all fetched by `_work/fetch_datasheets.py`):

Part	Choice	Why
T701, T801, T802	**Mini-Circuits ADT2-1T+**, CD542	Impedance ratio 2, 0.4–450 MHz, 50 Ω. The 100 Ω secondary (6/4) goes to the DAC, the primary (3/1) to the line. KiCad's PL-052 variant of the footprint grounds pin 4, which a balun must not, so the plain CD542 pads are used
L1001	Bourns SRP7028A-8R2M	Isat 7.5 A ≥ the LMR33630's 5.05 A current limit; Irms 4 A
L1010, L1020, L1030	Bourns SRP7028A-3R3M, -3R3M, -2R2M	Isat 12 / 12 / 14 A ≥ 3.5 A
Q1001	Diodes DMT10H015LFG (was DMP3013SFV)	100 V N-FET, back to back with Q1003 under LM74502-Q1 U1009: **POWER_SPEC.md** §1.1

6. Routing

6.1 The routed board (10 November 2026)

Result	**0 DRC errors, 0 unrouted connections, 0 schematic-parity problems** (zones refilled); re-checked after the review of 11 Nov (§6.4)
Copper	12.5 m of track (12 Nov): L1 4.9 m, L3 3.3 m, L6 1.2 m, L8 3.0 m, L4 0.1 m (supply stubs). Mostly 0.10 mm; the supplies 0.30 mm (+2V5 up to 0.5); the RF lines 0.183 mm; LVDS as §3
Vias	2,089 through vias, 0.45 mm on a 0.20 mm drill; 993 are ground (return vias, the RF band fence, the edge fence, exposed pads). About 590 sit in pads and are filled and capped (FABRICATION.md)
L2, L5, L7	Ground only (`_work/layout/planechk.py`)
L4	No signal tracks since 12 Nov; three supply stubs under the BGA
LVDS	9 of 19 pairs coupled end to end (0.10/0.15 mm on L3/L6), ADCR_D4 for 41 %; the others as two 50 Ω legs matched to ±5 ps. Every pair's 100 Ω termination sits on its two ball vias on the bottom face (§6.5)

6.2 What is left

1. **LVDS skew and termination stubs: fixed 10 Nov (§6.3).** LINK_RX_D0 and LINK_RX_D1 were half a bit apart; every pair at 1 Gb/s is now within 42 ps. Four terminations (R1109, R1111, R1112, R1113) moved next to the FPGA, where their pairs pass, and R514 turned round, so no leg at 1 Gb/s has a stub over 27 ps. What is left is in §6.3 and is tolerable.
2. **No supply track on L2 or L5** after any further routing: check with `_work/layout/planechk.py`.
3. **The LVDS pairs: re-routed as pairs on 12 Nov (§6.5).** Ten pairs could not be coupled; a LINK_RX's bank 34 is in the BGA's south-east corner; coupling it needs its AC capacitors at J101 moved together (§6.6).
4. **No dangling copper** after any rip-up: the DRC's `track_dangling` and `via_dangling` at zero.
5. **Check the planes** after a refill: every L4 island fed by vias, L2 unbroken under the pairs, and the tracks on L4 (the +3V3_D background only) not cutting off any +3V3_D via.

Before anything is ordered: DRC with zero errors and zero unconnected items, the widths confirmed in JLCPCB's

calculator, and the checks in **FABRICATION.md**.

```
py _work/layout/build_board.py       # rebuilds the board: overwrites any hand placement
kicad-cli pcb drc --schematic-parity -o drc.rpt KV260-IAS2RF.kicad_pcb
py _work/layout/check_placement.py drc.rpt   # passives' distance to their pins
py _work/fab/make_fab.py                     # Gerbers, drill, BOM, CPL into fab/ (docs/FABRICATION.md)
```

The board is routed: do not run `build_board.py` again. It would rebuild the board and drop every track. From then on the board file is the source, as the drawn sheets are once accepted.

6.3 LVDS skew review (10 Nov)

`_work/layout/lvds_skew.py board` follows each leg from the driver's pin to the receiver's, across the AC caps (LINK_ *and* *J_LINK*_), the series resistors (CLK_FPGA, FPGA_CLK) and U401's outputs before their caps. A leg's delay is that of the shortest copper path between the two chip pins, at 6.0 ps/mm on L1/L6 and 6.9 ps/mm on L3/L4 (POWER_AND_STACKUP §2.5). Copper off that path is a **stub**, reported apart: usually the branch to a termination resistor that the leg does not pass through. Rates: LINK ≤ 1 Gb/s a lane (INTERFACE_SPEC §3, 1 ns a bit), ADCS 1 Gb/s a lane (AD9253 one-lane, 62.5 MSPS × 16), ADCR 400 MSPS.

What was fixed. The first review (da14df5) summed all of a net's copper. Measured as paths, that board had:

Pair	P − N then	Cause	Now	Fix
LINK_RX_D1	+517 ps	P went round the board's right edge (207 mm)	−16 ps	Both legs re-routed (144 / 148 mm)
LINK_RX_D0	−478 ps	N looped down to y 190 and back (187 mm)	+4 ps	N re-routed (52 mm in the middle); P meandered by 15 mm on L1
ADCS_D1	+152 ps	N short	+42 ps	N meandered by 18 mm (as far as the room goes)
CLK_FPGA	−111 ps	P short	−13 ps	P meandered by 16 mm
CLK_ADCR	−74 ps	P short	−42 ps	P meandered by 6 mm; two of its bumps touched and shorted 4 mm out, now apart; no more room
ADCS_DCO	−93 ps	P short	−27 ps	P meandered by 13 mm
CLK_ADCS	+54 ps	N short	0 ps	N meandered by 9 mm
ADCS_FCO	−11 ps	No skew, but a **55 mm stub** on N to R1114 (346 ps)	−27 ps, stubs 3 / 5 ps	N re-routed through R1114's pad (fly-by), as P was; P meandered by 11 mm

The re-routes and meanders were checked against every clearance, then by the DRC (§6.1). The meanders are rectangular bumps of 0.5 mm, 0.5 mm apart, 0.5–1.5 mm high, on L1/L6 and in clear space only.

The board now:

Pair	P − N ps	Stub P / N ps	Verdict
LINK_RX_D0, D1, LINK_TX_D0, ADCS_D0, ADCS_DCO, ADCS_FCO, CLK_ADCS, CLK_FPGA, ADCR_D1, ADCR_DCO	−27 to +33	≤ 27, but CLK_ADCS N 45 (a bias resistor, below)	Fine
ADCS_D1	+42	22 / 2	Tolerable: 0.04 bit; no more room for meanders on N
LINK_TX_CLK	−36	≤ 19	Fine
LINK_RX_CLK	−60 → **0** (11 Nov: 10 mm of meander on P)	≤ 3	Fixed
CLK_ADCR	−42	11 / 57 (a bias resistor, below)	Tolerable: the 400 MHz sample clock; no more room to meander P
ADCR data and OR	−86 to +64	up to 52	Tolerable at 400 Mb/s (2.5 ns a bit)

What a P−N skew does: the two legs switch apart, so the differential voltage sits at zero for the skew time at every edge; that much of each bit is lost and cannot be tuned out at the receiver (IDELAY moves the pair, not one leg). Under 50 ps is 0.05 bit at 1 Gb/s.

Termination stubs: fixed 10 Nov. A 100 Ω termination sits across each pair the FPGA receives (R1101–R1116, CONTROL_SPEC §3, no DIFF_TERM in a 3.3 V bank), and one across each ADC clock at the ADC (R514, R642). What matters is the copper between the termination and the receiver's pin: it is an unterminated stub, as is a branch from the leg to a resistor the leg does not pass through. At 1 Gb/s with edges of about 300 ps, up to about 8 mm (50 ps) is harmless;

longer rounds the edges. `lvds_skew.py --stubs PS` lists every branch longer than PS and where it goes.

Pair	Was: stub P / N; termination to pin P / N (ps)	Now	Change
ADCS_DCO	134 / 73; 182 / 110	9 / 27; 57 / 64	R1113 moved from 10 mm out to where the legs part, 6 mm from the FPGA; old branches removed
ADCR_DCO	34 / 79; 88 / 149	0 / 12; 53 / 61	R1109 moved onto P's via, 6 mm from the FPGA; N joined by a 2 mm stub
ADCS_D0	13 / 66; 83 / 104	7 / 7; 36 / 31	R1111 moved between the legs, 5 mm from the FPGA
ADCS_D1	2 / 56; 112 / 125	22 / 2; 73 / 47	R1112 moved onto N's via, 6 mm from the FPGA; P joined by a 3 mm stub
CLK_ADCR	N 54 to R514; N 132	none; N 31	R514 turned 180°, so each leg meets its own pad on the way to its ADC pin; N passes through its pad

Left as it is:

- **U401's LVPECL pull-downs** R405 (CLK_ADCR N, 9 mm branch) and R407 (CLK_ADCS N, 7 mm): 200 Ω to ground, a weak tap; no free spot within 4 mm of the driver.
- **ADCR_D0 N and ADCR_D7 N**, 8 mm branches at 400 Mb/s; no free spot nearer the FPGA.
- **ADCS_FCO N** passes through R1114, which sits 141 ps (about 23 mm of route) from its FPGA pin; the area by the FPGA has no room for it. FCO is the frame clock, one edge per sample.

Data to clock, by mean leg delay (ps): LINK_RX_D0 +79 and LINK_RX_D1 +207 against LINK_RX_CLK; LINK_TX_D0 +2; ADCS_D0 −73, ADCS_D1 −17, ADCS_FCO +45 against ADCS_DCO; ADCR data −16 to −80 against ADCR_DCO. The ADC buses land on the XC7A50T's IDELAYE2 (78 ps taps, 2.5 ns range), so those are calibrated per lane at start-up. LINK_RX lands on the K26 (IDELAYE3), which can deskew too, but only if the Kria firmware trains each lane; the KV260's own trace lengths add to this and are not known here.

Not coupled: no pair runs as a coupled pair (0–3 % of the P leg within 0.35 mm of N, CLK_ADCR 12 %). Each leg is a 0.10 mm track on its own: 64 Ω on L1/L6, 62 Ω on L3 by the field solver (POWER_AND_STACKUP §2.6), so about 125 Ω between the legs against the 100 Ω termination (some reflection; less rejection of noise picked up on the way). Many legs also cross L4 (In3.Cu, the power layer). Acceptable for a first board at these rates; a pair-routed version is the better board. **Since 11 Nov the legs are 50 Ω** where they run apart (§6.4): the pair is about 100 Ω by leg width, and the eye simulates as an ideal pair's.

6.4 RF and high-speed review (11 Nov)

The full record, with the simulations, is **SIGNAL_INTEGRITY.md**. In short:

Area	Change
RF band	Rebuilt by hand: straight 183 µm switch → DC block → SMA legs on L1, bias parts on the bottom, four vias in each switch pad, L1/L6 ground pours with a 226-via fence, three vias per SMA ground leg, L2–L4 cut out under each SMA signal pad (openEMS: return loss 13.5 → 24.5 dB at 1 GHz)
RF lines	The eight long lines 183 µm end to end, ≤ 2 vias each, two ground vias at every via; the 64.9 Ω terminations moved under their caps (7–10 mm stubs gone); U401's input and output lines separated (−19.5 → about −45 dB)
LVDS	Legs widened to 50 Ω (74 % of the length at 0.175–0.183 mm); LINK_RX_CLK skew −60 → 0 ps; LINK_RX_CLK_P and LINK_RX_D0_P pulled apart (−18 → −46 dB); 136 return vias at layer changes (one layer change left with its ground via beyond 3 mm); legs of different pairs moved apart where there was room (SIGNAL_INTEGRITY §3.5)
PDN	Zone clearance 0.3 → 0.15 mm on L2/L4/L5; the +1V0 island joined to its corridor and extended under its caps; five vias in L1030's pad; four 0.47 µF (C1184–C1187) on the bottom face under the BGA, on ball vias; VCCINT under its target to 100 MHz (over it from 26 MHz before; `SIGNAL_INTEGRITY.md` §4.3)
Pads and edge	Via grids in every exposed pad (LMR33630, TPS7A8300 ×3, AD8352 ×4, ADCs, ADCLK948); a 176-via ground fence round the edge; L4 pulled back 1 mm from the edge
ESD	PESD5V0F1BL (D961–D970, D401, D402) on the SMA lines 2.15 mm from each SMA pad, ground pad on its own via, tuned out by 0.1 mm line sections either side (0.76 mm before, 1.4 mm after; openEMS −39 dB at 500 MHz); TPD4E05U06DQAR arrays U1108/U1109 above the Pmod and U1110 beside JTAG, GND vias butted to their ground pins (SIGNAL_INTEGRITY §7.1)

6.5 Eight layers (12 Nov)

The board moved from JLC06161H-2116A to JLC08161H-2116C and the LVDS were redone. The full comparison with the 6-layer board, with the simulations, is SIGNAL_INTEGRITY §8. What changed:

Area	Change
Stack	L5 GND and L6 SIG added; the old L4's signal tracks moved to L6; SMA launch cut-outs extended to L2–L6, so the pad references L7 at the same depth as it referenced L5
Terminations	R1101–R1114 and the new R105/R106 on the bottom face, each 0402 straddling its pair's two ball vias (via in pad): no stub between the termination and the receiver
LINK_TX	Terminated at the FPGA by R105/R106 (100 Ω); R101–R104 become 10 k bias to +1V2. Before, 2 × 49.9 Ω at the connector left the receiver 45 mm down an open line
LVDS routing	Pairs ripped and re-routed by a negotiated-congestion pair router: 9 of 19 coupled; the rest completed single-ended, widened to 50 Ω and matched to ±5 ps (worst |P−N| 9 ps, was 84)
Return vias	0 of 89 reference-changing vias without a GND via within 3 mm (was 1 of 186)
+2V5	The trunk widened to 0.5 mm where it fits: 122–129 mV drop at 601 mA (173–185 before)
Left open	ADCR data to DCO −28 to −177 ps (DCO is 51 mm, the data 27–44 mm): calibrated per bit by IDELAYE2, as before; done 12 Nov (§6.6)

DRC on 12 Nov: 0 violations of any kind, 0 unconnected, 0 schematic-parity problems (zones refilled).

6.6 DCO and CLK_ADCR skew (12 Nov)

Item	Before	Change	After
ADCR_DCO	51.6 mm, data − DCO −177 to −28 ps	The AD9484 has DCO's P pin west of N, so the coupled pair from the FPGA arrived crossed and went round the chip. Its legs are swapped at the FPGA instead (N14 = DCO_N, P14 = DCO_P; `INVERTED` in `control_spec.py`, the gateware inverts the clock) and R1109 turned 180°. Re-routed: the old L3 escape to a via pair, L6 to above the AD9484, a coupled drop to its pins	38.9 mm, 89 % coupled, P−N +2 ps; data − DCO −90 to +5 ps
CLK_ADCR	P−N −44 ps: C414 and C415 were 10 mm apart, N 16 mm longer	C414/C415 placed side by side (vertical, 1 mm pitch) next to U401; the pair coupled from the capacitors to R514; 1.5 mm meander on P (L3) between U401 and C414	P−N −3 ps
LINK_RX	South-east balls, legs matched	Moving the pairs to bank 34's outer balls (R2/R1, T4/T3, R3/T2) was tried and dropped: the router completed 3 of 6 legs, T2 and R2 have no free spot for a via on any layer, and T4/T3's vias land on ADCS_D1. Coupling would need the AC capacitors (C101–C106, up to 9 mm apart) moved together first	Unchanged

DRC on 12 Nov: 0 violations, 0 unconnected, 0 schematic-parity problems. Eyes, PDN, return vias unchanged (mean eye loss −8 mV, worst LINK_RX_D0 −52 mV; 0 of 95 layer changes without a GND via within 3 mm); other pairs' legs within 0.25 mm 65.8 mm (was 69.3).

6.7 The board as of Rev08 (17 November 2026)

Since §6.6 the board grew twice, and every check above was re-run on the final file:

Change	Where it is described
Rev06 (13–14 Nov): the Ethernet tab on the east edge (bounding box **140 × 132 mm**, §1), the PHY on its own FPGA pins, the fan header	CONTROL_SPEC §7, POWER_SPEC
Rev07 (15 Nov): the 30 MHz anti-alias low-pass on `J951`'s line	ROUTING_SPEC §1.1, SIGNAL_INTEGRITY §9.9
Rev08 (16 Nov): the `RX_VU` front end in two shield frames, `J961` on the back wall, the `STATUS` LEDs and the debug USB-C on the IAS0 tongue, `J103` over `J102`: 183 footprints (588 to 771), 2,631 mm of track, 336 vias	REV08_PLAN §11.6, SIGNAL_INTEGRITY §9.10

The final board: 771 footprints, 13,479 track segments and 5 arcs, 2,562 vias, 765 of them inside an SMD pad. `make_fab.py` on 17 November: DRC with the zones refilled and schematic parity, **0 violations, 0 unconnected pads, 0 footprint errors**. `lvds_skew.py` gives the same delay, skew, stub and coupling for all 29 pairs as `_work/sim/lvds_skew_8layer.json` (§6.6 and SIGNAL_INTEGRITY §8), field for field: Rev08 moved no LVDS copper. Every part, connector and LED with its use is in the **board manual**.

6.8 Before the tag (18 November 2026)

Three changes, made on the routed board and checked like the rest.

Skew. Three pairs had a short leg that the others did not: `CLK_ADCS` (+23.4 ps), `ETH_MDI2` (+17.7 ps) and `CLK_FPGA` (−41 ps, left out of the old figure). Each short leg gained rectangular bumps on one straight stretch, on the side away from its partner (`meander.py`):

Pair	Leg, layer, stretch	Added	P − N before	P − N now
CLK_ADCS	N, L6 (In5), x 193.4, y 155.4 to 159.0	3.4 mm in 2 bumps	+23.4 ps	−0.1 ps
ETH_MDI2	N, L6 (In5), y 128.4, x 206.0 to 210.6	2.6 mm in 2 bumps	+17.7 ps	−0.2 ps
CLK_FPGA	P, L3 (In2), y 136.6, x 175.7 to 184.1	5.9 mm in 3 bumps	−41.4 ps	−0.7 ps

All 28 pairs are now within ±9 ps (**figure**, `_work/sim/lvds_skew_8layer.json`).

`J1501` is now surface mount throughout. The maker's drawing of the HX-TYPE-C 16P 180 LT H10.0 shows four through-hole shell legs reaching 2.1 mm below its seat, and two pegs on a diagonal; the land pattern had neither, and on the IAS0 tongue, 0.8 mm above the carrier, the legs would have reached it. It is now the HRO TYPE-C-31-E-17 (LCSC C7424785), surface-mount contacts and shell tabs, plastic pegs 0.7 mm long, 6.0 mm tall, sealed to IPX5 (`_work/rev08_final_footprints.py`). Its 0.5 mm contacts were routed again by hand:

- `VBUS` crosses between the two rows on the lines of A9/B4 and A4/B9, with a via in the gap on each.
- B5, B6 and B7 leave east. `USB_CC2` goes on the top to `R1532`; `USB_DP` and `USB_DN` go through vias and L3 to `U1503`, under `+3V3_USB`.
- A5, A6 and A7 leave west to three vias, staggered at x 131.45 and 131.95 between the shell tabs, and cross under the receptacle on L3.
- The four shell tabs are grounded.

The GPS PPS path. `J1502`, a 15-way 1 mm FPC receptacle (XUNPU FPC-1.0FX-15PWCR-H20), sits on the top edge east of the IAS1 tongue (x 187 to 208, y 102.3 to 108.8), its cable side on the edge, so a 100 mm FFC runs over the carrier to the KV260's `J9`, about 67 mm away (located from AMD's STEP model, `kv260_step_locate.py`: TE 1-1734248-5 at KiCad x 195, y 18). `J1503`, the GPS receiver's and the vehicle CAN's JST-SH, is below it. The buffer, the ESD diode, the PTC and seven passives are on the bottom of the same corner, which lies beyond the carrier's edge (y > 107.25). Its contact pads are 0.35 mm from the ring of the mounting hole `H2`; the stitching via under its east tab moved 0.85 mm. What the circuit does is in **INTEGRATIONS §2.1**.

The vehicle CAN (added the same day). `J1503` became a 6-way JST-SH (first a side-entry SM06B-SRSS-TB, see below) and moved 0.6 mm east, because its wider west tab would have sat on `LINK_RX_D1_N`, which runs straight down x 189.65 on L1; the tab now clears it by 0.26 mm (the LVDS class asks for 0.15) and has its own ground via, since that track cuts it off from the L1 pour. `F1501`'s `+3V3_D` via, now under the new pin 1, moved under the PTC's body. The transceiver `U1506` (TCAN330DCNT; the TCAN3403DDFRQ1, same pins, since the Rev08 audit, section 6.9), the ESD diode `D1531`, `Q1530` and nine passives sit on the bottom south of the GPS circuit (x 186 to 194, y 115 to 128); `Q1531` and its two base resistors found room only east of the via field (x 203 to 207, y 120 to 127), so the FPC pin 10 line runs there and its collector comes back to `CAN_TXD`. The CAN signals use L1, L3, L6 and L8 only (`CANH`/`CANL` 0.2 mm, the GPS supply 0.3 mm), never the planes. The script is `_work/rev08_can_pcb.py`; what the circuit does is in **INTEGRATIONS §2.2**.

`J1503` made vertical (the same day). The side-entry SM06B opened north, 2.8 mm from the back of `J1502`: the plug would have stood out of it into the FPC's body, its wires had nowhere to go, and no finger could reach it. It is now the vertical BM06B-SRSS-TB, so the plug goes in from above and its cable rises straight to a grommet in the enclosure's lid (ENCLOSURE §2). Its six pads are where the SM06B's were (x 191.9 to 196.9, y 114.6, 0.6 x 1.55 mm), so the copper to the pins did not change; the part turned from 180° to 0°, its pin 1 is the west pad and the pin-out is the old one mirrored: 1 ground, 2 `CANL`, 3 `CANH`, 4 ground, 5 PPS, 6 GPS 3.3 V (the STATUS sheet with it). Its mounting tabs moved 1.35 mm south (y 112.075): the old tab stubs and the west tab's via went, each tab has a ground via or stub again, and `J9_CAN_TX10`, which ran down x 197.45 where the east tab now sits, was routed again (9 segments, 2 vias, 17.2 mm). Script: `_work/rev08_j1503_vertical.py`; DRC identical to before it.

The board after these changes: 795 footprints, 13,695 track segments, 2,613 vias. DRC with zones refilled and schematic parity: **0 violations, 0 unconnected pads, 0 footprint errors**; ERC 0 errors and the same 7 warnings. The warnings are those of the board before, plus three silkscreen overlaps between the new bottom-side passives.

6.9 After the RF and power audit (18 November 2026)

The fixes of **AUDIT_Rev08.md** that touch the copper are text edits of the board (`_work/rev08_audit_pcb.py`, which reproduces them from the commit before, UUIDs aside):

- **The 300 MHz high-pass ahead of preselector B (R1).** Seven 0402 parts in frame A, in the 2 mm between `U1304`'s east pins and the frame's east wall.
- The series capacitors climb a spine at x 118.4: `C1441` and `C1443`.
- The two shunt branches sit at x 119.4: `L1441` + `C1442` and `L1442` + `C1444`. Each is grounded straight to the wall, whose pad is ground, so the branches need no vias.

- `C1445` at x 117.35 ends on a via at (116.65, 116.5). That via sits where the two inner control lines (`VU_PSA_V2` on L3, `VU_PSA_V1` on L6) leave 0.16 mm.
- From there `VU_PSB_HP` runs on L8 to the old crossing under the wall and on to `U1306`.
- `VU_PSB_IN`'s old stub, via and L8 diagonal went.
- **`U1006` pin 5** (the 50 mV ANY-OUT pin) has a 0.2 mm stub to the exposed pad: +1V8_D at 1.85 V (P4).
- **`U1506` pin 5** becomes the TCAN3403's VIO: its ground via went, and a 0.25 mm stub joins it to the +3V3_D track 0.45 mm below (P1).
- **Values in the same footprints:**
- `U1002` TPS563201, `U1315` LP5907MFX-2.8;
- `F1001` PTC 2A hold (mSMD200-24V);
- `R1031` 3.24 k, `R1542`/`R1543` 330 Ω.
- **The front end's rail** is `+2V8_RF` (it was `+3V0_RF`).

A 2920 PTC was tried for `F1001` and dropped: its courtyard would overlap `J1001`, `Q1001`, `R1004` and `TP4`.

The board now has 802 footprints, 13,709 track segments and 2,612 vias. DRC with zones refilled and schematic parity gives **the same report as before the edits**: 0 errors, 0 unconnected, 0 parity problems, and the same warnings category by category. `make_fab.py`: DRC 0 errors, 0 unrouted; BOM 224 lines and 770 parts. ERC: the same 7 warnings.

6.10 The final re-audit's copper clean-up (19 November 2026)

The re-audit before the tag (**AUDIT_Rev08.md** section 5) took the 16 copper warnings that the earlier passes had carried as accepted: `hole_to_hole`, `via_dangling` and `track_dangling`. None of them broke a connection, but one was a drilling risk and the rest were dead copper. `_work/rev08_final_cleanup.py` clears them as text edits:

- **Two vias of `Net-(C1414-Pad2)` 0.10 mm apart, drill to drill** (the rule is 0.25 mm), beside `C1415` in preselector A. The second via and its dead L1 stub went; `C1415` pad 1 now joins the first via on L8.
- **Four vias in a pad that reached no other layer:** `Y401` pad 7 (`XO_SDA`), `C927` pad 1 (`U902` RFOUT2), `FL1303` pad 1 (`VU_LP1G_IN`) and `C1332` pad 2 (`VU_ATT_IN`). Each was a dead drill and a 1.6 mm stub on its line. The board's vias in pads are filled and capped, so solder wicking was never the issue.
- **Three through vias used only as a junction between two tracks on one layer:**
- `VU_SCLK` on L8;
- `VU_TCXO_OUT` on L3;
- `VU_RESETX` on L8, with a 0.58 mm dead end past it.

Each became a short track on its layer.

- **Dead stubs of 0.01-0.7 mm on GND, +3V3_D, +2V8_RF and +1V8_D.** On +1V8_D this was a chain of short pieces lying on top of the 1 mm diagonal they duplicated.

The board now has 13,698 track segments and 2,604 vias. DRC with zones refilled and schematic parity: 0 errors, 0 unconnected, 0 parity problems, and no copper warnings at all. What is left is silkscreen and library notices:

- 9 silkscreen segments clipped by the mask (the fab clips them anyway);
- 5 silkscreen overlaps;
- 3 footprints that differ from their library copies;
- 2 footprints (the shield frames) that live only in the board.

`make_fab.py`: DRC 0 errors, 0 unrouted; BOM 224 lines and 770 parts, unchanged.

Source: docs/SIGNAL_INTEGRITY.md

Signal and power integrity: 8-layer JLC08161H-2116C review

Current `main` *baseline:* `KV260-IAS2RF.kicad_pcb` *(8-layer* `JLC08161H-2116C` *stackup) · figures and their data in* **`docs/sim/`**

> **Current 8-layer `JLC08161H-2116C` board (see §8+):** Sections 1–7 document the baseline SI checks and item-by-item copper audit (historical 6-layer comparison snapshots are archived in **`docs/history/README.md`**). Section 8 onwards measures the 8-layer routed board with the same full-wave scripts and governs wherever an earlier number changed.

An RF/high-speed engineer looked at the board of 10 November and raised the points below. Every one was checked against the board's own copper, fixed where it was right, and measured or simulated again. This page is the record: what was wrong, what changed, the numbers before and after, and what is still a compromise.

Point raised	Verdict	Now
The switch → SMA legs were not 50 Ω	**Right**: the RF50 net class missed the auto-named nets, so they were 0.10 mm	Every RF50 net (28) at 183 µm, checked by net class and DRC (§2); the only narrower copper is deliberate: 0.15 mm necks at 0.5 mm-pitch pins and 0.1 mm sections that tune out each ESD diode (§7.1)
The SMA launch is not a transmission line	**Right**: one ground via per SMA, pad over L2	Three vias per ground leg, L2–L4 cut out under the pad; openEMS: return loss 13.5 → 24.5 dB at 1 GHz (§2.1)
Controlled impedance and length matching	Half right: lengths were matched, but the LVDS legs were 59 Ω single tracks (119 Ω pairs)	Legs widened to 50 Ω where they run apart: 74 % of their length at 50 Ω, eye as an ideal pair (§3)
Power planes / decoupling loop inductance	**Right** for VCCINT: its L4 island was cut off from its own decoupling and from the regulator by the plane clearance	Zone clearance 0.15 mm, island extended under its caps, four 0.47 µF on the bottom face under the BGA; VCCINT meets its target to 100 MHz (was over it from 26 MHz) (§4)
Autorouted, "random" placement	A style point	The checks below are what decides whether it works; they were all run

Other things a reviewer would look at, found and fixed in the same pass: return vias at the LVDS and clock layer changes, two clock lines coupled at −19.5 dB, a clock leg beside a data leg on the link, legs of different pairs side by side (§3.5), exposed pads without vias, the board edge without stitching, the power plane running to the edge (§5).

1. Stack and impedance

2D field solver (`_work/field_solver.py`, finite differences on the 2116A cross-sections; JLCPCB's calculator agrees within 1–3 %, POWER_AND_STACKUP §2.6):

Line	Width	Z0
L1/L6 microstrip over L2/L5 (0.1164 mm)	0.183 mm	49.8 Ω
L3 stripline (L2 0.13 mm above, L4 0.93 mm below)	0.175 / 0.183 mm	50.2 / 48.9 Ω
L4 track (L5 0.13 mm below, L2 1.06 mm above)	0.175 mm	50.4 Ω
L1 RF line beside the L1 ground pour, 0.3 / 0.5 mm gap	0.183 mm	49.3 / 49.8 Ω
Neck-down at a 0.5 mm-pitch pin (first mm)	0.15 mm	53–54 Ω

Every signal layer has a ground plane 0.12–0.13 mm away: L1 and L3 reference L2, L4 and L6 reference L5. That is why a split in L4 (the power layer) under an L3 line costs little: the line's return runs in L2.

Reference-plane check. The two ground planes were filled the way KiCad fills them and every RF50/LVDS/clock segment was walked in 0.1 mm steps: is the strip under it (trace width + 0.1 mm a side) solid copper? Over 3,628 mm, 10 places run more than 1 mm over a void, 11 mm in all, each a crossing of a via cluster's antipads in the BGA field. No slot, no split.

2. RF band (switch → DC block → SMA)

Rebuilt by hand, not by the router:

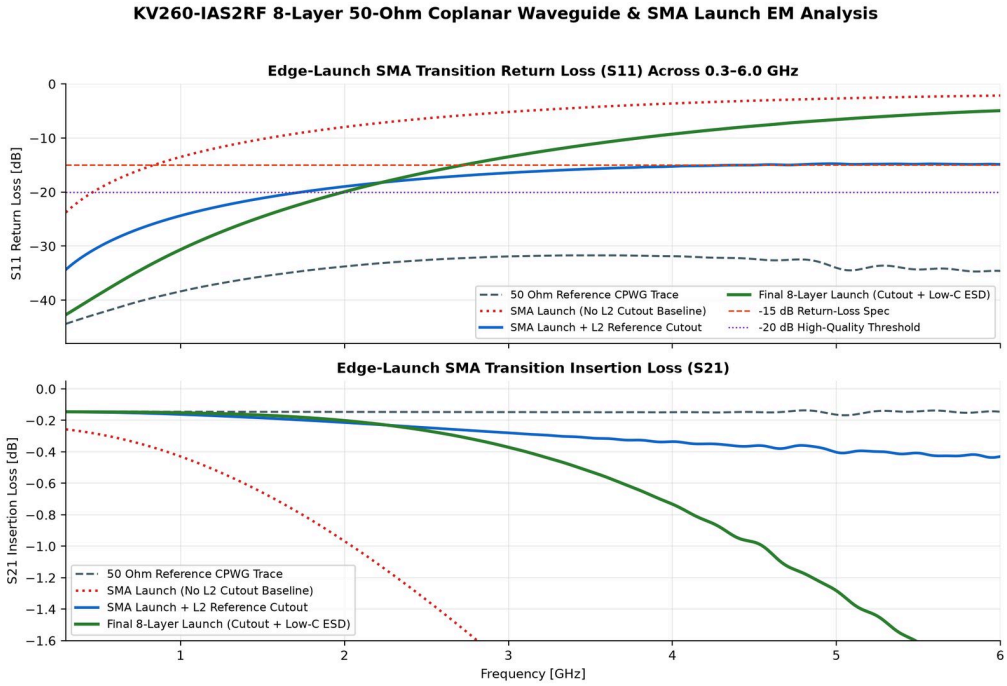
- every leg a straight 183 µm microstrip on L1, no via, 100 pF DC block next to the switch pin;
- the DC-bias parts (100 nF, Zener, resistors) moved to the bottom, under each switch cell;

- four vias in each switch's exposed pad; L1 and L6 ground pours over the band, tied to L2/L5 by a via fence 0.8 mm off each line at 1 mm pitch (226 vias);
- the 64.9 Ω terminations of the long IF lines moved under their DC-block caps (R501, R601, R621): the 7–10 mm stubs to them are gone;
- the RF50 net-class patterns now cover the auto-named nets (`Net-(J4*-In)`, `Net-(J9*-In)`, `Net-(U90*-RFOUT*)`, U401's clock nets). A design rule (`KV260-IAS2RF.kicad_dru`) lets the 0.15 mm neck at a 0.5 mm-pitch pin keep the default clearance, and a second one keeps the ground pour 0.24 mm off the 0.1 mm ESD compensation sections (§7.1).

The eight long RF lines (six IF, CLK_REF_IN, CLK_OUT) are 183 µm end to end with at most two vias each, and every via has two ground vias within 0.75–1.8 mm.

2.1 SMA launch, simulated

openEMS 0.37 (FDTD), the stack as built, FR-4 loss tan δ 0.02, the L1 pour, the via fence and the SMA's stitching vias. Through-line model: 183 µm line → the SMA's 1.27 × 3.2 mm signal pad → line. A bare line through the same set-up is the control: |S11| ≤ −32 dB, |S21| −0.15 dB to 4.5 GHz.



SMA launch

	S11		0.5 GHz	1 GHz	2 GHz	3 GHz
Pad over L2 (10 Nov)	−19.4 dB	−13.5 dB	−8.0 dB	−5.2 dB		
L2–L4 cut out under the pad	−30.2 dB	−24.4 dB	−19.0 dB	−16.4 dB		
Cut-out + ESD diode, uncompensated	−34.0 dB	−26.8 dB	−17.6 dB	−11.8 dB		
Cut-out + ESD diode, compensated (on the board, §7.1)	**−39.0 dB**	**−30.6 dB**	**−19.9 dB**	**−13.5 dB**		
Bare line (the set-up's floor)	−42.5 dB	−38.4 dB	−33.8 dB	−31.9 dB		

The wide pad 0.116 mm over L2 is a 13 Ω shunt capacitance; with the planes cleared it references L5 (1.36 mm down) and comes close to 50 Ω. |S21| at 3 GHz: −1.76 → −0.28 dB.

How to read the figure: the bare line is not a target a connector can reach, it is what the simulation itself returns for a uniform 50 Ω line with no connector (mesh and port error), so it is the floor. The band the SMAs carry ends at 500 MHz (shaded). There the board's launch is at −39 dB, 3.5 dB from the floor; return loss better than 20 dB (VSWR 1.22, the dotted line) holds to 2 GHz, four times the highest frequency used. Above 2 GHz the ESD diode's capacitance shows: the cost of protecting the connector, and outside the band.

3. LVDS

3.1 What the router left

The LVDS pairs (link to the Kria, both ADCs' data and clocks) were laid as two separate legs: 89 % of their length runs more

than 1 mm apart, so they are loosely coupled pairs. A loosely coupled pair's impedance is twice its legs' Z0, and the legs were 0.117 mm (the coupled-pair width): 59 Ω each, 117–119 Ω for the pair against a 100 Ω termination.

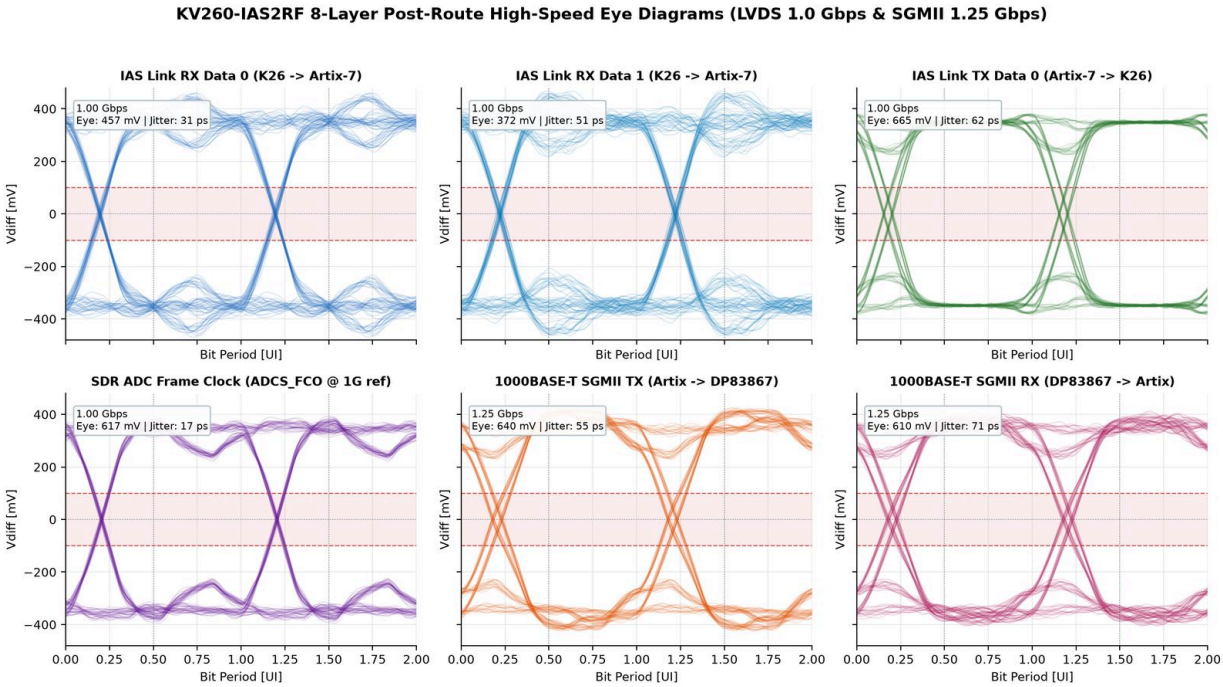
3.2 What changed

Each leg was widened to its layer's 50 Ω width (0.183 mm on L1/L6, 0.175 mm on L3/L4) wherever the clearances allow, judged in 0.5 mm pieces so a leg necks only where something is in the way. The centre lines did not move, so lengths and skew are unchanged.

Width	Length	Leg Z0	Pair
0.183 / 0.175 mm	1,896 mm, 74 %	49–50 Ω	≈ 100 Ω
0.15 mm	270 mm, 11 %	53–54 Ω	≈ 107 Ω
0.13 mm	102 mm, 4 %	57 Ω	≈ 114 Ω
0.117 mm (no room: BGA escapes)	237 mm, 9 %	58–59 Ω	≈ 118 Ω
coupled stretches, left as they were	55 mm, 2 %	n/a	100 Ω

3.3 Eye, simulated

ngspice, PRBS7 at 1 Gb/s, LVDS current driver (3.5 mA, 300 ps edges), 100 Ω across the receiver and 2 pF per input; each leg is its own copper by layer and width, with Z0 and delay from the field solver, the mismatched sections put together at the receiver end (ordered by Z0; sections under 3 mm lumped). Re-run on the final board of 11 Nov (with the ESD parts); differences from the first run are within 15 mV and 10 ps. Three cases per pair: an ideal 100 Ω pair of the same length and termination, the board on 6 layers (11 Nov) and on 8 layers (12 Nov, §8).



LVDS eyes on the 8-layer board

Pair	6 layers: ideal / routed	8 layers: ideal / routed
ADCR_D0	600 / 583 mV, 29 / 25 ps	634 / 632 mV, 16 / 16 ps
ADCR_D1	515 / 484 mV, 14 / 15 ps	474 / 473 mV, 19 / 19 ps
ADCR_D2	594 / 481 mV, 27 / 56 ps	465 / 463 mV, 23 / 23 ps
ADCR_D3	531 / 526 mV, 62 / 53 ps	464 / 463 mV, 23 / 23 ps
ADCR_D4	542 / 557 mV, 34 / 54 ps	633 / 607 mV, 19 / 17 ps
ADCR_D5	458 / 446 mV, 54 / 71 ps	505 / 505 mV, 16 / 16 ps
ADCR_D6	540 / 513 mV, 20 / 41 ps	471 / 500 mV, 22 / 25 ps
ADCR_D7	633 / 609 mV, 18 / 18 ps	471 / 466 mV, 16 / 17 ps
ADCR_DCO	626 / 581 mV, 24 / 35 ps	609 / 610 mV, 17 / 18 ps

Pair	6 layers: ideal / routed	8 layers: ideal / routed
ADCR_OR	450 / 465 mV, 69 / 85 ps	647 / 646 mV, 19 / 18 ps
ADCS_D0	581 / 564 mV, 41 / 51 ps	618 / 614 mV, 22 / 25 ps
ADCS_D1	589 / 533 mV, 53 / 39 ps	625 / 607 mV, 16 / 15 ps
ADCS_DCO	597 / 602 mV, 40 / 35 ps	632 / 609 mV, 18 / 20 ps
ADCS_FCO	648 / 650 mV, 49 / 46 ps	628 / 617 mV, 17 / 17 ps
FPGA_CLK	448 / 446 mV, 16 / 17 ps	517 / 499 mV, 29 / 29 ps
LINK_RX_CLK	548 / 516 mV, 12 / 14 ps	395 / 392 mV, 10 / 10 ps
LINK_RX_D0	607 / 559 mV, 35 / 30 ps	509 / 457 mV, 25 / 31 ps
LINK_RX_D1	575 / 559 mV, 75 / 77 ps	385 / 372 mV, 41 / 51 ps
LINK_TX_CLK	661 / 635 mV, 63 / 69 ps	642 / 643 mV, 63 / 63 ps
LINK_TX_D0	664 / 653 mV, 65 / 68 ps	674 / 665 mV, 64 / 62 ps

Eye opening at the centre of the bit, then zero-crossing spread; each board against the ideal line of its own pair length and termination.

The ideal line differs between the two boards because the pair lengths and the termination point changed (on 8 layers every termination sits on the FPGA's ball vias). The opening is in every case several times the receiver's ±100 mV threshold. For LINK_RX the model ends at the AC capacitors, so those eyes are indicative only. The numbers are in **`docs/sim/`** (`lvds_eye.csv`).

On the rate. IAS1 carries five pairs, but two are source-synchronous clocks: three data lanes at up to 1 Gb/s each (two to the Kria, one back; INTERFACE_SPEC §3). What signal integrity sees is the rate per lane, 1 Gb/s.

3.4 Skew

Unchanged by the widening (`_work/layout/lvds_skew.py`, pin to pin). One change: **LINK_RX_CLK** was −60 ps, over the 50 ps rule of LAYOUT §6.3; its P leg now has 10 mm of meander on L1, on the side of its own N leg: **0 ps**. Data to clock on LINK_RX: D0 +79 → +51 ps, D1 +207 → +177 ps (the Kria's IDELAYE3 trains these).

With the FPGA's package delays (11 Nov evening). The figures above are pad to pad. AMD gives each XC7A50T-FTG256 ball's flight time inside the package (Vivado `get_package_pins`, MIN_DELAY and MAX_DELAY; 35–133 ps across the I/O balls). They are in `_work/layout/xc7a50t_ftg256_pkg_delays.csv`, and `lvds_skew.py` now adds each FPGA ball's mean delay to its leg (`--no-pkg` for pad to pad):

	Pad to pad	With the package
Package share of a pair's P−N	n/a	−4.4 to +9.4 ps
Worst P−N, pairs at 1 Gb/s	±42 ps	±40 ps (ADCS_D1 +40, LINK_TX_CLK −36)
LINK_RX data − clock	D0 +51, D1 +177 ps	D0 +41, D1 +190 ps
LINK_TX data − clock	+2 ps	−17 ps
ADCS (AD9253) data − DCO	−74 to +45 ps	−81 to +26 ps
ADCR (AD9484) data − DCO	−80 to −16 ps	−88 to 0 ps

The P−N skews stay within the rule. The data-to-clock offsets are what each lane's IDELAY calibrates at start-up (78 ps taps on the Artix-7, 1.1 ns range on the K26's IDELAYE3).

3.5 Crosstalk

Parallel runs closer than three widths for more than 2 mm were listed and the coupling computed with the field solver (even/odd mode):

Run	Before	Fix	After
U401's reference input (CLK0) and its output Q3, 47 mm side by side on L3	0.22 mm gap, NEXT −19.5 dB: the buffer's output fed back into its own input pin	Q3 moved out to the board edge (x 207.55) and its diagonal 1.3 mm off	1.0–1.3 mm, about −45 dB
LINK_RX_CLK_P beside LINK_RX_D0_P, 31 mm on L1	0.16 mm gap, about −18 dB	Each P leg moved next to its own N leg	1.0 mm between the pairs, about −46 dB

Legs of different pairs side by side. Because the pairs are not coupled, a leg can run beside a leg of another pair with

nothing of its own partner to cancel it. Every fast leg was walked in 0.25 mm steps against every other pair's copper on its layer: 133 mm (of 3,639 mm) ran with less than 0.25 mm to another pair's leg, at the class clearance of 0.15 mm in the worst places. Field solver, 0.183 mm legs on L1/L6: backward coupling 14.5 % at a 0.15 mm gap, 7.7 % at 0.25 mm, 4.6 % at 0.35 mm, 2 % at 0.55 mm (L3: 16.7 / 9.7 / 6.1 / 2.8 %). A run shorter than 25 mm (half a 300 ps edge) couples in proportion to its length.

Where there was room the leg was moved away with a 45° jog at each end (seven runs, 42 mm; skew changed by 3 ps at most): ADCS_FCO_N off ADCS_D1_N (14 mm, 0.15 → 0.35 mm), off LINK_RX_CLK_P, ADCR_D2_P off ADCR_D0_P, LINK_RX_D0_N off ADCR_OR_N and three shorter ones. **98 mm are left** with less than 0.25 mm, none with room to move without re-routing its neighbours. The worst:

Run	Layer	Length under 0.25 mm	Near-end crosstalk on the victim leg
ADCR_D0_P beside ADCR_D1_N	L6	12.6 mm at 0.15 mm	7 % of the aggressor's swing
ADCR_D1_P beside ADCR_D3_P	L1	7.7 mm	4.5 %
F_DACR_CLK beside LINK_RX_CLK_N	L1	6.4 mm	3.7 %
ADCR_D4_P beside ADCS_FCO_P	L1	6.0 mm	3.5 %
ADCR_OR_N beside ADCS_D1_P	L6	5.7 mm	3.3 %
ADCR_D6_N beside ADCR_D7_N	L1	5.6 mm	3.2 %
LINK_TX_CLK_P beside LINK_TX_D0_N	L3	3.9 mm at 0.18 mm	2.5 %

7 % of a 350 mV leg is 25 mV on one leg of a pair whose eye opens 550–650 mV and whose receiver threshold is ±100 mV: it works, with less margin than a coupled pair would have (a coupled pair sees the same aggressor on both legs). These are in the escape between the FPGA and the two ADCs; they go with the fan-out (§6). The rest of the list is a data leg beside a supply track, or flash and I²C lines that are static while the board runs.

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4. Power distribution

4.1 What was wrong

Measured on the board's copper (KiCad-style fill of L4, connectivity by overlap, 0.4 nH/mm of track, via barrels by height; UG483's criterion is the impedance from 100 kHz to 10 MHz):

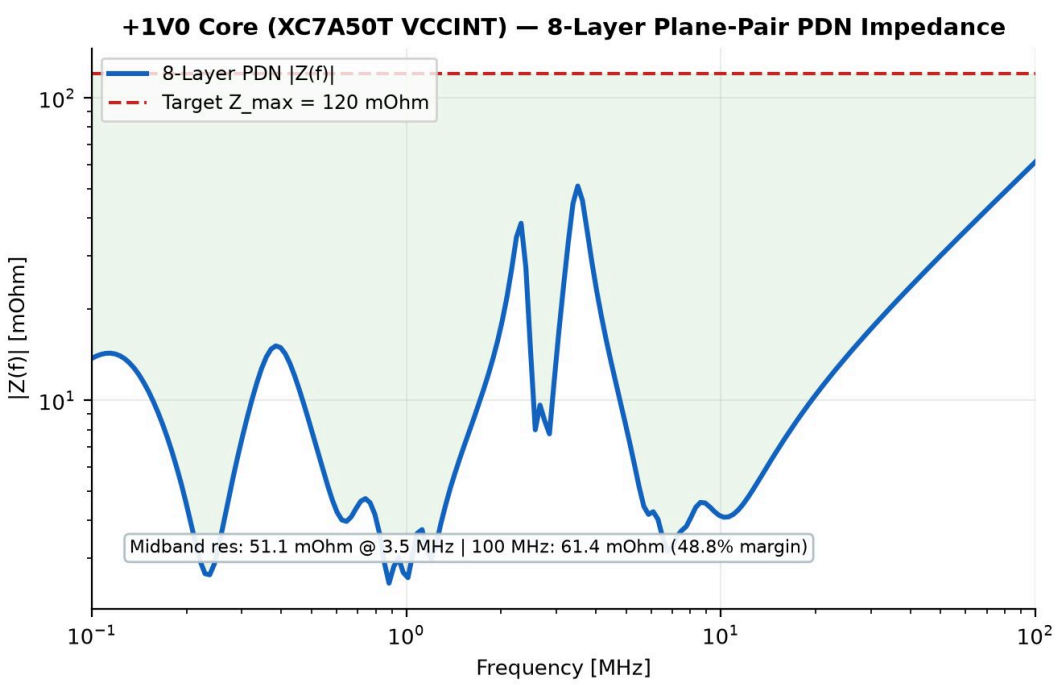
- **VCCINT's L4 island under the BGA was cut off from the strip that feeds it** from the buck. With a 0.3 mm zone clearance, the 0.45 mm vias at 1 mm pitch leave no copper between them: the island reached the rest of +1V0 only through tracks. The same clearance on the GND planes left no web between neighbouring BGA vias.
- VCCINT's 0.47 µF caps reached the balls through 58–63 nH of track.

4.2 What changed

- **Inner-plane zone clearance 0.3 → 0.15 mm** (L2, L4, L5): 0.25 mm of copper between vias at 1 mm pitch. JLCPCB's inner-layer minimum is 0.1 mm.
- The +1V0 island extended under the four 0.47 µF caps below the BGA (no +3V3_D via needs L4 there) and a notch cut where it swallowed a DAC's +3V3_D via.
- Five vias in the buck inductor L1030's output pad, straight into the strip.
- Butted vias on decoupling pads where there was room (UG483: "never connect vias to the lands with a section of trace").
- **Four more 0.47 µF 0402 (C1184–C1187) on the bottom face inside the BGA footprint**, each pad on a +1V0 or a GND ball via (via in pad, filled and capped): L4 is 0.25 mm from the bottom face and 1.18 mm from the top, so their loops are 0.60–0.71 nH, against 1.1–1.4 nH for the best top-side caps and 7–13 nH for the 4.7 µF ones. FPGA_IRQ was re-routed off one of them.

UG483's required caps for the XC7A50T in FTG256 (Table 2-2: VCCINT 1 × 330 µF, 3 × 4.7 µF, 5 × 0.47 µF; VCCBRAM 1 × 100 µF, 1 × 0.47 µF; VCCAUX 1 × 47 µF, 2 × 4.7 µF, 3 × 0.47 µF) are all on the board. Artix-7 has no capacitors inside its package (UG483 p. 14), so the board's network is all there is.

4.3 Impedance at the balls



VCCINT

Rail	Target		Z	max, 0.1–10 MHz (before → now)	Over the target
+1V0 VCCINT	120 mΩ	67 → **51 mΩ**	26 MHz and up → **nowhere to 100 MHz**; 470 → 61 mΩ at 100 MHz		
+1V8_D VCCAUX, VCCO_35	700 mΩ	127 → 109 mΩ	nowhere to 100 MHz		
+2V5 VCCO_34	2 Ω	149 → 146 mΩ	nowhere		
+3V3_D VCCO	1 Ω	36 → 37 mΩ	nowhere		

Model (`pdn2.py`): each capacitor's loop is its ESL, its pads and vias, and the copper path to the balls; the die draws on all its balls of a rail at once, so from a plane the paths to the balls are in parallel. Both boards above are computed with the same model. Without the four bottom-side caps VCCINT went over its target from 81 MHz (149 mΩ at 100 MHz). Above 100 MHz the package and the die's own capacitance take over, which a board model cannot see; UG483 sets the board's job at 100 kHz–10 MHz, where VCCINT is at less than half its target.

The other rails' plots: **`sim/pdn_1V8_D.png`**, **`sim/pdn_2V5.png`**, **`sim/pdn_3V3_D.png`**.

4.4 DC drop

Least-resistance copper path from the regulator to the balls (1 oz outer, 0.5 oz inner; parallel paths ignored, so an upper bound):

Rail	Current (FPGA's share)	Path	Drop
+1V0 from L1030	700 mA	27–46 mΩ	19–32 mV (1.9–3.2 %; 34–53 mΩ before the inductor's vias)
+1V8_D from U1006	about 150 mA	184–263 mΩ	28–39 mV (1.5–2.2 %)
+2V5 from L1020	about 100 mA	287–307 mΩ	29–31 mV (1.2 %)

VCCINT's limit is ±5 %. With the TPS562201's ±1.5 % and 32 mV, the worst ball sits at about 0.958 V at full estimated load: inside, with little to spare. If Vivado's power report comes in above 700 mA, set the buck to 1.02 V (one feedback resistor).

Corrected by the Rev08 audit (18 November, AUDIT_Rev08.md §2.2). The TPS562201's reference is 749-787 mV over temperature, ±2.5 %, not ±1.5 %, and Vivado now gives VCCINT 735 mA at 70 °C. `R1031` is 3.24 k: +1V0 at 1.017 V, so the balls sit at about 0.983 V at full load. The worst-case linear stack (reference, 1 % resistors, ripple and step, 34 mV of drop) spans 0.933-1.067 V; the root-sum-square of the same terms stays inside 0.95-1.05 V. To measure on the first board; the XADC reports VCCINT in `XADC_TEMP_VCCINT`.

5. Other checks

Check	Found	Fixed
Return vias at layer changes (LVDS, clocks)	145 of 185 reference-changing vias without a ground via within 1 mm	136 ground vias added (118 at 0.2 mm from other nets, then 18 more at the 0.15 mm the net classes ask for, two of them after moving a supply and an I²C track aside): 50 within 1 mm, 91 within 2 mm, 44 within 3 mm, **one at 3.1 mm** (ADCR_D4_P; λ/20 at the 1.2 GHz knee of a 300 ps edge is 6 mm). RF50: two within 1.8 mm, one exception with one
Exposed pads	LMR33630, all three TPS7A8300 (one dissipates 0.5 W), one AD8352 with **no via**; AD9253 3 vias in 31 mm²	Via grids in every pad (POFV): LMR33630 15, each TPS7A8300 4, AD8352s 2–5, AD9253 15, AD9484 16, ADCLK948 6
Board edge	256 of 1,122 points on the outline had a ground via within 3 mm	176-via fence 0.8 mm in, 2.5 mm pitch (22 stations blocked by connectors)
Power plane at the edge	L4 ran to the edge with L2/L5	Every L4 zone pulled back 1 mm from the edge
Plane splits under fast lines	None (§1)	n/a
Acute angles	453 junctions under 90°, mostly overlapping collinear segments and the router's 45° steps	None: JLCPCB's process does not need it; no DFM flag

6. What is still a compromise

- **11 of the FPGA's 69 supply balls have no via of their own.** Seven have a plane to reach and no room for the via: VCCINT K9, L8; GND A1, F8, G13, N5; +3V3_D L16. Each reaches its plane through a short top track to a neighbour's via (VCCINT: 7 of 9 balls have their own; the four bottom-side caps of §4.3 sit on those vias). The other four (+1V8_D A6, J2, K11; +2V5 R4) are on rails that have no plane under the BGA at all: they are fed by tracks, and a via would reach nothing. Their impedance is inside the target all the same (§4.3: 109 mΩ against 700, 144 mΩ against 2 Ω). Two ways were tried on every ball: ripping what blocks the spot and re-routing (GND K7, K14), and leaving the routing alone but bending the blocking tracks round the new via (VCCINT F7, G6; GND N15; +3V3_D T11); each kept only at zero unrouted and zero violations. What is left needs the escape of those rows redone.
- **The LVDS pairs are loosely coupled**, not routed as coupled pairs: 100 Ω by leg width, but less rejection of common-mode noise picked up on the way, and legs of different pairs side by side between the FPGA and the ADCs (§3.5: 98 mm under 0.25 mm, 7 % crosstalk on the worst leg). A pair-routed board is the better board; on this placement and pin assignment the pairs cross each other on the way out of the BGA, which is why the router could not keep them together. It is a change of FPGA pin assignment and escape, not a touch-up.
- **One LVDS layer change has its nearest ground via 3.1 mm away** (ADCR_D4_P; the limit set here is 3 mm, λ/20 at a 300 ps edge is 6 mm). The other 185 are within 3 mm, 141 of them within 2 mm.
- **VCCINT's 4.7 µF caps** sit 6 mm above the BGA, fed by track (7–13 nH): no room on either face over the island. UG483 allows "within two electrical inches"; the impedance target holds.

What has not been simulated (12 Nov). Everything above is 2-D field solving, circuit simulation and the openEMS SMA launch. None of it replaces measuring a built board:

- **No 3-D full-wave model of the board.** The LVDS eyes use lossless lines with the field-solved Z0 and delay of each section, and the crosstalk figures are 2-D coupling coefficients times the parallel length. Vias, the BGA breakout and the Hirose connector enter only as lumped sections.
- **No cascade analysis of the RF chains.** The ADC drivers' gains (15 + 10 dB, as AERIS-10), the baluns, the anti-alias and reconstruction filters and the RF switches are drawn from their data sheets and application notes. Nobody has computed a noise figure, IP3 or ripple-and-gain budget per channel, nor simulated the filters' responses with the board's parasitics.
- **No thermal analysis** beyond the per-part dissipation and thermal vias in §7.
- **Nothing is measured.** The first boards are for evaluation: the link's bring-up test is in IAS_LINK_SPEC §6, and its capacity and rate ceiling in §7.

How each of these would be done is in §9.6. §9 also covers the rest of the board: the supply tracks, fixed on 12 Nov (§9.1), and what is still open there (§9.2–9.4).

7. Environment

	State
Temperature	Every IC industrial or better: XC7A50T-2FTG256I (Tj −40 to 100 °C), ADCs, drivers, clock buffer, DACs, regulators −40 to 85/125 °C, RF switches −55 to 105 °C, Hirose BM20B −35 to 85 °C. Capacitors X7R/X5R (X5R to 85 °C)
Heat	The 0.5 W LDO now has its thermal vias; the bucks are SOT-23 parts at ≤ 0.4 W
Input	12 V: PTC, SMCJ33CA, back-to-back 100 V N-FETs under an LM74502-Q1 (reverse battery to −65 V, overvoltage cut-off 18.3 V), SMBJ18CA on +12V: POWER_SPEC §1.1 (13 Nov, after the RF review)
Mechanics	Five M3 holes (two through the KV260, three to standoffs); edge SMAs soldered and through the board. For vibration: staking of the SMAs and the 7343 capacitor, or a conformal coat, at assembly
EMI	Ground planes next to every signal layer, edge fence, power plane pulled back, return vias (§5)
ESD	Every external connector: a PESD5V0F1BL (0.4 pF, bidirectional, IEC 61000-4-2) on each of the 12 edge SMAs (and, since Rev08, D1301 on `J961`, §9.10), 2.15 mm from the SMA pad and tuned out by 0.1 mm line sections either side; TPD4E05U06DQAR four-channel arrays (0.5 pF) on the Pmod (U1108, U1109) and JTAG (U1110) next to their headers. Each ground pad has its own GND via (0.4–1 mm). The 12 V input already has its SMBJ15CA. §7.1

7.1 ESD on the SMAs

The SMAs carry HF from 100 kHz, the wideband SDR to about 250 MHz, the radar IF at 120 MHz and the reference clock to 500 MHz. A shunt inductor to ground (an "RF choke") that does not load 50 Ω at 100 kHz needs more than 80 µH, which self-resonates at a few MHz: it would short VHF and protect nothing. A low-capacitance TVS is the part for this band. openEMS, the launch of §2.1 with the diode's pad and 0.5 pF where it is placed (2.15 mm from the SMA pad):

	0.5 GHz	1 GHz	2 GHz	3 GHz
S11, diode alone	−34.0 dB	−26.8 dB	−17.6 dB	−11.8 dB
S11, compensated (on the board)	**−39.0 dB**	**−30.6 dB**	**−19.9 dB**	**−13.5 dB**
S21, compensated	−0.15 dB	−0.15 dB	−0.20 dB	−0.37 dB

The diode is a shunt capacitance on the line. It is tuned out by two short high-impedance sections either side of it (series inductance, so the three make a low-pass π section close to 50 Ω): the line is 0.1 mm wide from the DC-block pad up to the diode pad (0.76 mm, all the room there is) and for 1.4 mm past it towards the SMA, with the ground pour kept 0.24 mm off them (a design rule). openEMS sweep of the length, 0.1 mm each side: 0.8 mm −38.3 dB at 0.5 GHz, 1.4 mm −39.4, 2.0 mm −37.1, 2.8 mm −32.2; 0.8 mm before and 1.4 or 1.8 mm after, as fits: −39.0 dB (`_work/sim/sma_launch.py tvsnAA_BB`). With it the launch with the diode is better in the band than the bare cut-out was (−30.2 dB at 0.5 GHz).

8. Eight layers (12 November)

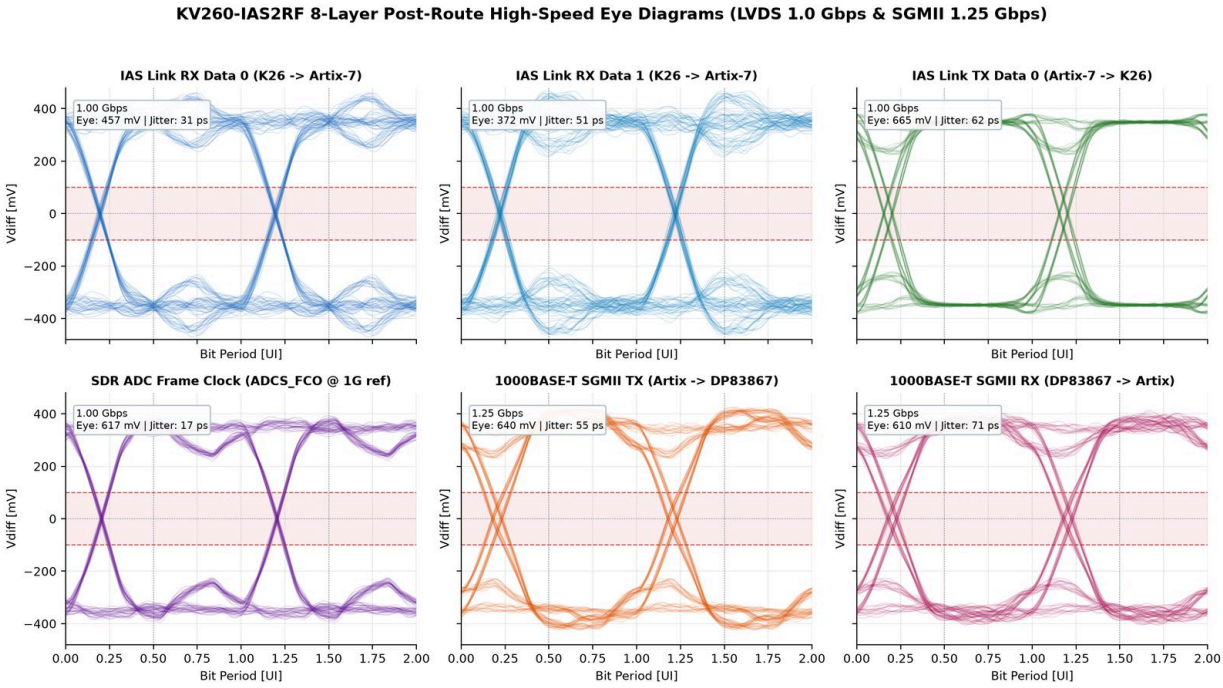
The stack moved to JLC08161H-2116C: L1 · L2 GND · L3 · L4 PWR · L5 GND · L6 · L7 GND · L8, with 2116 prepreg (0.1194 mm) under the outer layers, so the 183 µm RF width and the SMA launch stand. Field solver (`_work/field_solver8.py`):

Line	Width / gap	Z
L1/L8 microstrip	0.183 mm	50.4 Ω
L3/L6 stripline, single	0.151 mm	50 Ω
L3/L6 coupled pair	0.10 / 0.15 mm	100.2 Ω
L3/L6 pair under the FPGA	0.09 / 0.12 mm	98.5 Ω
L1 coupled pair	0.117 / 0.15 mm	100.4 Ω

What changed on the board: L4 carries no signal; L6 lies between two ground planes; 9 of the 19 LVDS pairs are coupled 100 Ω pairs end to end and the other 10 are two 50 Ω legs matched to ±5 ps; every 100 Ω termination sits on its pair's two ball vias on the bottom face (no stub); LINK_TX is terminated at the FPGA (R105/R106 added, R101–R104 now 10 k bias), where before the 2 × 49.9 Ω at the connector left the FPGA's receiver at the end of a 45 mm open line.

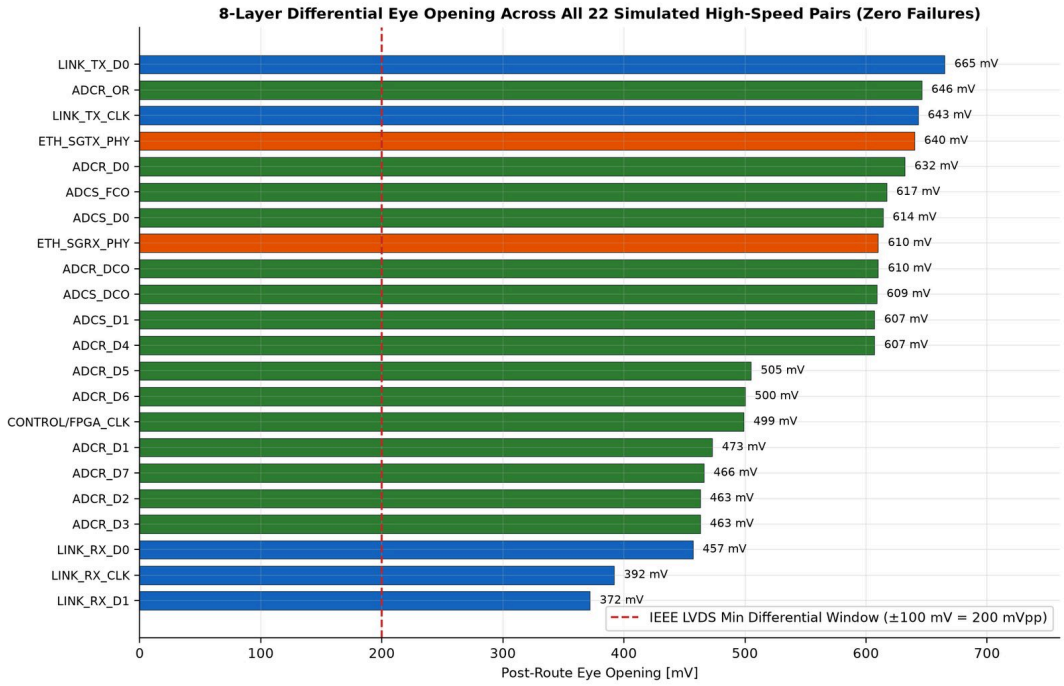
Check	6 layers (11 Nov)	8 layers (12 Nov)
DRC	0 errors, 0 unconnected, 0 parity	0 violations of any kind, 0 unconnected, 0 parity
Pairs coupled	0 of 19	9 of 19 (ADCR_D4 41 %)
Worst intra-pair |P−N|, package included	84 ps	9 ps
Layer changes without a GND via within 3 mm	1 of 186	0 of 89
Track over a plane void	10 runs, 11 mm	5 runs, 5 mm

Check	6 layers (11 Nov)	8 layers (12 Nov)
Legs of other pairs within 0.25 / 0.55 mm	97.6 / 328.4 mm	69.3 / 213.5 mm
Eye lost to the routing (routed − ideal, 20 pairs)	mean −22 mV, worst −113 mV	mean −8 mV, worst −52 mV
Zero-crossing spread added by the routing	mean 5 ps, worst 29 ps	mean 1 ps, worst 10 ps
VCCINT impedance (target 120 mΩ)	51 mΩ max to 10 MHz, 61 at 100 MHz	41 / 63 mΩ
+1V8_D / +2V5 / +3V3_D at 100 MHz	545 / 488 / 40 mΩ	545 / 460 / 37 mΩ
DC drop +2V5 at 601 mA	173–185 mV	122–129 mV (trunk widened to 0.5 mm)
SMA launch S11 at 1 / 3 GHz, with the ESD diode	−30.6 / −13.5 dB	−30.9 / −13.7 dB

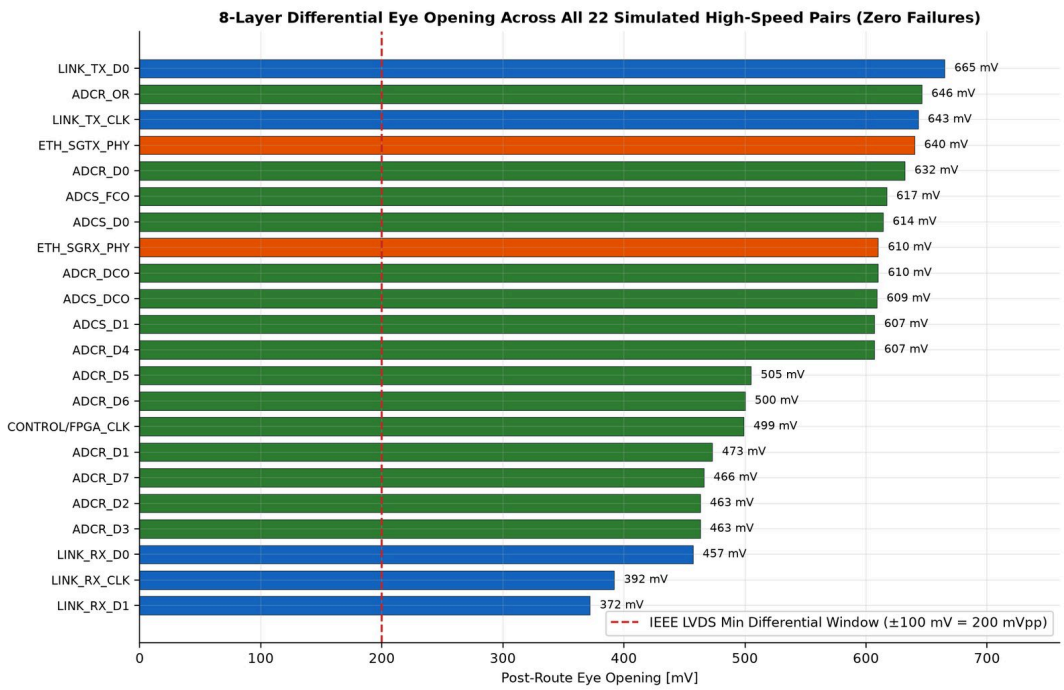


LVDS eyes on the 8-layer board

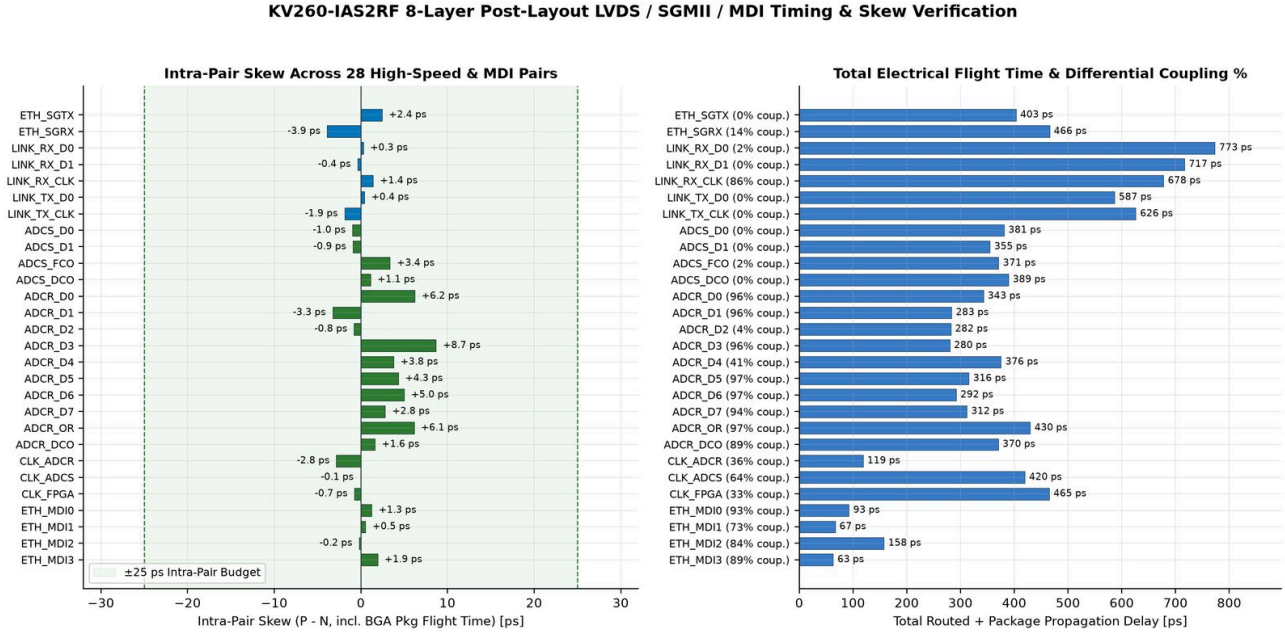
The eye model drives each leg from a current source into the routed sections and a 100 Ω, 2 pF receiver. The receiver's capacitance reflects and the driver re-reflects, so even the ideal line has some ISI and it depends on length: the "ideal" of a pair differs between the two boards. The fair comparison is each board against its own ideal line:



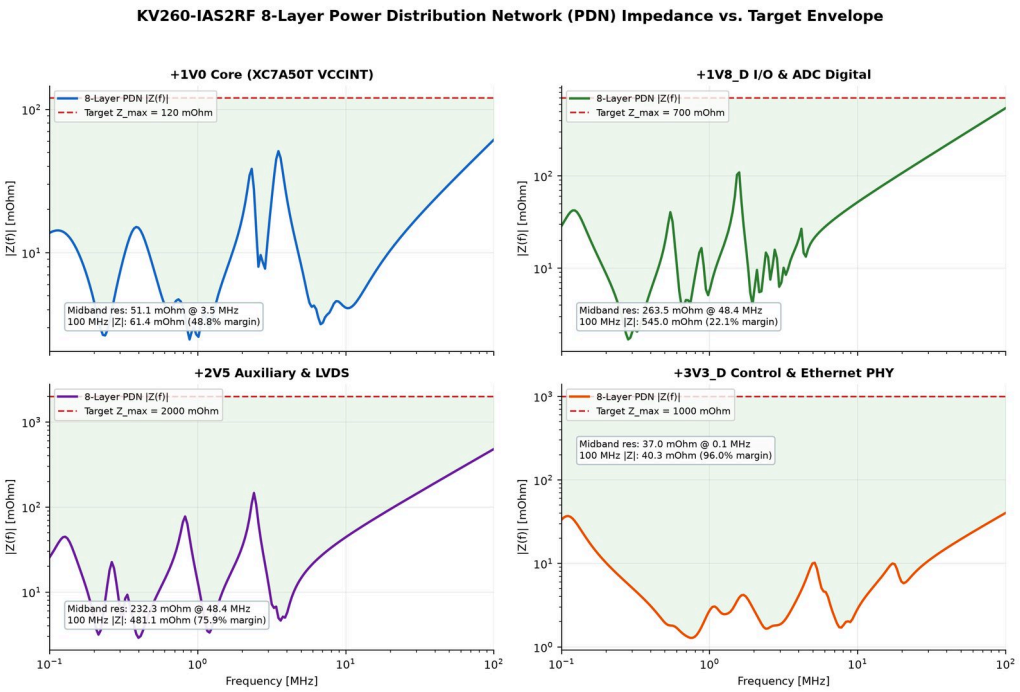
Eye lost to the routing



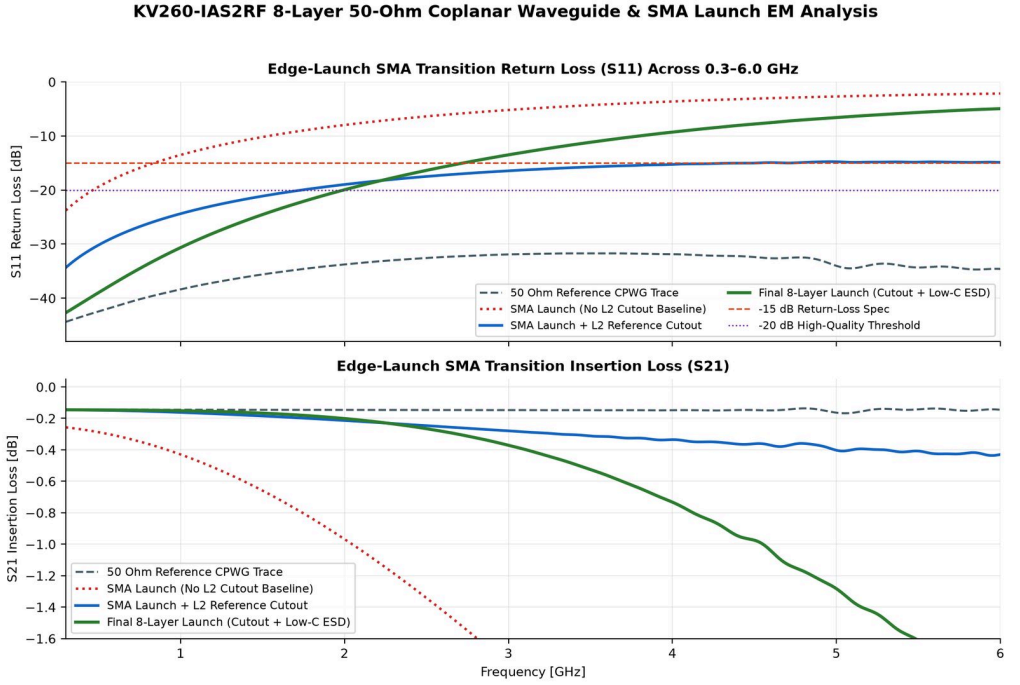
Eye opening and spread, every pair



Intra-pair skew



PDN impedance



SMA launch

The third series in the eye and skew plots is the 6-layer board with the same corrections (terminations at the balls, coupled pairs, LINK_TX at its receiver), routed the same way: only 8 pairs fit coupled, because under the FPGA L4 is +1V0 islands where no track may go and L3 is the only inner layer, and the board could not be completed (seven nets left unconnected). On six layers the schematic change, the +2V5 widening and the return vias carry over as they are; the stub-free terminations and the coupled pairs need the second inner signal layer.

Still open on the 8-layer board:

- **ADCR data to DCO: −90 to +5 ps** (6 layers: −23 to −88; −177 to −28 until 12 Nov). ADCR_DCO's legs are swapped at the FPGA (the gateware inverts the clock), so the pair no longer goes round the AD9484 to reach its pins the right way round: 39 mm instead of 51, 89 % coupled, eye 2 mV under ideal. The rest is inside the IDELAYE2's 2.4 ns range, calibrated per bit at start-up.
- **Ten pairs are not coupled** (LINK_RX_D0/D1, LINK_TX_D0/CLK, the four ADCS pairs, ADCR_D2, ADCR_D4 partly). The LINK_RX pairs leave the FPGA's south rows and must cross every ADC pair on the way north; the AD9253's 0.5 mm pins leave no room for a coupled fan-out. They are 50 Ω legs matched to ±5 ps, within 1–26 mV of their ideal eye

except LINK_RX_D0 (−52 mV). LINK_RX's bank 34 sits in the BGA's south-east corner: there are no north-side balls for it, and its outer balls (tried 12 Nov) leave no room for the vias. Coupling it needs the AC capacitors at J101, now 9 mm apart, placed together first.

- **CLK_ADCR P−N: −3 ps** (−44 until 12 Nov): C414 and C415 side by side at 1 mm pitch, so both legs leave U401 together, and a meander on P on L3.
- Supersedes in §6: the pairs are now partly coupled, and every layer change has a ground via within 3 mm.

9. The rest of the board (12 November, evening)

Sections 2–8 cover what the review named: the RF band, the LVDS pairs and the FPGA's supplies. This pass looks at every other net, with three checks run on the board file:

- **Current through each supply track.** Each track that every path from a rail's source to some of its loads must cross is given those loads' current (the budget of POWER_AND_STACKUP §1.3–1.4). The check reports its IPC-2221 temperature rise and the series drop.
- **Other nets' copper beside analogue nets**, on the same layer, within 0.3 mm. Broadside coupling to the next layer is not counted.
- **Each net's routed length against its shortest tree.** In all, 11.5 m of track for 9.4 m of minimum tree (×1.21), and 1,099 signal vias.

9.1 Supply tracks necked to 0.1 mm (fixed 12 Nov)

The router had necked supply tracks down to 0.1 mm wherever space was short. The `Power` netclass did not stop it, for two reasons:

- **It sets the default width for new tracks, not a minimum.** The necks on the named rails were legal.
- **It does not cover the switch nodes or the input path.** `Net-(U100x-SW)`, `Net-(F1001-Pad1)` and `Net-(Q1001-D)` have no name to match: the same gap the review found on the SMA legs.

Path	Current	Before	After
Input, J1001 → F1001 → Q1001	0.75 A	0.1 mm, 8 mm (ΔT ≈ 32 °C)	1.0 mm
+12V, Q1001 → U1001	0.75 A	0.3 mm, a 1.6 mm piece on L3	0.4–1.0 mm
U1001's switch node → L1001 (+5V0)	1.6 A	**0.1 mm, 8 mm (ΔT ≈ 180 °C)**	0.4–1.0 mm; two 0.4 mm pieces at 0.2 mm by the pins
U1002's switch node (+3V3_D)	1.13 A	0.1 mm, 6 mm	0.15–1.0 mm; the narrow 2 mm next to the pins
U1003 / U1004's switch nodes (+2V5, +1V0)	0.6 / 0.7 A	0.1 mm, 7–9 mm	0.15–1.0 mm
+1V8_A, U1005 → FB502/FB602: 75 mm, mostly on L3 (15 µm copper)	0.5 A	0.1 mm for 11 mm, then 0.3 mm: 0.50 Ω, **251 mV drop**, ΔT ≈ 240 °C on the narrow part	1.0 mm for 99 mm, narrower only between vias and pads: **66 + 8 mV**

The ΔT figures are the IPC-2221 chart for a long track. A piece under a millimetre between wide copper runs cooler. Every `Power` track was widened where its clearances allowed (1.0, 0.8, 0.6 … 0.15 mm, judged in 0.5 mm pieces):

`Power`-class track	Before	After
≤ 0.15 mm	365 mm	161 mm
≥ 0.5 mm	119 mm	865 mm
Total	1,554 mm	1,554 mm

L4, the supply plane layer, was left alone. DRC is 0 / 0 / 0 with schematic parity.

+1V8_A, the ADCs' AVDD, now starts at 1.85 V. Its LDO sits 75 mm from the ADCs.

- **The problem.** At the budget's 0.5 A the copper drops 74 mV and FB502's ferrite up to 30 mV (DCR ≤ 0.1 Ω, ADC_RADAR_SPEC). From 1.8 V that leaves 1.69 V at the AD9484, under its 1.7 V minimum. Before the widening it would have been about 1.5 V.
- **The fix.** U1005's 50 mV ANY-OUT pin is now grounded (POWER sheet, `power_spec.py`): 0.8 + 0.05 + 0.2 + 0.8 = 1.85 V. The ADCs see about 1.74 V at full budget and 1.85 V unloaded, both inside 1.7–1.9 V even with the LDO's 1 % tolerance.
- **What else would work.** Moving U1005 next to the ADCs would remove the drop, at the cost of a re-placement.

9.2 Analogue nets beside digital ones (open)

`xtalk.py` (§3.5) compares LVDS legs only. Against the analogue nets, the longest same-layer parallels within 0.3 mm are:

Victim	Aggressor	Layer	Parallel, gap
SDR DAC reconstruction filter, DAC2 (C834)	`DACS_D0`	L3	12.5 mm at 0.11 mm
SDR DAC reconstruction filter, DAC1 (C814)	`+1V0` (a buck's output)	L1	13.5 mm at 0.20 mm
SDR DAC reconstruction filter, DAC1 (C814)	`DACS_D4`	L8	4.0 mm at 0.10 mm
SDR DAC reconstruction filter, DAC2 (C834)	`ADAR2_CS`	L3	4.1 mm at 0.10 mm
SDR ADC input network (C605)	`CONV_SPI_SDIO`	L3	4.4 mm at 0.10 mm
SDR ADC input network (C607)	`CLK_ADCS_P`	L1	4.0 mm at 0.15 mm
Radar IF, between the two AD8352s (C508)	the external reference clock `Net-(U401-CLK0)`	L3	5.0 mm at 0.28 mm
`IF_TX_B`	`FPGA_PROG_B`	L8	7.7 mm at 0.26 mm

Why it matters. A data bit beside a filter node couples its edges straight into the SDR's baseband. The DAC bus toggles at up to 125 MSPS, and the filter passes everything under 50 MHz.

What was done (12 Nov). Two scripted passes, each kept only at DRC 0/0/0:

- **The widened supply tracks were narrowed again where they ran beside analogue nodes.** That was 64 pieces, cut back to the width that keeps 0.3 mm, but never under 0.3 mm. The widening of §9.1 had brought them closer.
- **Seven tracks were moved 0.15–0.5 mm sideways, with a 45° jog at each end.** Four were aggressors (`ADAR2_CS`, `CONV_SPI_SDIO`, `+2V5`, `+1V8_D`) and three were analogue legs, moved away from `DACS_D0`, `CLK_ADCS_P` and `ADAR2_CS`.

Same-layer run beside analogue nodes	Board of 11 Nov	After the widening	Now
Within 0.3 mm	91 mm	109 mm	**81 mm**
Within 0.2 mm	43 mm	59 mm	**33 mm**

What is left needs parts moved, not tracks. Every case below is where the SDR DAC's filter is threaded between the DAC bus and the `+1V0` feed on L1/L3:

Victim	Aggressor	Run
C814	`+1V0`	13.5 mm at 0.20 mm
C834	`DACS_D0`	11 mm at 0.11 mm
`IF_TX_B`	`FPGA_PROG_B`	7.7 mm at 0.26 mm
C814	`DACS_D4`	4 mm at 0.10 mm
C834	`ADAR2_CS`	3 mm at 0.10 mm

The fix is the one in §9.3: re-place the filter. **Done on 12 Nov (§9.3):** the four filter rows are gone. Other nets within 0.3 mm of the DAC1/DAC2 filter nodes (each node's own partner not counted) went from 59 mm to 14 mm. What is left is `+5V0` beside T801's secondary (5.9 mm at 0.15 mm, unchanged) and the DAC's own `FSADJ` pins next to its outputs.

The external reference input (13 Nov). `Net-(U401-CLK0)`, from the CLK_REF_IN SMA to U401, ran 16 mm beside a 1.0 mm `+5V0` track on L3, 0.26 mm apart: the buck's ripple next to the clock reference. That stretch of `+5V0` feeds only FB601 (the SDR drivers), so it was narrowed to 0.4 mm there: 0.56 mm apart, and `audit.py` no longer lists the pair. The drop to FB601 goes from 3 to 4 mV.

9.3 Long differential analogue paths (the SDR DAC filters re-placed 12-13 Nov)

Path	P / N	Vias
SDR DAC1 filter, between its two inductor sections (C814), before 12 Nov	57 / 66 mm	8 / 6
SDR DAC2 filter (C834), before 12 Nov	39 / 62 mm	4 / 6
SDR DAC1 filter (C814), 12 Nov: re-routed as a pair	51 / 47 mm	3 / 3
SDR DAC1 filter (C814), 13 Nov: re-placed on the bottom face	3 / 1.5 mm	2 / 1
SDR DAC2 filter (C834), now: re-placed	4 / 4 mm	0 / 0
SDR ADC driver → ADC (C605 / C606), simulated 13 Nov, left as it is	45 / 32 mm	4 / 4
Reference oscillator → U401 (Y401 CLK±), before 13 Nov	10.5 / 20.8 mm	3 / 2

Path	P / N	Vias
Reference oscillator → U401, 13 Nov: a coupled 100 Ω pair on L3, legs matched	24 / 24 mm pad to cap	2 / 2

- **The DAC filters.** At 0.4 nH/mm, 60 mm of 0.1 mm track is about 25 nH: a quarter of the filter's own 107 nH coils. The legs also differ by 23 mm, about 160 ps, which unbalances the balun's input.
- **Y401's outputs.** They differed by 10 mm, about 70 ps on the master reference. Re-routed on 13 Nov as a coupled pair on L3 (KiCadRoutingTools' diff-pair router, the 130 Ω pull-downs joined after), the shorter leg meandered by 3.1 mm: the legs now match within 0.3 mm.

These were routed as unrelated nets. The fix is to place the filter parts in two rows beside the DAC and route each pair together.

Done on 12 Nov, DRC 0/0/0 with parity:

- **DAC2 (AD9767 → T802): the filter moved next to its balun.** L831–L834 sit in two rows, one per leg, between J1103 and T802, with C834 between the rows and C835 at T802's pins. The DAC end keeps its loads (R831/R832, C831–C833).
- **What the move changes.** The long copper is now between the 49.9 Ω loads and the first coils, as a coupled 100 Ω pair (0.10 / 0.15 mm, 77 / 84 % coupled, 49 / 46 mm). A matched line there is close to transparent, where the same copper inside the filter added to its coils. Inside the filter each node is under 10 mm, with no vias.
- **Moved for it.** `SW_CTRL0` and `SW_CTRL2`, two static switch controls, were re-routed across the area.
- **DAC1 (AD9767 → T801): the middle node re-routed as a pair, no parts moved.** There is no room for L811/L812 near T801, which is where the second section already is: one free 0603 spot was found. The C814 node now runs as a coupled pair, 83 / 90 % coupled, 51 / 47 mm, with 3 vias a leg instead of 8 / 6. C814's second pad joins its leg through a via placed by hand, beside the pair.

Simulated (12 Nov), and the copper costs little. Each filter was run in ngspice twice: with ideal connections, and with every node's copper as a line of its field-solved Z0 and delay. The balun is taken as ideal.

Filter	−3 dB, ideal / routed	At 100 MHz, ideal / routed	Common mode below differential, 10 / 50 MHz
AD9708 → T701	70 / 67 MHz	−24 / −26 dB	−57 / −36 dB
AD9767 DAC1 → T801	70 / 64 MHz	−24 / −29 dB	−59 / −35 dB
AD9767 DAC2 → T802	70 / 64 MHz	−24 / −29 dB	−47 / −31 dB

- **The passband is unchanged.** It keeps the filter's own ripple of about 2 dB at 30 MHz.
- **The corner moves 4–9 % lower**, and the stop band rolls off slightly faster.
- **The legs' imbalance** leaves a common mode at least 30 dB under the signal inside the passband.

The same simulation after the re-placement:

Filter, as routed	−3 dB, before / now	At 100 MHz	Common mode below differential, 10 / 30 / 50 MHz, before → now
AD9767 DAC1 → T801	64.0 / 64.8 MHz	−29 / −28 dB	−59 / −45 / −35 → −53 / −42 / −35 dB
AD9767 DAC2 → T802	64.0 / 64.0 MHz	−29 / −28 dB	−47 / −36 / −31 → **−68 / −50 / −40 dB**

- **DAC2 gains 9–21 dB of common-mode rejection** across the passband, and the most common mode anywhere below 100 MHz falls from −9 to −19 dB. The corner does not move. The model takes each net's copper as uncoupled lines, so the matched pair's benefit is if anything understated.
- **DAC1 is a trade.** Under 50 MHz its common mode is 3–6 dB worse than before, still under −42 dB to 30 MHz. Above 50 MHz it is better, and the worst below 100 MHz goes from −11 to −18 dB. The corner moves up 1 %.
- **Fewer vias and fewer digital neighbours on both.** A full re-placement of DAC1 needed room near T801 that the top face does not have.

DAC1 re-placed on 13 Nov, on the bottom face. Under T801 the bottom face was free. L811, L812 and C814 now sit there, under L813/L814, so the filter's middle node is 3 / 1.5 mm with 2 / 1 vias (51 / 47 mm and 3 / 3 the day before). As for DAC2, the long copper moved to the DAC side: the outputs run from the AD9767's pins 45/46 (adjacent, 0.5 mm apart) as a pair, 46 / 50 % coupled, the shorter leg meandered so both are 56 mm. `ADAR5_CS` and `ADAR5_TX_LOAD` were re-routed in the box under the parts only. DRC 0/0/0 with parity.

AD9767 DAC1 → T801, as routed	−3 dB	At 100 MHz	Common mode below differential, 10 / 30 / 50 MHz	Worst below 100 MHz
12 Nov (middle node as a pair)	64.8 MHz	−28 dB	−53 / −42 / −35 dB	−18 dB

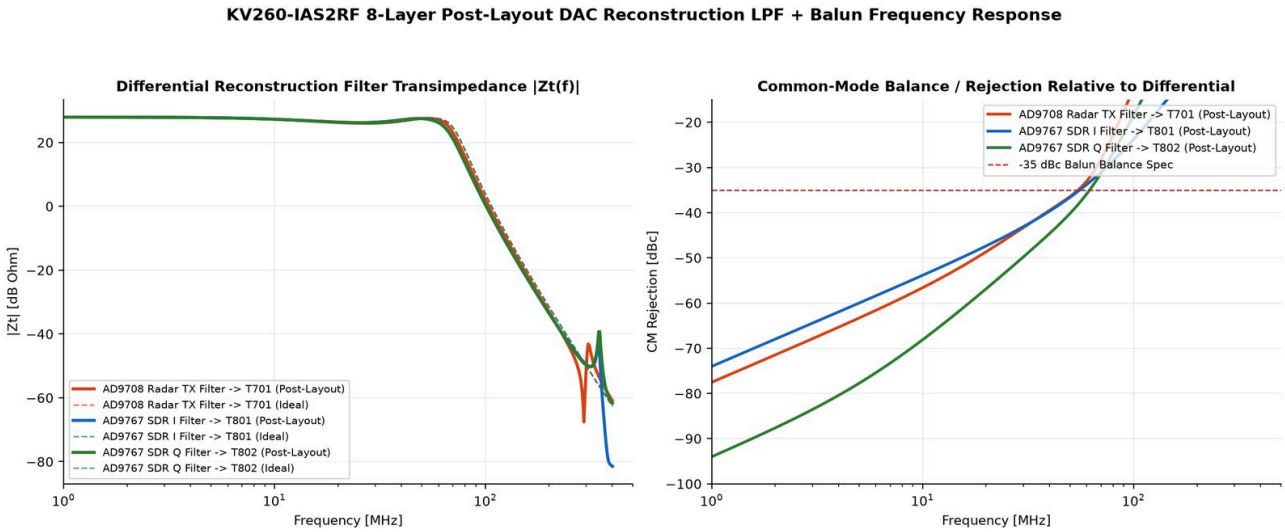
AD9767 DAC1 → T801, as routed	−3 dB	At 100 MHz	Common mode below differential, 10 / 30 / 50 MHz	Worst below 100 MHz
13 Nov (re-placed)	64.0 MHz	−28 dB	**−54 / −43 / −37 dB**	**−24 dB**

- **Better at every frequency than the day before**, by 1–2 dB in the passband and 6 dB at its worst. Against the board of 11 Nov (−59 / −45 / −35 dB) it is 5 dB worse at 10 MHz: what is left is mostly T801's own pins, 5 mm apart, with C815 at one end (13.7 / 4.0 mm of copper on the two secondary nets).
- **Match the legs first.** Before the meander the legs were 56 / 49 mm and the common mode came out 3–4 dB worse than the day before: in this model a leg mismatch costs more than the length.

The SDR ADC's input network, simulated (13 Nov), and left as it is. `adcsim.py` runs the AD8352 → 100 nF → 200 Ω bias → 33 Ω → AD9253 network the same way, with the 45 / 32 mm nodes as routed:

SDR ADC input (U602 → U601 channel A)	1 MHz	10 MHz	30 MHz	62.5 MHz
Gain, routed against ideal	+0.00 dB	+0.01 dB	+0.08 dB	+0.31 dB
Common mode below differential, routed	−90 dB	−70 dB	−58 dB	n/a

At HF the copper is a few nH and pF: it changes nothing the ADC could see. The nodes' only neighbours within 0.3 mm are 2 mm of `+1V8_A` on L3. A re-placement would mean moving parts round the ADC, where both faces are full, for no gain, so it was not done.



DAC reconstruction filters, ideal and as routed, and their common mode before and after the re-placement

The DAC buses are not matched either:

- `DACS` data bits run 37–84 mm, with `IQSEL` at 104 mm;
- `DACR` runs 34–51 mm.

Those 48 mm are about 0.3 ns on an 8 ns period: inside the FPGA's output timing, set by constraints.

9.4 Pairs not coupled: 11 of 22, counting the clocks

§8 counts 19 data and link pairs, of which 10 are not coupled. U401 drives three clock pairs as well. Of those, `CLK_ADCS` and `CLK_FPGA` were coupled on 12 Nov, so 11 of the 22 are still not coupled:

Pair	Coupled	Copper P / N	Vias P / N
`CLK_ADCS`, before 12 Nov	0 %	63 / 67 mm	5 / 6
`CLK_ADCS`, now (below)	**74 / 80 %**	56 / 52 mm of track	2 / 3
`CLK_FPGA`, before 12 Nov	0 %	85 / 71 mm	2 / 5
`CLK_FPGA`, now (below)	**62 / 56 %**	43 / 46 mm, cap to ball	5 / 6
`CLK_ADCR`	36 %	24 / 28 mm	2 / 3
ADCS ×4, ADCR_D2, ADCR_D4	0–41 %	27–43 mm	2–5
LINK_RX_D0/D1, LINK_TX_D0/CLK	0–2 %	71–119 mm	4–9

The order to re-route them in:

1. **The sampling clocks.** Common-mode noise on them becomes jitter.
2. **The ADCS pairs.** The AD9253's P and N pins are adjacent, so the pair can leave the chip together.
3. **LINK.** It needs its AC capacitors at J101 placed together first. It gains least: its eyes are already within 1–52 mV of ideal.

The tool is the one that re-routed ADCR_DCO (from 0 to 89 % coupled), driving KiCad's own push-and-shove router. What coupling buys is common-mode rejection and less crosstalk, not millivolts of eye.

`CLK_ADCS`, re-routed on 12 Nov: now coupled. It runs on L6 (In5) as a 100 Ω pair, 0.10 mm legs with a 0.15 mm gap, from vias in C416/C417's pads to vias in the termination R642's pads.

CLK_ADCS	Before	Now
Layers	P on L1, N on L8, apart	both on L6 for 42 mm, then 4–11 mm to the pins
Coupled (partner within 0.4 mm on the same layer)	0 / 1 %	**74 / 80 %** (41.7 mm)
Track P / N	54.0 / 52.7 mm	56.2 / 51.5 mm
Other nets within 0.3 mm on the same layer	7 nets, 5.0 mm (closest 0.15 mm)	2 nets, 1.1 mm (closest 0.23 mm)

- **How it was done.** KiCad's PNS router could not start from a via in a pad. The diff-pair router of KiCadRoutingTools could, once the pair had two ends: the AD9253's pins were taken off the nets for the routing and put back after. Then the router added the short legs from R642 to the pins (`--keep-input-copper`), on layers other than L6.
- **What is left.** P's leg from R642 to pin 6 goes round C670 and C671 on L1: 11.5 mm against N's 4.6 mm. The 4.7 mm difference is about 30 ps. At a 62.5 MHz clock with 1 ns edges that moves the crossing by about 15 ps, a fixed offset and not jitter. Moving C670 would shorten it, but the pins have no room for it in a 0.5 mm pitch corner already full of supply vias.
- **Checks.** DRC 0/0/0 with parity. No other net changed.

`CLK_FPGA`, re-placed and re-routed on 12 Nov: now coupled. The pad (CONTROL_SPEC §2: 24.9 Ω in series and 24.9 Ω to +1V2 on each leg) had its series resistors 12 mm apart and each shunt 8 mm from its series resistor, so the line from U401 was not terminated in one place.

- **Re-placed.** The four 0402s now sit stacked in the one free column east of the BGA, at x = 168.4: R1116 and R1115 (series, N and P) at y 139.7 and 140.7, R1117 (P shunt) under them at 141.6, R1118 (N shunt) above at 137.8. Each shunt is 1–2 mm from its series resistor. Upright pairs side by side did not fit: the BGA's courtyard ends at x 167.5 and `ADCR_DCO`'s vias sit at x 169.3.
- **Re-routed.** `CLK_FPGA_*` runs from C418/C419 as a coupled 100 Ω pair, mostly on L3 (In2), 62 / 56 % coupled. `FPGA_CLK_*` runs from the pad to balls N11/N12, about 10 mm a leg, and the shunts' +1V2 ends reach the bias node through two vias.

CLK_FPGA	Before	Now
Coupled (partner within 0.4 mm, same layer), C418/C419 to the series resistors	0 / 0 %	**62 / 56 %**
Copper, capacitor to ball, P / N	85 / 71 mm	43 / 46 mm
Pad to ball (the unterminated stub)	13–14 mm, shunts 8 mm off	about 10 mm, shunts 1–2 mm off
Other pairs' legs within 0.25 mm	3.5 mm (LINK_RX_D0_N)	none
Over a void in the reference plane	8.5 mm (`CLK_FPGA_P` over `+3V3_D`)	none

- **How it was done.** As for `CLK_ADCS`: KiCadRoutingTools' diff-pair router for the pair, then its router with `--keep-input-copper` for the short legs and +1V2. That router also moved one far +1V2 track to another layer; it was put back as it was.
- **Checks.** DRC 0/0/0 with parity. Only `CLK_FPGA_*`, `FPGA_CLK_*` and the shunts' +1V2 changed.

9.5 Supply balls without their own via

Unchanged: 11 of 69 (§6). Both ways were tried on every ball, and four of them are on rails with no plane to reach. The impedance is inside the target with margin (+1V0: 41 / 63 mΩ against 120). A further gain needs the BGA's escape redone by hand.

9.6 Thermal, RF budget, and what is still not simulated

Thermal (12 Nov; re-run 13 Nov with the Ethernet PHY, and 17 Nov for Rev08).

- **The model.** `thermal2d.py` treats the board as a 2-D sheet. In-plane conduction runs through each layer's real copper coverage on the Rev08 board: L2, L5 and L7 75 %, L4 70 %, the outer layers 15–23 %, the signal layers 5–7 %. Both faces cool by natural convection.
- **The heat.** 8.2 W, from the power budget (POWER_AND_STACKUP §1.3–1.4), spread over each part's pads. It was 7.5 W before Rev08 (6.9 W until 13 Nov, when the Ethernet PHY added 0.5 W and its load 0.1 W more in the bucks). The GPS receiver of 18 November (`J1503`, POWER_AND_STACKUP §1.3) draws 0.2 W, but in the receiver, off the board; on the board it adds about 0.03 W of buck loss, so the maps below stand. Rev08 adds 0.7 W:
- the RFFC5072, 0.38 W (125 mA at 3.0 V);
- the two SPF5043Z, 0.08 W each;
- the LP5907's drop, 0.05 W;
- the LEDs and I/O expanders, 0.05 W;
- the extra load in the LMR33630, the `+3V3_D` buck and the `+1V8_A` LDO, 0.07 W.

The PHY's θJB is taken as 12 °C/W, typical of a 6 × 6 mm QFN, not read. The RFFC5072's θJB is also taken as 12 °C/W, the figure the enclosure CFD uses, not read.

- **The junctions.** Each is the board temperature under the part plus P × θJB, or θJC for the exposed-pad parts, from the data sheets read.

At 25 °C ambient, still air	h = 10 W/m²K per face (convection only)	h = 15 (with radiation)
Board, mean / hottest rise	+30 / +52 °C	+20 / +40 °C
LMR33630, junction (0.96 W, θJB 13.6)	**87 °C** (board 74)	76 °C
ADCLK948, junction (0.95 W, θJC 8.8 °C/W, Rev. B Table 6)	**85 °C** (board 77)	74 °C
Si549, junction (θJB 17)	78 °C	67 °C
TPS7A8300 for +1V8_D, junction (θJB 12.3)	77 °C	66 °C
RTL8211FSI, the Ethernet PHY (0.5 W, θJB 12 assumed)	71 °C	60 °C
AD9484, junction (θJC 1.7)	71 °C	60 °C
AD9253, junction (0.46 W at most, θJC 7.1, Rev. E Table 7)	66 °C	56 °C
XC7A50T, junction (0.73 W, θJB 8.4, UG475 Table 5-1 FTG256)	65 °C	55 °C
RFFC5072, junction (Rev08, 0.38 W, θJB 12 assumed)	64 °C	53 °C
AD9767, junction (LQFP, only θJA 91 is given)	under 86 °C (board 58 + P × θJA, a bound)	under 76 °C

Re-run with the audited powers (Rev08 audit, 18 November; AUDIT_Rev08.md P6). The table above takes the FPGA at 0.73 W. The re-run takes, at 25 °C typical:

- the FPGA at Vivado's 1.20 W;
- `U1006` at 0.82 W;
- the LMR33630 at 1.17 W;
- the TPS563201 for +3V3_D at 0.65 W;
- the front end at 2.8 V;
- the TCAN3403.

That is 9.4 W in all. The map at the end of this list is that run.

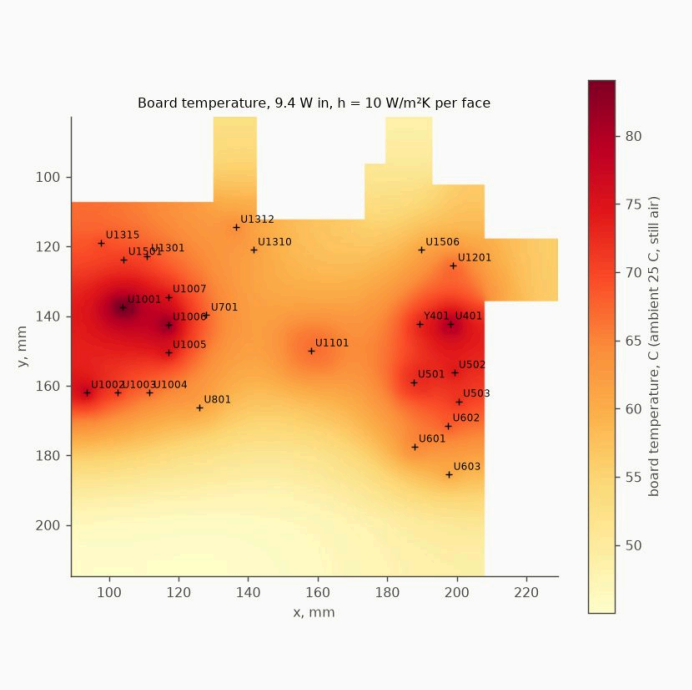
At 25 °C ambient	Still air (h = 10)	Fan only (h = 25)	Before (8.2 W, still air)
Board, hottest / mean rise	+59 / +34 °C	+34 / +14 °C	+52 / +30 °C
LMR33630	**100 °C**	75 °C	87 °C
TPS7A8300 for +1V8_D	92 °C	67 °C	77 °C
ADCLK948	88 °C	64 °C	85 °C
TPS563201 for +3V3_D	88 °C	65 °C	not in the table
Si549	81 °C	58 °C	78 °C
XC7A50T	77 °C	55 °C	65 °C

At 25 °C ambient	Still air (h = 10)	Fan only (h = 25)	Before (8.2 W, still air)
AD9484	74 °C	51 °C	71 °C
RTL8211FSI	74 °C	51 °C	71 °C
RFFC5072	68 °C	45 °C	64 °C

The FPGA's extra 0.5 W shows at its own junction, +12 °C in still air. The power corner gains the most: the LMR33630 and the +1V8_D LDO, +13-15 °C. Bare in still air at 70 °C ambient, the LMR33630 would pass its 125 °C rating, so the vehicle install needs the enclosure's fan and sinks, as below. The enclosure's own rating comes from the CFD re-run with these powers (**ENCLOSURE_V2_THERMAL**), not from this 2-D sheet.

On the bench this is comfortable. In a vehicle it is not.

- **The cause.** The board is small (138 cm²) for 8.2 W. The 12 V buck, the clock buffer, the radar ADC and the four drivers share it. Since Rev08 the buck is the hottest junction, by 2 °C.
- **The arithmetic.** At 60–70 °C ambient, add 35–45 °C to every figure above. Around the clock buffer, the ADCs and the 12 V buck the board then passes 110 °C.
- **What it exceeds.**
- The parts' 85 °C ambient rating: the board under the ADCs and the clock buffer is the ambient they see.
- The FPGA's 100 °C junction limit (I grade): 65 °C on the bench becomes 100–110 °C.
- The ADCLK948 reaches 120–130 °C at the junction, and the LMR33630 122–132 °C. That is under their 150 °C maximum, but outside the ADCLK948's rated range.
- **What a vehicle install needs.** The KV260's fan blowing across this board, or a thermal path to the enclosure, as VEHICLE_PLATFORM plans. At 1 m/s the data sheets' θJA fall by 10–15 %, and the board's h roughly doubles, which halves every rise.
- **The front end is not a hot spot.** The RFFC5072 sits in the free block at 59 °C of board in still air, 18 °C below the clock buffer's corner. Its 85 °C ambient rating is reached at 51 °C ambient in still air; with the fan, at 70 °C the board under it is 85 °C.
- **Not modelled.** Heat flowing into the KV260 through the connector and the standoffs, and any airflow.



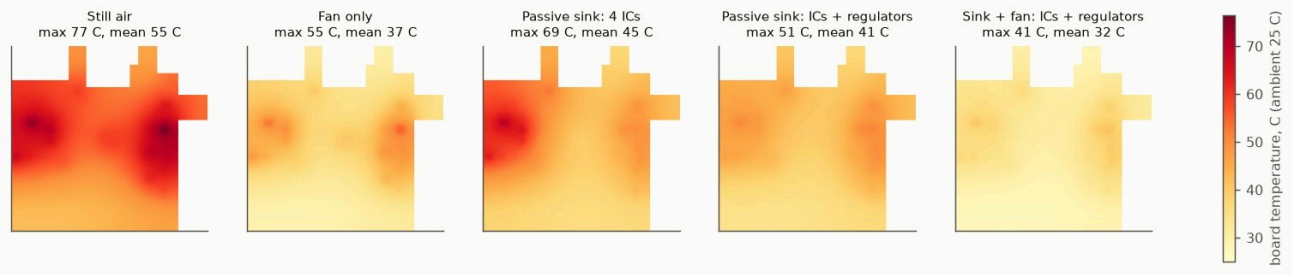
Board temperature

With cooling (12 Nov, re-run 17 Nov for Rev08). `thermal2d.py --sink` adds one heatsink, a node of Rsa °C/W to ambient, pressed onto each listed part's top through θJC(top) and a gap pad (3 W/m·K, 0.5 mm). Each of those parts' heat then splits between the board (through θJB) and the sink, and its junction is solved, not estimated.

- **Fan only.** h = 25 W/m²K per face, roughly 1–2 m/s across the board.
- **Passive sink.** One finned plate about the board's size, Rsa = 3 °C/W in still air.
- **Active sink.** The same plate with a 40 mm fan: Rsa = 0.8 °C/W, and h = 25 on the board.

- **Contacts.** The FPGA 4.8 °C/W (UG475 θJC 4.24 plus the pad). The ADCLK948 27, and the AD9484 and AD9253 18 each (an assumed QFN top θJC of 15–20 plus the pad). The regulators 35–40.

Hottest junction, at 25 °C ambient (and at 70 °C)	Still air	Fan only	Passive sink, 4 ICs	Passive sink, ICs + regulators	Sink + fan, ICs + regulators
Board, max / mean	77 / 55 °C	55 / 37	69 / 45	51 / 41	41 / 32
Hottest part	LMR33630 87 (132)	LMR33630 66 (111)	LMR33630 82 (127)	Si549 and LMR33630 56 (101)	LMR33630 46 (91)
ADCLK948	85 (130)	64 (109)	52 (97)	54 (99)	44 (89)
XC7A50T	65 (110)	46 (91)	38 (83)	40 (85)	31 (76)
AD9484 / AD9253	71 / 66	50 / 47	45 / 42	46 / 43	37 / 34
LMR33630	87 (132)	66 (111)	82 (127)	56 (101)	46 (91)
RTL8211FSI (not under the sink)	71 (116)	51 (96)	55 (100)	56 (101)	45 (90)
RFFC5072 (Rev08, not under the sink)	64 (109)	44 (89)	57 (102)	52 (97)	41 (86)



Board temperature for five ways of cooling it

- **Airflow alone halves every rise.** At 70 °C it brings the FPGA to 91 °C, inside its limit. The board under the clock buffer still reaches about 100 °C.
- **A sink on the four ICs alone leaves the power corner hot.** The 12 V buck stays the hottest part. The sink has to touch the regulators too: the LMR33630, the two TPS7A8300s and the buck (`U1002`, now TPS563201; was TPS562201) that dissipate most.
- **Sink plus fan keeps every junction under 92 °C at 70 °C ambient.** It takes 3.5 of the 8.2 W. The board's hottest spot is then 86 °C, at the parts' 85 °C rating, no longer under it with margin. The PHY and the front end are outside the sink here. Touching the PHY too, or a pad to the RJ45 pedestal of the mount (MECHANICAL), would win that back.
- **Rev08 changed little.** Against the Rev07 board each figure moved by 0–5 °C: the front end's 0.7 W is spread through the free block, away from the clock and power corners.
- **Not modelled.** The contacts' tops are estimates; the ADI data sheets give no θJC(top). The sink is taken as isothermal. Heat into the KV260 is not counted, which errs on the hot side.

RF budget (12 Nov), `cascade.py`. Noise is followed as voltage density node by node:

- the source and its 64.9 Ω termination;
- each AD8352's 2.7 nV/√Hz referred to its input (Rev. C Table 2);
- the ADC's own noise, from its SNR over its Nyquist band.

Radar receive, IF_RX_B → SW2 → AD8352 15 dB → AD8352 10 dB → AD9484	
Full scale at the SMA	**−17.6 dBm** (ADC_RADAR_SPEC estimated −17)
Noise figure, front end only (switch and drivers)	15.5 dB
Noise figure including the ADC	**26.8 dB**: the 8-bit AD9484 is 92 % of the noise
Noise floor at the SMA	−147 dBm/Hz; 47 dB SNR over 200 MHz, plus 12 dB of processing gain after the ÷16 DDC
Input IP3	+15 dBm, 33 dB above full scale

- **The ADC sets the floor.** Its SFDR of 79 dBc, not the drivers' OIP3 of +40 dBm, sets the linearity.
- **More gain here would only move full scale down.** The receiver's sensitivity is decided ahead of this board, in AERIS-10's own IF chain.

SDR receive, AD8352 12 dB → AD9253 (Rev. E, −125 grade: 2 V p-p, SNR 75.2 dBFS at 30.5 MHz, 5.2 kΩ)	`IF_RX_A` (through SW1)	`IF_RX_C`
Full scale at the SMA	**−2.4 dBm**	**−3.0 dBm**
Noise figure, front end only	15.4 dB	14.8 dB
Noise figure including the ADC	**22.4 dB**: the AD9253 is 80 % of the noise	**21.8 dB**
Noise floor at the SMA	−152 dBm/Hz	−152 dBm/Hz
Input IP3	+29 dBm, 31 dB above full scale	+28 dBm

- **The 14-bit ADC still sets the floor.** One AD8352 at 12 dB does not lift the input far enough above the AD9253's own noise. The SNR is taken over the 31.25 MHz Nyquist band of the 62.5 MSPS one-lane mode, taking the ADC's noise voltage as independent of its clock.
- **For weak signals, gain belongs ahead of this board.** The SDR's own LNA must give at least 15–20 dB to bring the system NF below about 5 dB. More gain on this board would only lower full scale.
- **Linearity is set by the ADC too.** The AD9253's SFDR is about 90 dBc, and the driver's IIP3 is 31 dB above full scale.

Transmit, full-scale tone at the SMA	
AD9708, 20 mA, → T701 → SW4 → `IF_TX_B`	**0 dBm**
AD9767 DAC1, 10 mA, → T801 → SW3 → `IF_TX_A`	**−6.1 dBm**
AD9767 DAC2, 10 mA, → T802 → `IF_TX_C`	**−5.5 dBm**

These levels take the 49.9 Ω loads in parallel with the balun's 100 Ω, the balun's 0.4 dB and the switch's 0.6 dB (ADT2-1T+, M3SWA2-34DR+). The filter's passband ripple, 0 to −2 dB, comes on top.

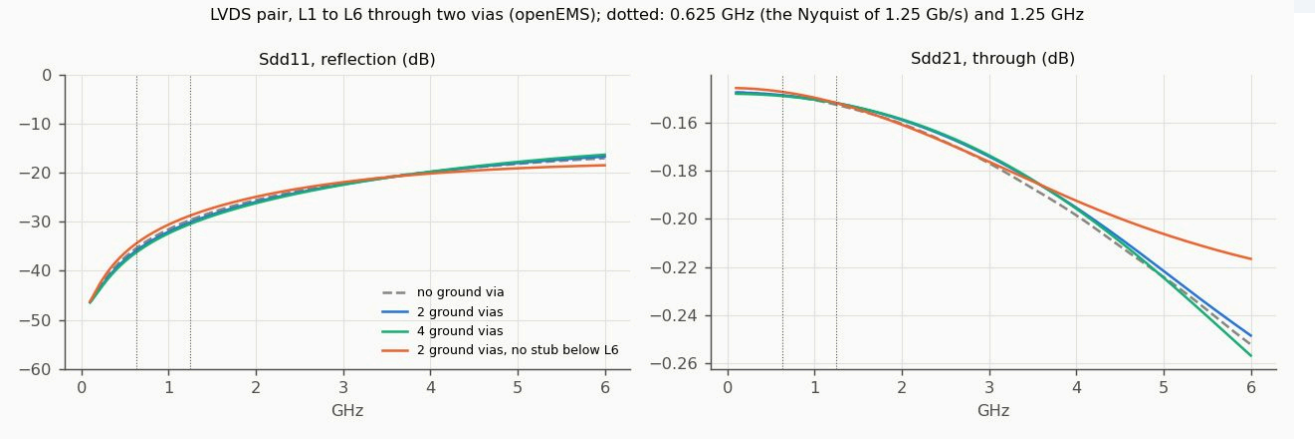
3-D full-wave: the layer change (12 Nov), `layer_change.py`. This is the first of the sub-models. In openEMS, an LVDS pair goes from L1 to L6 the way the board's pairs do:

- the L1 microstrip pair (0.117 / 0.15 mm, 100 Ω) jogs out to two through vias (0.45 / 0.2 mm, 0.75 mm apart);
- it goes on as the L6 stripline pair (0.10 / 0.15 mm);
- each plane has a 0.85 mm antipad round each via, and FR-4 loss is included.

Both ports are driven in odd mode, so the result is the differential S-parameters. Four cases, 3.5 minutes each on the workstation's CPU:

Differential	No ground via	2 ground vias	4 ground vias	2, and no via stub below L6
Sdd11 at 0.625 / 1.25 GHz	−35.5 / −29.6 dB	−36.0 / −30.1	−36.4 / −30.4	−34.5 / −28.7
Sdd11 at 2.5 / 4 GHz	−23.7 / −19.8	−24.0 / −19.8	−24.2 / −19.8	−23.2 / −20.2
Sdd21 at 1.25 GHz (18 mm of line included)	−0.15 dB	−0.15	−0.15	−0.15

- **For the differential signal, the layer change does no harm.** Reflection stays under −29 dB up to 1.25 GHz, the Nyquist of a 2.5 Gb/s lane, more than twice the link's 1 Gb/s. The lumped sections of `lvds_eye.py` were not hiding anything here.
- **Return vias barely matter for the differential mode.** Each leg's return current flows in its partner's via. The ground vias do matter for the common mode and for what leaks into the plane cavity: that is the crosstalk and EMI side, not the eye.
- **The 0.3 mm stub below L6 is negligible** at these rates: under 1 dB of Sdd11 either way, up to 4 GHz.



LVDS pair changing layer, four via arrangements

3-D full-wave: the other sub-models (12 Nov). Same stack, loss and odd-mode ports; each also run in even mode, which gives the mode conversion. They share `stack3d.py`. Three things had to be fixed before the numbers could be trusted:

- **Transverse cells.** Cells over 40 µm across the lines made the absorbing boundary unstable within 1 ns.
- **DC in the excitation.** An excitation with DC left a charge the ports could not drain.
- **Ports on coupled lines.** A port on a line coupled to its neighbour read the neighbour's field as its own wave.

The runs below are after those fixes; each energy trace decays to −40 dB.

BGA escape (`bga_escape.py`): a pair from two adjacent balls, via in pad, out on L6 across three ball columns, then coupled	Sdd11 at 0.625 / 1.25 GHz	Sdd21 at 1.25 GHz	Scd21 (to common mode) at 1.25 GHz
Legs 0.10 mm in the via field (the board's necks)	−30.4 / −24.6 dB	−0.1 dB	−39.7 dB
Legs 0.183 mm (50 Ω) in the via field	−41.9 / −37.1 dB	−0.1 dB	−39.7 dB
Coupled from the vias, one channel (under the 0.15 mm rule)	−38.0 / −34.6 dB	−0.1 dB	−47.1 dB

- **The necks cost 12 dB of return loss and still reflect under −24 dB** at 1.25 GHz: 6 % of the wave at most, on a pair whose eye has 450–650 mV. They are not worth a re-route.
- **The conversion to common mode comes from where the legs meet, not from the necks.** The two legs reach the coupled pair after different jogs, so it is the same with 0.10 or 0.183 mm legs.

Two pairs side by side for 12.6 mm on L6 (`pair_xtalk.py`), the board's worst run (§3.5)	NEXT at 0.625 / 1.25 GHz	Peak for a 300 ps edge: on the pair / on the nearest leg
Legs 1 mm apart (not coupled), 0.15 mm to the other pair (the board)	−32.5 / −27.0 dB	**0.94 % / 1.9 %**
Same, 0.35 mm	−44.2 / −38.6 dB	0.25 % / 0.51 %
Coupled pairs, 0.15 mm	−34.0 / −28.5 dB	0.82 % / 1.9 %
Coupled pairs, 0.35 mm	−46.3 / −40.7 dB	0.20 % / 0.47 %

- **The 2-D estimate of §3.5 was pessimistic by about 3.5 times.** It gave 7 % of the aggressor's swing on the nearest leg; the 3-D model gives 1.9 %, about 7 mV on a 350 mV leg.
- **The far end hardly couples on stripline** (FEXT under −50 dB), as expected with one dielectric round the lines.
- **Spacing matters more than coupling.** 0.35 mm instead of 0.15 mm cuts the crosstalk four times. Coupling the pairs at the same spacing gains only 13 %: at 0.15 mm the victim's far leg is too far off to cancel much.

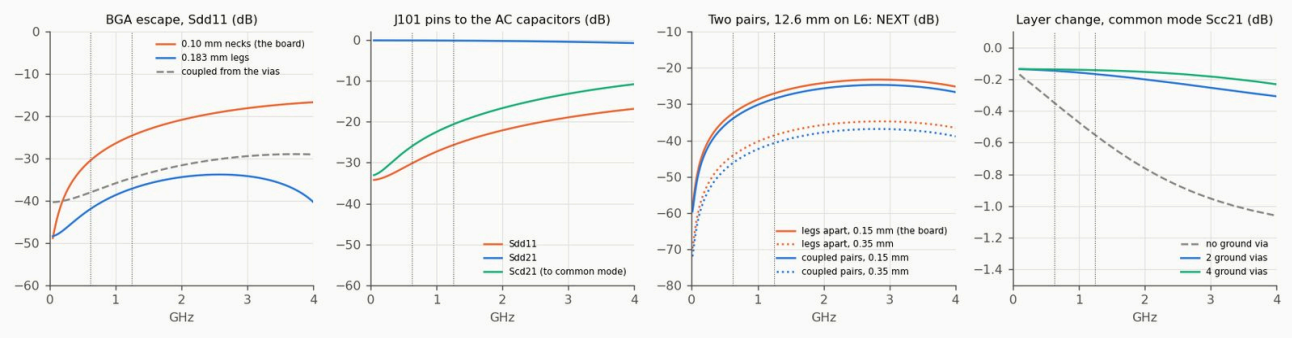
Common mode through the layer change (`layer_change.py even`)	Scc21 at 1.25 GHz	Common-mode power not reflected and not through, at 1.25 GHz	Sdc21, up to 4 GHz
No ground via	−0.55 dB	**7 %** (into the plane cavity, mostly)	under −93 dB
2 ground vias	−0.17 dB	0.9 %	under −89 dB
4 ground vias	−0.14 dB	0.5 %	under −94 dB

- **This is what the return vias are for.** The differential signal did not need them. The common mode does: without them 7 % of its power goes into the cavity between the planes at 1.25 GHz, where it can reach every other via. Two return vias 0.75 mm off bring that to 1 %. Every layer change on the board has a ground via within 3 mm (§5, §8), most of them 1–3 mm off, so the board sits between the two cases; how fast the benefit falls with distance was not run.

- **The symmetric layer change converts nothing between the modes** (Sdc21 under −89 dB).

J101 to the AC capacitors (`hirose_escape.py`), `LINK_RX_D0` as on the board	0.625 GHz	1.25 GHz	2.5 GHz
Sdd11, reflection	−30.2 dB	−25.7 dB	−20.3 dB
Sdd21, through	−0.1 dB	−0.1 dB	−0.3 dB
Scd21, differential turned into common mode	−26.0 dB	**−20.6 dB**	−14.7 dB

- **The modelled path.** The pins are on the bottom, at 0.4 mm pitch, and the capacitors C101/C102 sit right above them on the top. P leaves pin 4 outwards and goes up a via 0.65 mm away. N leaves pin 5 between the two pin rows, at 0.10 mm, and goes round on L1 to C102, 1.5 mm further on. The mating connector is not modelled.
- **For the eye, the footprint is clean.** Reflection stays under −25 dB to 1.25 GHz.
- **It is the link's largest source of common mode.** The legs' different routes turn about 9 % of the differential wave into common mode at 1.25 GHz, and 5 % at 0.625 GHz. The receiver rejects it. J101 mates board to board with the KV260's IAS1 socket, so no cable starts here: the common mode crosses the connector into the carrier's tracks to the SOM, and has no cable to radiate from. (An earlier version of this line said the AERIS-10 ribbon starts here. It does not: that is J1103.) `LINK_RX_CLK` at J101 escapes the same way (one via outside the rows, one between them); the other pairs were not checked.
- **The fix would be the one noted in §9.4 for LINK.** Escape both legs the same way, with the AC capacitors placed together. Both runs (odd and even) give the same conversion, as reciprocity requires: a check on the model.
- **Tried on 13 Nov and not kept.** C105 (`LINK_RX_D1_P`, 9 mm from C106) has a free spot 2.5 mm from C106. Moved there and re-routed, its leg came out 96.3 mm with 8 vias against 95.8 mm and 7, and still leaves the connector by a different path from N. A symmetric escape means redoing the whole J101 escape, ten nets at 0.4 mm pitch, next to the link itself. Since J101 mates board to board, the common mode it makes has no cable to radiate from, so the board was left as it was.



The other 3-D sub-models: BGA escape, J101 to the AC capacitors, two pairs side by side, common mode through the layer change

What is still not simulated:

1. **The 3-D sub-models' S-parameters inside the eye simulation.** `lvds_eye.py` still uses lumped sections; the sub-models above say those were not hiding anything at 1 Gb/s. A cheaper step first is conductor and dielectric loss in its lines.
2. **What the RF budget above leaves out.**
3. The parts' tolerances, run through the filters as a Monte Carlo.
4. The baluns from their manufacturers' S-parameters, not as ideal.
5. The anti-alias networks at the ADC inputs, with their copper.
6. **What the thermal map leaves out.**
7. Airflow.
8. Heat lost into the KV260.
9. A through-thickness model under the hottest parts.

9.7 The Ethernet option's branches on two link pairs (13 November)

The Ethernet PHY shares LINK_RX_D0 and LINK_TX_D0 by fitting parts (CONTROL_SPEC §7). As built, its four coupling capacitors C1218–C1221 are not fitted, so each leg of the two pairs carries an open branch ending on an empty 0402 pad. Each leg was simulated as routed, with the branch added (`lvds_eye.py`'s line model, LVDS driver, 100 Ω and 2 pF a leg at the receiver, PRBS7 at 1.25 Gb/s):

Pair	No branch	As built	Branch
LINK_TX_D0	518 mV, 21 ps	477–484 mV, 18–23 ps	P: C1218 on the top face at (178.9, 98.3), a via in each pad: 0.9 mm of L3 and the via up, about 14 mm from the connector. N: 1.0 mm, about 10 mm from it
LINK_RX_D0	609 mV, 93 ps	601–607 mV, 109 ps	4.3 mm (P) and 5.2 mm (N, 2 vias), near the connector

Where C1218 went (all three simulated the same way):

C1218	LINK_TX_D0 eye	Why not kept
Top face beside R101, 6.6 mm branch	461 mV	the branch
Bottom face on R101's via, only its pad	489–499 mV	over the carrier, 0.8 mm above it: no part may go on the underside there (LAYOUT §1)
Top face below the notch, 0.9 mm of L3 + via (kept, 13 Nov)	**477–484 mV**	n/a

Its tap now sits 3.2 mm further down LINK_TX_D0_P than C1219's on N, so in Ethernet mode the P path is 21.7 ps shorter. ETH_SGRX_PHY_P makes it up with a 3.2 mm bump on L8 (PHY-side P−N +20.9 ps): end to end, PHY to FPGA, the legs match within 1 ps in this model (vias not counted).

In Ethernet mode the paths through the PHY's own pairs measure 350 mV / 50 ps (FPGA to PHY) and 637 mV / 53 ps (PHY to FPGA).

(Individual 1.25 Gb/s SGMII eye plots: `sim/eye_ETH_SGTX_1P25G.png`*,* `sim/eye_ETH_SGRX_1P25G.png`*; all 8-layer eyes in* `sim/eyes_1g.png`*.)* On final `main`, `U1201` (`RTL8211FSI`) moves onto dedicated Bank 34 pins (`R2/R1`, `R3/T2`), eliminating the `C1218–C1221` assembly stubs so both `IAS1` lanes (`LINK_RX_D0/D1`) and `1000BASE-T` operate simultaneously. The PHY's input pair runs beside LINK_RX_D1_N on L1 for 5.2 mm at 0.17 mm; the gateware should hold LINK_RX_D1 static in Ethernet mode.

9.8 Final RF review: limits to know, and what to measure first (15 November)

A last pass over the analogue chains, against the data sheets and the gateware. Nothing here blocks fabrication of the evaluation boards. These are limits of the design as drawn, stated so nobody finds them on the bench.

Point	What it is	Consequence	What to do
No anti-alias filter on the SDR inputs	Between the SMA and the AD9253 there is the AD8352 (flat past 1 GHz) and 2 × 33 Ω with 5 pF, a corner near 480 MHz. The ADC samples at 62.5 MSPS (50 MSPS with the 400 MHz master)	Everything up to several hundred MHz folds into 0–31 MHz at full strength. The FM broadcast band, 88–108 MHz, lands on 17–31 MHz. The wideband path (AD9484, 2 × 24 Ω with 2.7 pF) is the same above its 200 or 250 MHz Nyquist	An external preselector on every receive input: a 30 MHz low-pass for HF, a band-pass for any band taken by undersampling (PMR446 in the second zone of 500 MSPS). It belongs with the LNA the noise budget already asks for (§9.6)
The DAC clocks come from the FPGA	`DACR_CLK` and `DACS_IQCLK` are ODDR outputs of an MMCM clock, as on AERIS-10. The ADCs take the Si549 through the ADCLK948	The clock, not the DAC, sets the transmit noise. The ceiling is −20 log(2π f σ): at 30 MHz, 55 dB for 10 ps rms and 49 dB for 20 ps. That is at the 8-bit AD9708's level and far under the 14-bit AD9767's 86 dB. Close-in, the MMCM's phase noise is the transmitter's	Read the clock's jitter from Vivado's report and measure the SDR output's phase noise. For the radar it is AERIS-10's own arrangement. If a cleaner SDR transmitter is ever wanted, the ADCLK948 has four free outputs (Q4–Q7): an LVPECL-to-CMOS buffer on one of them is a board change
The RF switches below 10 MHz	The M3SWA2-34DR+ (GaAs) is specified from DC, but its data sheet's lowest point is 10 MHz, where P0.1dB is +17.7 dBm and input IP3 +46 dBm (+23.4 and +52 dBm at 1 GHz). Compression falls with frequency	At 1–5 MHz the switch, not the AD8352, may set the receive linearity. The board's levels (−2.4 dBm full scale in, 0 dBm out at most) are 17 dB under the 10 MHz figure, so compression itself is not expected	A two-tone test at 1–5 MHz through SW1 and SW3. `IF_RX_C` and `IF_TX_C` do not pass through a switch and are the reference to compare against
Transmit to receive, on the board	The radar transmits 0 dBm at `IF_TX_B` and its receiver's full scale is −17.6 dBm, with a floor of −147 dBm/Hz. The switches isolate 73 dB or more at 100 MHz; the coupling between the SMA lines and through the supplies was not simulated	Unknown until measured. A leak above −60 dBc would show in the radar's dynamic range	S21 between every transmit and receive SMA on the first board, converters off, then the ADC's spectrum with the DAC running
The transmit outputs are exciter outputs	−6 to 0 dBm after a filter that is −3 dB at 50 MHz and −31 dB at 100 MHz. The image of a 40 MHz tone clocked at 125 MSPS, at 85 MHz, is about 23 dB down in the filter plus the DAC's sinc	Not for an antenna as it is	A power amplifier and a band low-pass filter between the board and any antenna, as the legal notice requires

Point	What it is	Consequence	What to do
Switcher harmonics in the receive band	400 kHz and 580 kHz (POWER_SPEC §2), so harmonics all through MF and HF. The ADC rails are LDO and ferrite filtered	Spurs at those multiples are to be expected at some level	A spectrum of each ADC with its input terminated, as the first receive measurement
Thermal margin at 70 °C	The CFD puts the Si549 at 101.7 °C against 105 °C, and the K26 about 1 °C from its limit (ENCLOSURE_V2_THERMAL)	3 °C is inside the model's error. 70 °C ambient is a target, not a demonstrated rating	Take 60 °C as the working limit until a thermocouple on Y401 says otherwise

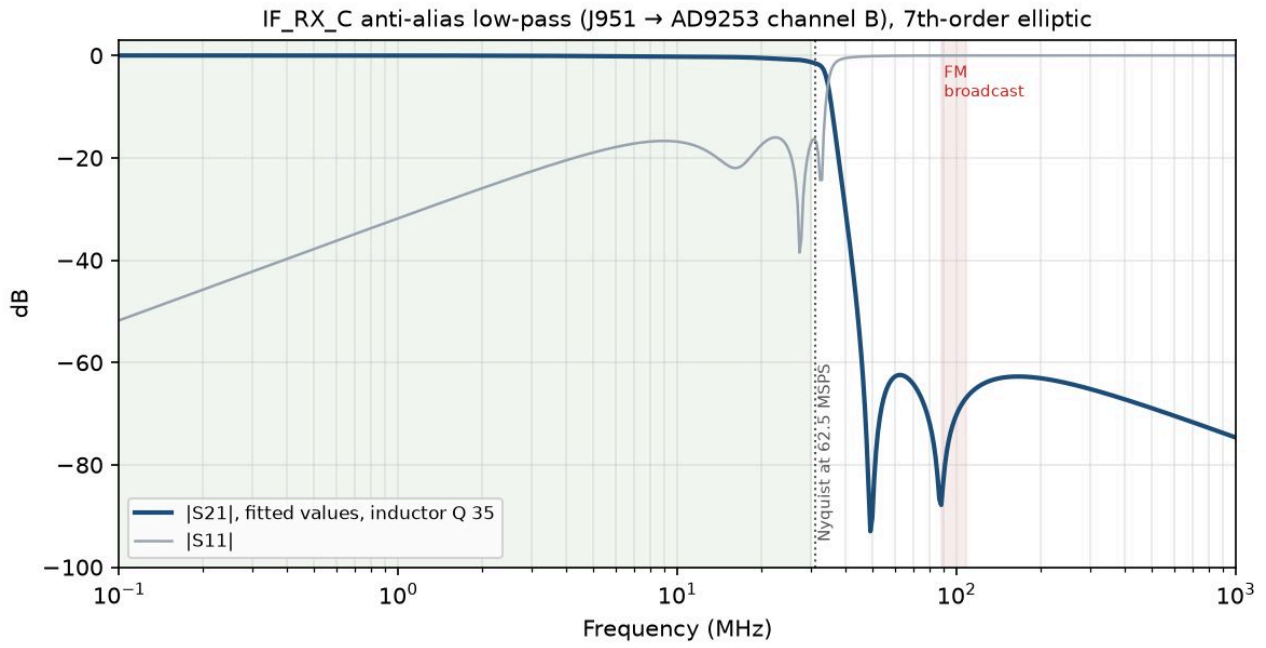
What stands without reservation: the converters' networks follow their data sheets part for part, the clock tree (Si549 into the ADCLK948) is far better than either ADC needs (about 80 dB at the 120 MHz IF for the 120 fs of the Si549 and the buffer together), the SMA launches and the 50 Ω lines are right for the band, every external connector is protected, and ERC, DRC and schematic parity are clean on the board as committed.

9.9 Rev07: what was done about 9.8 (15 November)

1. An anti-alias filter on the HF input (J951, `IF_RX_C`). A 7th-order elliptic low-pass, 50 Ω at both ends, on the board between C951 (the SMA's DC block) and the AD8352, on the straight L1 run of the line (`_work/rev07_aaf.py` for the ROUTING sheet, `_work/rev07_aaf_pcb.py` for the board, values from `_work/sim/aaf_lpf.py`):

Ref	C953	L951 ‖ C954	C955	L952 ‖ C956	C957	L953 ‖ C958	C959
Value	82 p	220 n ‖ 47 p	150 p	270 n ‖ 39 p	160 p	330 n ‖ 10 p	100 p

C0G 0402 capacitors and 0805 wirewound inductors (LQW2BASR22J, SDWL2012CR27G, LQW2BASR33G: 0.7–1.4 Ω, Q about 40 at 30 MHz; the 0603 LQW18AN of the DAC filters have 3.4 Ω and would have cost about 1 dB more).



IF_RX_C anti-alias low-pass

	10 MHz	25 MHz	30 MHz	45 MHz	50–54 MHz	88–108 MHz	146 / 433 MHz
|S21| (fitted values, Q 35)	−0.2 dB	−0.7 dB	−1.3 dB	−55 dB	−68 to −89 dB	−67 to −88 dB	−63 / −68 dB

Monte Carlo over the fitted parts' tolerances (2000 boards: L951 ±5 %, L952/L953 ±2 %, capacitors ±5 % or 0.1 pF, Q 30–45): passband loss 1.7 dB at most, return loss 11 dB or better to 30 MHz, at least 34 dB at 42 MHz and **at least 60 dB from 50 to 600 MHz**. FM broadcast, 6 m and every VHF/UHF service are now 60 dB or more down before they reach the converter. Above about 700 MHz the rejection depends on the parts' parasitics (the capacitors' ESL with their vias, the inductors' self-resonance) and is to be swept on the first board.

What it costs on this input: 0.2–0.7 dB more noise figure and full scale over HF (§9.6: NF 21.8 → about 22.3 dB, full scale −3.0 → about −2.6 dBm at 25 MHz). In the 400 MHz master mode the Nyquist is 25 MHz: 25–30 MHz still folds onto 20–25 MHz there, as before.

Channel A (J911 → SW1 → AD9253) is left wideband on purpose: SW1's other throw brings the radar IF (120 MHz) to the same ADC, sampled in a higher Nyquist zone, which a low-pass would remove. J911, J922 and the radar ports still need an

external preselector when an antenna is connected.

Layout. Four nodes 4.5 mm apart along the line; each shunt capacitor stands on the track with its GND via 0.9 mm above it, each inductor sits in the line, its parallel capacitor above it. The check of point 4 below found `IF_RX_B` running 9.8 mm beside the filter's output at 0.57 mm (−58 dB at 100 MHz, a path round the filter for anything arriving on J921/J922). `IF_RX_B` was moved 2.4 mm away, same length: no same-layer copper within 1.5 mm now. DRC with zones refilled and schematic parity: 0 errors, 0 unconnected, 0 parity problems.

2. The FPGA's clock, and the DAC clocks without an MMCM (gateware). Checking where the DAC clocks come from found a worse problem: the gateware took `CLK_FPGA` as 100 MHz, while the board gives it the 400/500 MHz master through the ADCLK948. Its MMCMs would never have locked. Now (**FPGA_GATEWARE.md**, `fpga/artix/clk_mode_ctrl.v`):

- at power-up the FPGA runs from its own configuration clock (STARTUPE2 CFGMCLK), programs the Si549, sets both MMCMs' input divider through the DRP (÷5 at 500 MHz, ÷4 at 400 MHz), then releases them; the 400/500 MHz switch at run time goes the same way, and the IAS link retrains after it;
- the XDC constrains `CLK_FPGA` at both 400 and 500 MHz;
- `DACR_CLK` and `DACS_IQCLK` come from `CLK_FPGA` ÷ 4 (100 / 125 MHz) through a BUFG, no MMCM: Vivado's clock uncertainty on them falls from 0.165 to 0.035 ns, with no MMCM discrete jitter or phase error left. What is left is the master's own jitter and the FPGA's output buffer, to be measured as 9.8 says;
- with Ethernet on, the GPS discipline of the Si549 is clamped to ±50 ppm (SGMII needs ±100 ppm).

Vivado 2026.1, both builds (Rev08 phase 1 re-run): WNS +0.071 ns, WHS +0.014 ns, pulse width +0.008 ns, no failing endpoint; the AD9484 radar domain is closed at 400 MSPS only and held in reset in 500 MHz mode. Every bench passes at 400 and at 500 MHz, `tb_system` included (S1–S6 with Ethernet and IAS1), re-run independently; the clamp's mutation fails as it should.

3. HF on the inputs and outputs without a switch. J951 (`IF_RX_C`, now filtered) and J952 (`IF_TX_C`, DAC2) have no RF switch in their path, so the GaAs switch's behaviour below 10 MHz does not touch them. They are the board's HF receive and transmit ports; the gateware makes channel B and DAC2 the SDR's default channels. J911 and J931 still reach the same converters through SW1 and SW3, for use above HF or to compare. The two-tone test of 9.8 stays on the first board's list, to know what SW1/SW3 do at 1–5 MHz.

4. Transmit to receive. `_work/sim/txrx_isolation.py` walks every receive line's copper and looks for transmit or clock copper on the same layer (lines on different layers are screened by a ground plane 0.12–0.13 mm away): within 1.5 mm, it integrates the field-solver coupling of §3.5 along the run.

Receive line	Same-layer transmit copper within 1.5 mm	Clock copper within 1.5 mm
`IF_RX_A` (SW1, AD9253 ch A)	none	none
`IF_RX_B` (SW2, AD9484)	none	`CLK_REF_IN`, 0.4 mm at 1.1 mm on L3: about −100 dB at 120 MHz
`IF_RX_C` (filter, AD9253 ch B)	none	none

So the board's tracks are not the leak path: at 0 dBm out, a track coupling of −100 dB is far under the radar receiver's floor. What is left for the measurement is what the script cannot see: radiation between the SMAs (8.5 mm apart, edge-mounted, each with its ground vias), coupling through the shared −3V3/+3V3 switch supplies, and the converters' own feedthrough. The measurement is unchanged: S21 TX SMA → RX SMA on the first board, converters off, then the radar ADC's spectrum with the chirp running.

5. Thermal margin (the 15 November upgrade and Rev08 audit P6, ENCLOSURE_V2_THERMAL §7–§8). The Si549's limit in 9.8 was wrong: its junction limit is 125 °C and its rating is 85 °C *ambient* (data sheet Tables 2.1 and 2.6), so at 70 °C its junction had 20 °C to spare. The real limit is the KV260 itself: its SOM is the commercial K26C, 85 °C junction (UG1090). Enclosure v2 has a 50 × 50 × 15 mm fan, nine more exhaust slots in the back wall and taller heatsinks (ENCLOSURE.md §6). Fine-mesh CFD with the real Vivado `XC7A50T` power (`1.249 / 1.604 W` upper bound) and audited regulator losses (`U1006 = 0.91 W`, `U1002 TPS563201 = 0.69 W`): **55.9 °C ambient with the stock KV260, 62.5 °C by the adapter's `TA` parts (`Tb <= 85 °C`), and 68.2 °C with an industrial K26I SOM** without `HS4` (`XC7A50T` hits `101.81 °C` at 70 °C). With Rev08's front end, camera and **`HS4` fitted on `U1101`**: **56.1, 63.3 and 70.9 °C** (`XC7A50T` drops from `102.08 °C` to `93.38 °C` clean / `94.24 °C` clogged at 70 °C; `68.0 °C` K26I without `HS4`; ENCLOSURE_V2_THERMAL §8).

9.10 Rev08: the VHF/UHF front end's copper (phase 6, 17 November)

REV08_PLAN section 11, phase 6 and gate G3: the new copper of phase 5 simulated with the method of 9.9. Every check below ran on a copy of the board with the zones refilled (the board in git keeps its zones unfilled, as FABRICATION says;

`make_fab.py` fills them on its own copy).

1. Coupling into the converters and the clock tree (G3). `_work/sim/txrx_isolation.py` now also takes the front end's copper as aggressors: the RFFC5072's mixer ports (which carry its LO leakage), its reference, the IF chain from the mixer to `IF_VU` (the 142.3 mm L6 stripline to SW2), the preselector link `VU_PSB_OUT` and the USB pair. As victims, it takes both converters' inputs (the `IF_RX` lines, the AD8352 driver nets and the ADC VIN nets), `IF_VU` itself and the clock tree (Si549, ADCLK948, the ADC and FPGA clock pairs). It adds 1.1 GHz to the frequencies, caps the in-phase sum at the run's largest Kb, and lists aggressor vias within 1.0 mm of a victim's track on any layer.

Front-end aggressor	Same-layer copper within 1.5 mm of an ADC input or a clock net	Aggressor via within 1.0 mm	Closest approach, any layer
LO (RFFC5072 mixer ports)	none	none	8.7 mm to `IF_VU`; 29.8 mm to `CLK_FPGA`, 57.8 mm to the AD9484 drivers
RFFC5072 reference (TCXO)	none	none	18.0 mm to `IF_VU`
IF chain (anti-alias, IF amplifier, PE4312)	none	none	23.6 mm to `CLK_FPGA`
IF line `IF_VU` (L6)	none	none	crosses `IF_RX_A/B/C` on other layers; 5.5 mm from the ADCLK948's nets
`VU_PSB_OUT`	none	none	15.0 mm to `IF_VU`
USB (`J104` to the CH340X)	none	none	28.4 mm to `IF_VU`

Where `IF_VU` crosses the `IF_RX` lines it is on L6 and they are on L1 or L8: L5 and L7 are solid ground along all of `IF_VU`'s 142.3 mm except 0.9 mm at its own via by SW2. Into `IF_VU` itself, the only items within 1.0 mm are two vias that cross L6: the radar chirp's (`IF_TX_B`, 0.87 mm) and a DAC output's ahead of its filter (0.57 mm). Both were already placed so in phase 5 (2W from L6 copper), and a via is a short vertical, not a parallel run.

G3: passed. No LO, reference, IF or USB copper runs on the same layer within 1.5 mm of either converter's input or of the clock tree, and no front-end via comes within 1.0 mm of them. The track model therefore gives nothing to add to the Rev07 figure (`CLK_REF_IN` into `IF_RX_B`, −102 dB at 120 MHz, which the script still reproduces). The front end's coupling into the ADCs is below that figure. What the script cannot see is the same as in 9.9: radiation inside the box, the supplies, and the parts' own feedthrough. The frames and the front end's own LDO are there for those, and the first board's spectrum (LO on, antenna terminated) is the measurement.

`VU_PSB_OUT` (0.12 mm, 21.2 mm on L3 and 9.1 mm on L6, preselector B to A up to 1.1 GHz): 55.2 ohm by the field solver of 3.5 (0.151 mm would give 50.1 ohm). The 10 % mismatch over 30 mm costs under 0.05 dB and a return loss of about 26 dB at 1.1 GHz. It is left as drawn. Its reference planes are solid except at its own three vias.

2. `J961`'s launch. The phase 5 copper already had the L2-L6 cut-out under the signal pad (keep-outs on In1-In5, x 89-93, y 120.25-122.35), so the pad references L7, as under J921. What the other twelve SMAs have and `J961` did not:

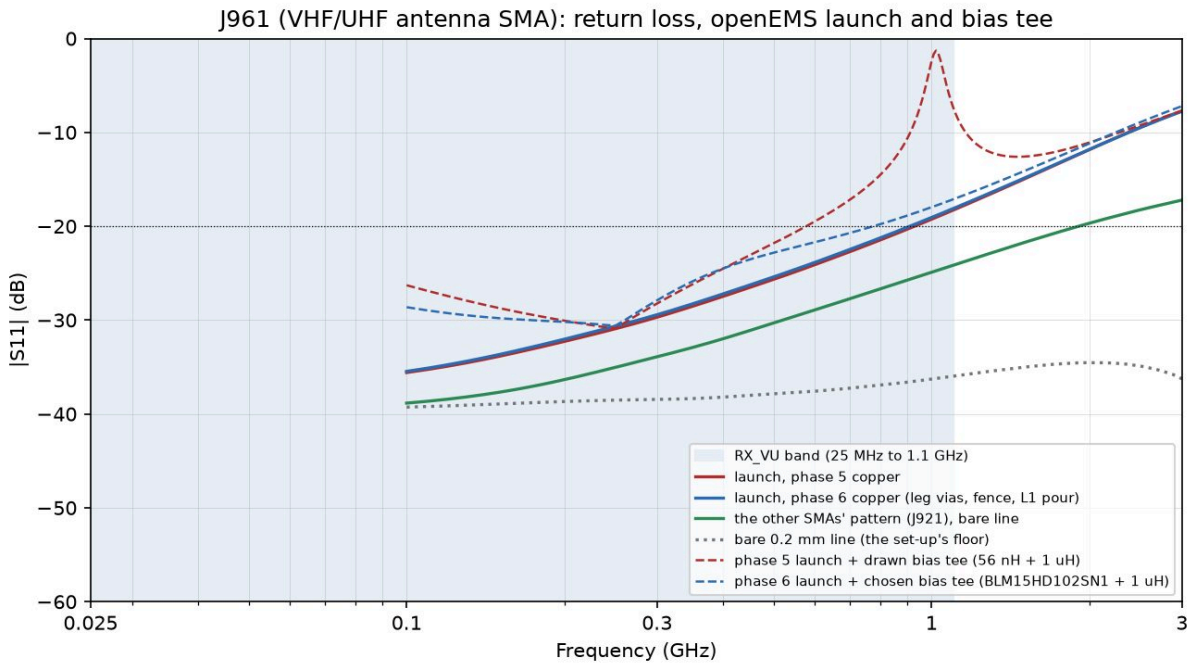
- an L1 ground pour around the line;
- three ground vias in each leg (it had one, at the edge);
- a via fence along the line.

Added, as text edits of the board (no router; nothing else's copper moved, checked zone by zone after the refill):

- six vias in the legs (x 90.5, 91.5, 92.5);
- fence vias at (93.3, 120.5), (93.3, 122.1) and (95.25, 122.1), the last on D1301's ground, which had no via;
- the pour "L1 VU_ANT GND" (0.5 mm clearance, as the RF band's) on the legs and south of the line.

North of the line past x 94 there is no room for vias: `U1315` and a LED track sit under it on B.Cu.

`_work/sim/j961_launch.py` (openEMS, the 8-layer stack, 0.1-3 GHz) models the launch with the parts on the line: D1301 0.5 pF, the bias tee's pad, and C1301 as a through.

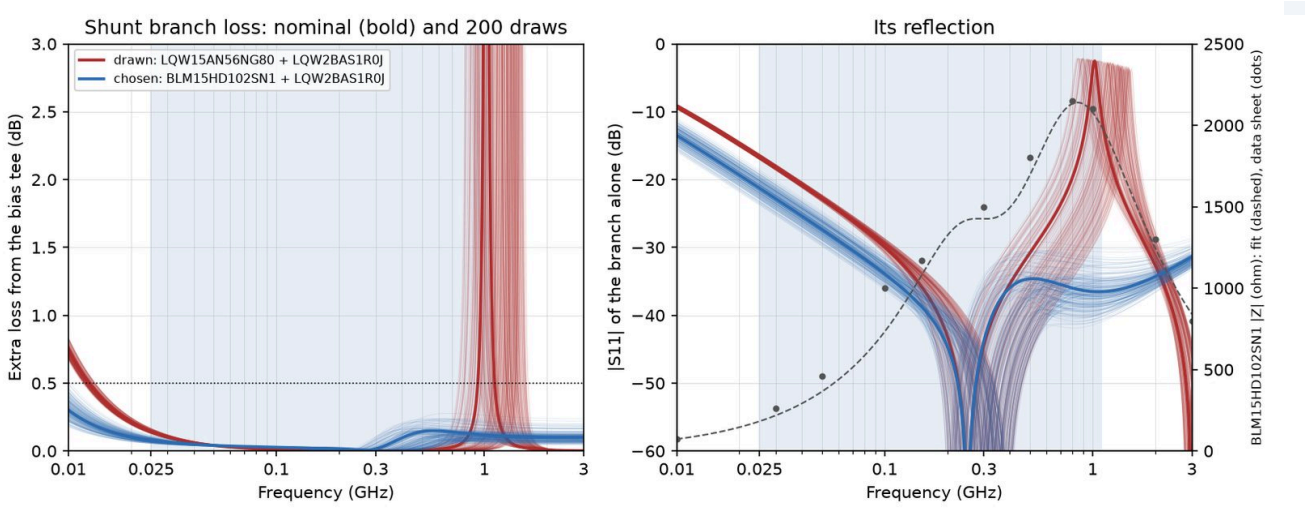


J961: return loss

|S11|	100 MHz	300 MHz	500 MHz	1.0 GHz	1.1 GHz	2.0 GHz
Phase 5 copper	−35.6 dB	−29.7 dB	−25.7 dB	−19.3 dB	−18.3 dB	−11.8 dB
Phase 6 copper	−35.5 dB	−29.4 dB	−25.4 dB	−19.1 dB	−18.1 dB	−11.8 dB
The other SMAs' pattern (J921), bare line	−38.8 dB	−33.9 dB	−30.3 dB	−24.9 dB	−24.2 dB	−19.7 dB
Bare 0.2 mm line (the set-up's floor)	−39.3 dB	−38.5 dB	−37.8 dB	−36.3 dB	−36.0 dB	−34.5 dB

All four runs are stable (the model's margins keep every via out of the absorbing boundary). The phase 6 copper returns the same |S11| as the phase 5 copper, within 0.3 dB: what the legs, the fence and the pour bring is the return path and the shielding of the other SMAs, not a better match. Both stay 6 dB above J921's pattern because of the parts on the line, not the launch: D1301's 0.5 pF alone is a 21 dB reflection at 1.1 GHz (ωCZ0 = 0.17), and the bias tee's and C1301's pads add the rest. The worst in the band is −18.1 dB at 1.1 GHz, a mismatch loss of 0.07 dB, and |S21| is −0.28 dB there. With the bias tee added (dashed in the figure, the two reflections summed in magnitude, the worst case of their phases), the drawn 56 nH + 1 µH alone reflected −3.8 dB at 1 GHz and took the total near 0 dB; the chosen branch reflects −34 dB or less above 500 MHz and moves the total by under 1 dB (−17.1 dB at 1.1 GHz). The SMA's own body is not in the model, the same for every case.

3. The bias tee, and the same fault on the LNA. The bias tee's shunt branch hangs across the antenna line: whatever it fails to block is lost. As drawn, it was a 56 nH (`L1302`, LQW15AN, self-resonance ≥ 2.8 GHz) in series with a 1 µH (`L1301`, 0805). Past its own self-resonance (≥ 200 MHz for the 0805 wirewound) the 1 µH is a capacitor of 0.16-0.63 pF, and with the 56 nH it makes a series resonance at 0.85-1.7 GHz: a short across the antenna line. The parts' data, the models and the Monte Carlo are in `_work/sim/bias_tee.py`. The ferrite bead's impedance curve is fitted from Murata's data sheet; at the bias current it is derated to 40-100 % on top of its ±25 % tolerance.



Bias tee: loss and reflection

Shunt branch (25 MHz-1.1 GHz, 3,000 draws)	Nominal	p99	Worst	Where
As drawn: 56 nH + 1 µH	12.0 dB	13.3 dB	13.7 dB	0.84-1.1 GHz
Now: FB1302 BLM15HD102SN1 + L1301 LQW2BAS1R0J	**0.15 dB**	**0.24 dB**	**0.30 dB**	560 MHz
Bead + 1 µH power inductor (rejected)	0.25 dB	0.88 dB	1.13 dB	135 MHz
Bead alone (rejected)	0.31 dB	0.91 dB	1.07 dB	25 MHz

The 56 nH's place takes a 0402 GHz ferrite bead. Above 150 MHz it is a resistor of 1-2 kohm, so the branch can no longer resonate, and below 150 MHz the 1 µH carries the impedance (157 ohm at 25 MHz). The parts use the same pads, so no copper changed. The bead is rated 250 mA and the AP22652 limits the bias to 155 mA. The two inductors' resistance (1.25 + 2.4 ohm) drops 0.6 V at the limit. The BOM rules name the two parts (`lcsc_select.py`: C21516 and C333860, in stock on 17 November). A value match would not do: a BLM21BD-type bead or a 1 µH power inductor would bring the dip back (third row).

The same sweep over every choke on an RF line in `RX_VU` found the pattern once more, worse, at the LNA's output. The SPF5043Z's drain feed was `L1304` (56 nH) from the output to a node that `C1305` (100 pF) took to ground. A 56 nH in series with 100 pF is a short at 67 MHz, right on the LNA's output:

LNA output, shunt branch	30 MHz	67 MHz	88 MHz	100 MHz	150 MHz	Worst, 25 MHz-1.1 GHz (3,000 draws)
As drawn: 56 nH, 100 pF to ground, 1 µH to the rail	0.8 dB	21 dB	7.4 dB	4.7 dB	1.5 dB	22.6 dB at 69 MHz
Now: FB1304 BLM15HD102SN1, C1305 not fitted, L1303 1 µH	0.06 dB	0.03 dB	0.03 dB	0.03 dB	0.02 dB	**0.23 dB**

The IF amplifier's choke `L1305` (1 µH straight to `+3V0_RF`, now `+2V8_RF`) has no series capacitor. The rail's 100 nF puts its series resonance near 0.5 MHz, so over the IF band (25-170 MHz) it costs 0.31 dB at most and is left as it is. The filters' inductors are the filters (`rev08_filters_mc.py`). The 0603 1 µH of `L1303` and `L1305` gets its own BOM rule, AHW1608F-1R0KTF (SRF 400 MHz, 330 mA).

4. Checks. The board is changed by text edits (5 property lines, 9 vias, 1 zone). On a copy with the zones refilled, DRC with schematic parity gives **0 errors, 0 unconnected, 0 parity errors**. The 35 warnings are the 36 of before less one dangling stub, which the pour now covers. ERC: the same 7 pin-to-pin warnings. `check_sheet.py rx_vu`: PASS. After the refill, the zone fills differ from those of the unchanged board only around `J961`: the new pour, and the antipads of the nine vias on L4.

10. How it was checked

The checks were scripts run on the board file, none by hand: a KiCad-style plane fill, the connectivity graph of each net, the field solver, ngspice and openEMS (built from source in WSL). The DRC after every change: **0 errors, 0 unconnected, 0 schematic-parity problems** (on 12 Nov, for the 8-layer board, 0 violations of any kind).

Source: docs/AUDIT_Rev08.md

Rev08 audit: RF and power, before the tag

18 November 2026 · audited on `main` *at* `6df5766`*, fixed the same day; re-audited on 19 November (section 5); ground offset addendum the same day (section 6) · scripts* `_work/sim/rev08_rf_audit.py`*,* `_work/power/power_audit.py`*,* `_work/power_budget.py`*,* `_work/rev08_audit_sch.py`*,* `_work/rev08_audit_pcb.py` *· figures and data in* **`docs/sim/`**

A last pass over the whole board as an RF engineer would make it before ordering. It covers the receive and transmit chains from HF to 3 GHz and the clocks. It also covers the power tree: what each part gets, what each regulator carries and what the vehicle can do to the input, so that nothing on the board can be damaged. Every finding was then fixed. This page records both: what was found, with its numbers, and what changed.

The simulations already in the repository are reused where they apply. Three things are new:

- the Vivado power report of the routed FPGA;
- a study of the converter's preselection, now with the high-pass that fixes it;
- a power audit with eight checks, including time-domain simulations of the start-up and of the ISO 7637-2 and ISO 16750-2 pulses.

The reused simulations are:

- the SMA and `J961` launches (openEMS), the eyes and the skew, the PDN impedance;
- the filters' Monte Carlo, the bias tee and the LNA chokes;
- the transmit-to-receive isolation (G3) and the thermal maps;
- the gateware's end-to-end benches (`tb_system`, `tb_e2e`) and the G-8 synthetic campaign.

Marks as elsewhere: `[V]` from a data sheet or a tool run on the design, `[E]` an engineering estimate.

0. Verdict

Before the fixes. The analogue chains, the clocks and the SMA launches stood. No rail could exceed an absolute maximum, and the input stage survived every ISO 7637-2 pulse, the suppressed load dump, a jump start and reverse battery. But the audit found:

- three ways to damage something;
- one design gap in the new VHF/UHF converter;
- a power budget short by 0.3 A at 12 V. It had left out four loads and estimated the FPGA's VCCAUX at a quarter of what Vivado reports.

After the fixes. Every finding below is closed on the board, in the BOM or in the gateware, or is left as a stated bench check. On the board as committed:

- DRC with schematic parity gives the same report as before the edits, and ERC the same 7 warnings (LAYOUT 6.9);
- `make_fab.py` gives 0 errors and 0 unrouted;
- the board files are reproduced by `rev08_audit_pcb.py` from the audited commit, UUIDs aside.

#	Finding	Severity	Fix	Where
P1	`U1506` TCAN330: CANH/CANL absolute maximum ±14 V. A CAN wire shorted to the battery (13.8-14.8 V while charging, 24 V on a jump start) destroys it; `D1531` PESD1CAN does not conduct below 24 V	Damage	**TCAN3403DDFRQ1** (±58 V bus fault, 3.3 V, SOT-23-8). Pin 5 is VIO, so it moved from ground to +3V3_D	Schematic, BOM, a 0.25 mm stub
P2	The Pmod back-powers whichever board is off: eight 3.3 V lines with 0 Ω at both ends (the KV260's R276-R283), up to about 100 mA a line into the unpowered FPGA's clamp diodes	Damage (latent)	**Gateware on both FPGAs**. The Artix drives `PMOD_MISO` only while a Kria is present, and `PMOD_SPARE2` (the debug UART) open-drain. The K26 keeps its Pmod outputs high-Z until the adapter is alive	Gateware; no copper (the lines run as a 0.2-0.3 mm bus with no room for resistors)
P2b	The GPS PPS into an unpowered K26 through 220 Ω: 11 mA while the pulse is high	Damage (latent)	`R1542`/`R1543` 330 Ω: 7.6 mA	BOM

#	Finding	Severity	Fix	Where
P2c	`FPGA_IRQ`, push-pull 1.8 V into the K26's HPA bank: up to about 48 mA while an alert holds it high with the KV260 off	Damage (latent)	Gateware: driven only once the IAS1 link has trained	Gateware
P3	`F1001` (PTC, 1.5 A hold) trips in a hot car: 1.12 A worst case at 12 V, 1.28 A at 10.5 V, against 1.15 A held at 56 °C	Function (resets)	**mSMD200-24V, 2.0 A hold**, same 1812 footprint: worst case trips above 84 °C at 12 V and 73 °C at 10.5 V. A 2920 part does not fit	BOM
P4	`U1006` (+1V8_D LDO) dissipates 0.91-0.94 W, not 0.50 W: VCCAUX is 0.31-0.37 A (Vivado), not 0.1 A. Through its single path to the balls (184-263 mΩ, SI 4.4), VCCAUX could sag to 1.665 V against 1.71 V	Margin	**+1V8_D at 1.85 V** (the 50 mV ANY-OUT pin grounded, as on `U1005`): VCCAUX 1.714-1.873 V at the balls. The LDO keeps its 0.91 W, checked in the CFD (P6)	Schematic, a 0.2 mm stub
P5	+3V3_D carries 1.78-1.89 A from a 2 A TPS562201 (89-95 %)	Margin	**`U1002` TPS563201**: 3 A, pin for pin, with the same divider and inductor (63 %)	BOM
R1	**The converter has no IF rejection.** The UHF image filter is a low-pass, so 30-480 MHz reached the mixer, the 100-170 MHz IF window included (≤ 0.4 dB). FM broadcast, airband, 2 m, marine VHF and PMR leaked through the mixer onto the UHF tuning; the 1 GHz low-pass path did the same for 480-1000 MHz	**Design gap**	**A 300 MHz high-pass ahead of preselector B** (5th-order elliptic, seven 0402 parts in frame A). IF rejection goes from 31-46 dB to 84-99 dB. Converted coverage now starts at 300 MHz	Schematic, board (LAYOUT 6.9)
P6	The thermal model and the CFD took the FPGA at 0.73 W; Vivado gives 1.20 W at 25 °C and 1.55 W at 70 °C, maximum process	Margin	**CFD re-run** with 1.25 / 1.60 W (an upper bound: the industrial grade gives 1.22 / 1.45 W) and the new regulator losses. At 70 °C the XC7A50T reaches 102.1 °C without `HS4` (limit 100 °C) and **93.4 °C with it**. The enclosure's rating stays **63.3 °C**, set by `U401`'s board temperature, and there the XC7A50T is about 95 °C without `HS4`. **Fit `HS4` in a vehicle**: it is required above 68 °C with a K26I (**ENCLOSURE_V2_THERMAL** section 8)	Simulation; `HS4` in the assembly notes
P7	VCCINT, VCCO and the 3.3 V parts' ±5 % windows were met nominally but not in the worst-case linear stack (the TPS562201's reference is ±2.5 % over temperature)	Note	`R1031` 3.24 k: +1V0 at 1.017 V, so the balls sit at 0.983 V at full load. Root-sum-square inside every window; measure each rail on the first board (the XADC reads VCCINT)	BOM
P8	`U1315` (+3V0_RF) could reach dropout at the worst corner (26 mV of headroom against 180 mV), letting the 580 kHz ripple of +3V3_D onto the RFFC5072's supply	Note	**LP5907MFX-2.8**: the rail is `+2V8_RF`, with 232 mV of headroom at the worst corner	BOM, net rename
R2-R8	Half-IF response, LO leakage, the TCXO's pin 1, the bias tee against the antenna TVS, no limiter on `J961`, floating switch controls at power-up	Notes	Section 1.3; R3 by gateware	Mostly none

1. RF

1.1 What stands (reused simulations)

Chain or item	Evidence	Result
SMA launches (12) and `J961`	openEMS, SI 2.1 and 9.10	Return loss ≥ 39 dB at 500 MHz on the twelve; `J961` −18.1 dB at 1.1 GHz (0.07 dB mismatch loss)
HF input `IF_RX_C`	Rev07 anti-alias filter, Monte Carlo (SI 9.9)	≥ 60 dB from 50 to 600 MHz, ≤ 1.7 dB in band
VHF/UHF filters with catalogue parts	`rev08_filters_mc.py`, 2,000 runs each	All four pass their masks at p1/p99 (REV08_PLAN 5.4)
Bias tee and LNA drain feed	`bias_tee.py` (SI 9.10)	≤ 0.30 dB and ≤ 0.23 dB from 25 MHz to 1.1 GHz, no resonance
Coupling into converters and clocks	`txrx_isolation.py`, gate G3	No LO, reference, IF or USB copper within 1.5 mm on the same layer; worst track coupling −102 dB
Converter cascade	`rev08_frontend.py`	NF 2.0 dB direct, 3.7 dB UHF, 7.1 dB ADS-B; full scale −52 to +2 dBm. The high-pass adds 1.1-1.5 dB ahead of the mixer, after the LNA's 22 dB: about 0.1 dB of NF
Clock tree	SI 9.8	Si549 + ADCLK948 ≈ 120 fs, about 80 dB SNR ceiling at a 120 MHz IF
Link, Ethernet, PDN	SI 3, 4, 9.7	Eyes open at 1 and 1.25 Gb/s; VCCINT under target to 100 MHz

Chain or item	Evidence	Result
End to end	`tb_system` S1-S7 at 400 and 500 MHz, `tb_e2e`, G-8 campaign (FPGA_GATEWARE)	Pass, with their mutations failing as they should

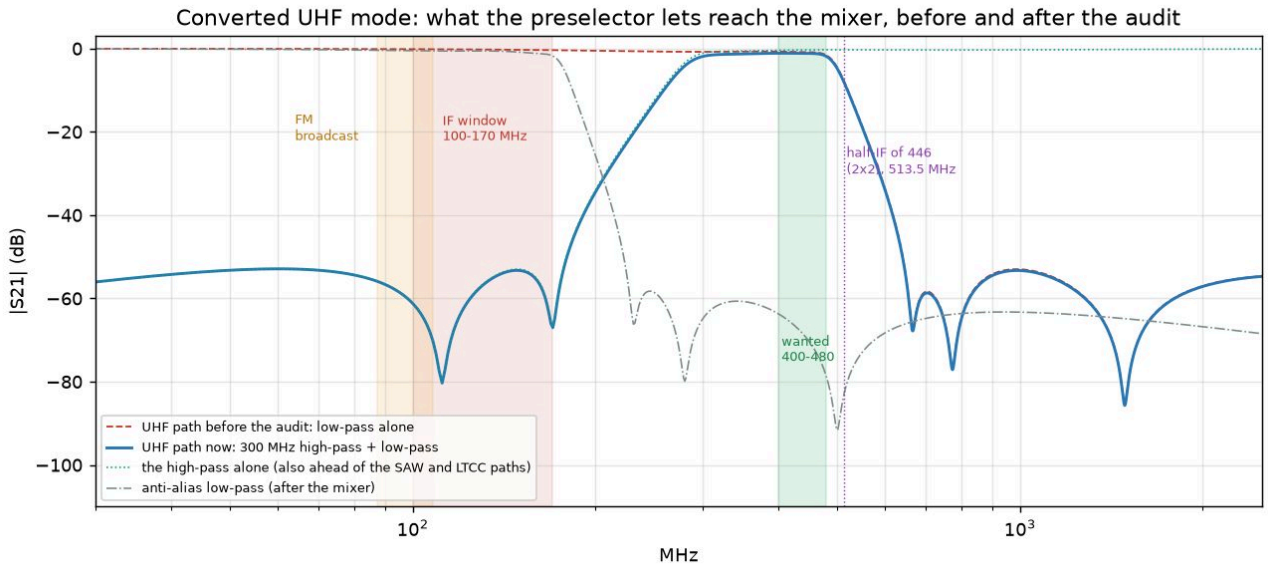
The pin-outs were checked again in this pass against:

- the RFFC5072's data sheet (DS140110 pin table and the wideband application schematic, p.13);
- both baluns: the TC4-1W+ secondary with its centre tap to the mixer (200 Ω), and the TC1-1-13M+;
- the SPF5043Z;
- the TCXO's level: 0.8 V p-p minimum into the reference input's 0.5-1.5 V p-p.

They match. The mixer's output pins are numbered 27 OPN / 28 OPP in the pin table and the other way round in the application schematic. A receiver does not care: it is a 180° phase.

1.2 R1: the converter had no IF rejection, and the high-pass that fixes it

`rev08_rf_audit.py` runs the preselection with its drawn values (the lossy-inductor and pad model of `rev08_filters_mc.py`):



Converted UHF mode: what the preselector lets reach the mixer, before and after

Frequency	88-108 MHz	118-170 MHz	250 MHz	300 MHz	446 MHz	513.5 MHz	660-2500 MHz
UHF low-pass alone (as audited)	0.1-0.2 dB	0.2-0.4 dB	0.7 dB	0.8 dB	0.8 dB (in band)	7.9 dB	≥ 53 dB
High-pass + low-pass (now)	56-70 dB	53-67 dB	13 dB	1.9 dB	1.2 dB	8.2 dB	≥ 53 dB

What was wrong. The design checked the image (RF + 270 MHz, ≥ 50 dB) and the LO, but not the IF itself.

- Anything already at 100-170 MHz reached the mixer at full strength, after 22 dB of LNA.
- It then leaked to the mixer's output at the mixer's RF-to-IF isolation and landed in the IF window as if it had been converted, at RF = LO − f.
- At 446 MHz, for example, FM 100-108 MHz showed at 473-481 MHz, airband at 444-463 MHz, and 2 m, marine and PMR at 407-437 MHz.

The data sheet plots the mixer's RF leakage only from 500 MHz up (45-60 dB below a 0 dBm input). Taking 35-50 dB at 135 MHz [E]:

- the IF rejection was **31-46 dB**;
- a −30 dBm FM or airband carrier at the antenna then looked like a −61 to −76 dBm UHF signal, 53-68 dB above the −129 dBm floor in 12.5 kHz;
- the same carriers loaded the mixer: −20 dBm at the antenna was about 0 dBm at its input.

The fix. A 5th-order elliptic high-pass in series with preselector B's common input (`VU_PSB_IN` to `VU_PSB_HP`):

- the parts: series 11 pF, shunt 24 nH + 36 pF, series 5.6 pF, shunt 22 nH + 91 pF, series 8.2 pF (`C1441`-`C1445`, `L1441`-`L1442`, LQW15AN and C0G);

- nominal: 1.13 dB of loss at most from 300 MHz to 3 GHz, 12.7 dB of return loss, 52.8 dB of rejection below 175 MHz;
- Monte Carlo over 3,000 boards (L ±2 %, C ±0.1 pF or ±2 %, pads, inductor Q 35-55, capacitor ESL, 0.25 nH in each shunt branch): loss p99 1.51 dB, return loss p1 10.7 dB, rejection p1 51.7 dB.

What it gives.

- **IF rejection: 84-99 dB.** The same −30 dBm carrier now sits 0-15 dB above the 12.5 kHz floor; a typical −50 dBm one is under it.
- It serves every preselector B path. The SAW and LTCC high-pass paths did not need it; the LTCC low-pass path did, for 480-1000 MHz.
- **The converter covers 300 MHz up.** From 170 to 300 MHz nothing is covered: the direct path ends at 170 MHz, and a 135 MHz IF cannot reject signals that close to its own frequency. A dual conversion (REV08_PLAN §6) is the way to cover them in a later revision.
- On the board: seven 0402 parts in frame A between `U1304` and the frame's wall, the shunt branches grounded straight to the wall (LAYOUT 6.9).

1.3 Smaller RF points

#	Point	Consequence	Status
R2	Half-IF (2×2) response of 446 MHz at 513.5 MHz: the preselection takes off 8.2 dB (14.8 dB for 3×3 at 536 MHz)	DVB-T channel 26 (506-514 MHz) sits on it; the mixer's own 2×2 suppression (not in the data sheet) is what is left	Bench check with a DVB-T multiplex. A 7th-order filter cannot pass 480 MHz and stop 513 MHz
R3	LO at the mixer input, estimated −45 dBm [E], back out of `J961`	−100 dBm through the UHF low-pass and the LNA; about −49 dBm with the LNA bypassed on the 1 GHz low-pass path, above the −57 dBm receiver spurious limit [E]	**Fixed in the gateware**: the LNA is held in while the converter runs on the LFCN path; RFFC5072_PROGRAMMING §6
R4	LO at the ADC: −38 dBm at the mixer output [V plot], then 63-78 dB of anti-alias filter	−63 to −78 dBFS; aliased into the window at 125 MHz (TETRA) and 155 MHz (ADS-B)	Known fixed tones, 10-20 MHz off the wanted signal: nothing to do
R5	TCXO pin 1 to its supply through 10 k (`R1341`)	If the fitted 1XXD part is the VC-TCXO variant, Vcont sits above its 0.4-2.4 V range: +3 to +5 ppm (about 2 kHz at 446 MHz), no damage	Check the variant on the reel; for a VC-TCXO, a divider to 1.4 V
R6	Bias tee at 5 V against `D1301` PESD5V0F1BL (5 V stand-off)	With +5V0 at its 5.18 V maximum the antenna line sits above the TVS's stand-off: leakage, no damage [E]	BOARD_MANUAL: prefer `JP1301` at 3.3 V for antennas that accept it
R7	No limiter on `J961`; the SPF5043Z's absolute maximum is +25 dBm in	A transmitter on the same vehicle (a 2 m mobile at 1 m) can destroy the LNA	BOARD_MANUAL: an external limiter for co-sited installs
R8	The TCA6416A's ports are inputs until written: the PE4259, PE42442 and SKY13418 control pins float at power-up	Random path, perhaps a few hundred µA of extra current, no damage; the PE4312 powers up at 31.5 dB and the RFFC5072 off, so the ADC is protected	The gateware writes the expander at start; pull-downs on the next revision

The direct-sampling path, the radar and the HF chains are unchanged from SI 9.8-9.9. They keep the limits stated there:

- wideband `J911`/`J922`;
- the DAC clocks from the FPGA;
- the switches below 10 MHz;
- exciter-level outputs;
- switcher harmonics in HF.

2. Power

2.1 The budget, with Vivado's figures and the loads that were missing

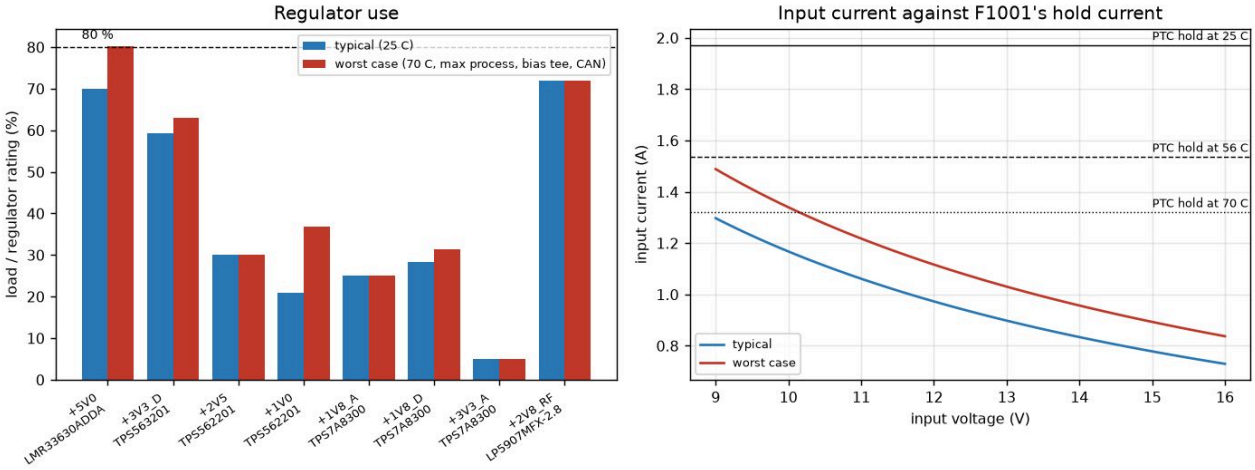
`power_budget.py` used to carry the FPGA as estimates: VCCINT 700 mA, VCCAUX 100 mA. Four loads that are on the board were not in it at all:

- the RTL8211FSI PHY, 0.5 W;
- the TCAN transceiver, 55 mA while dominant;
- the fan, 0.1 A;
- the bias tee, up to 155 mA.

Vivado 2026.1 `report_power` on the routed Rev08 design (vectorless, so "Low" confidence until measured) gives:

FPGA rail	25 °C, typical	70 °C, maximum process	Estimate until now
VCCINT + VCCBRAM	420 mA	735 mA	700 mA
VCCAUX	313 mA	365 mA	100 mA
VCCADC (from VCCAUX)	21 mA	31 mA	not counted
On-chip power	1.20 W	1.55 W	0.73 W (the thermal model's figure)

VCCAUX feeds the three MMCMs (0.40 W) and the I/O (0.33 W: IDELAY, ISERDES, LVDS).



Regulator use, and input current against F1001

The board as fixed. The worst case is 70 °C with maximum process, the bias tee at its limit, CAN dominant and the fan running.

Rail	Regulator (rating)	Typical	Worst	Use	Dissipation, worst
+5V0	LMR33630 (3 A)	2.10 A	2.41 A	80 %	1.34 W
+3V3_D	**TPS563201 (3 A)**	1.78 A	1.89 A	63 % (95 % of the TPS562201)	0.69 W
+2V5	TPS562201 (2 A)	0.60 A	0.60 A	30 %	0.20 W
+1V0	TPS562201 (2 A)	0.42 A	0.74 A	37 %	0.10 W
+1V8_A	TPS7A8300 (2 A)	0.50 A	0.50 A	25 %	0.32 W
+1V8_D	TPS7A8300 (2 A), 1.85 V	0.57 A	0.63 A	31 %	0.91 W
+3V3_A	TPS7A8300 (2 A)	0.10 A	0.10 A	5 %	0.17 W
+2V8_RF	**LP5907-2.8 (0.25 A)**	0.18 A	0.18 A	72 %	0.09 W
Input		**0.97 A, 11.7 W**	**1.12 A, 13.4 W**		

+1V8_D's LDO stays at 0.91 W. Feeding it from +2V5 would halve that, but it would mean re-routing its input through the power corner. With the 3 A buck for +3V3_D, the only reason to move it is thermal, and the CFD with the real losses decides that (P6).

2.2 Voltage windows and LDO headroom

Each rail's tolerance at the part is taken as the sum of:

- the regulator's reference over temperature (LMR33630 ±1.5 %, TPS562201/TPS563201 749-787 mV, TPS7A8300 ±1 %, LP5907 ±3 %);
- 1 % resistors;
- ripple and load step [E];
- the copper drop of SI 4.4.

Nothing reaches an absolute maximum.

Part	Rail at the part, worst case, as fixed	Range	Note
XC7A50T VCCAUX (at the balls)	1.714-1.873 V (was 1.665-1.823 V at 1.80 V)	1.71-1.89	P4
AD9484 / AD9253 DRVDD	1.797-1.873 V	1.70-1.90	inside

Part	Rail at the part, worst case, as fixed	Range	Note
XC7A50T VCCINT	0.933-1.067 V linear, inside on root-sum-square	0.95-1.05	P7: measure
XC7A50T VCCO 2.5 / 3.3 V, Si549, RTL8211FSI	9-60 mV outside ±5 % at the linear corners	±5 %	P7: measure
RFFC5072, SPF5043Z, the switches	2.701-2.889 V	RFFC5072 2.7-3.3 V	P8
AD9484, AD9253 AVDD, AD8352, DACs, ADCLK948, TCAN3403, M3SWA2	inside	each part's own	inside
M3SWA2 VEE (LM2663)	−3.38 to −3.20 V	−3.3 typ, −3.6 limit	inside

LDO	Worst headroom	Dropout at its load	
U1005 +1V8_A from +2V5	0.50 V	0.05 V	OK
U1006 +1V8_D (1.85 V) from +3V3_D	1.27 V	0.06 V	OK
U1007 +3V3_A from +5V0	1.52 V	0.01 V	OK
U1315 +2V8_RF from +3V3_D through FB1301	**0.23 V** (was 0.03 V at 3.0 V)	0.18 V	OK

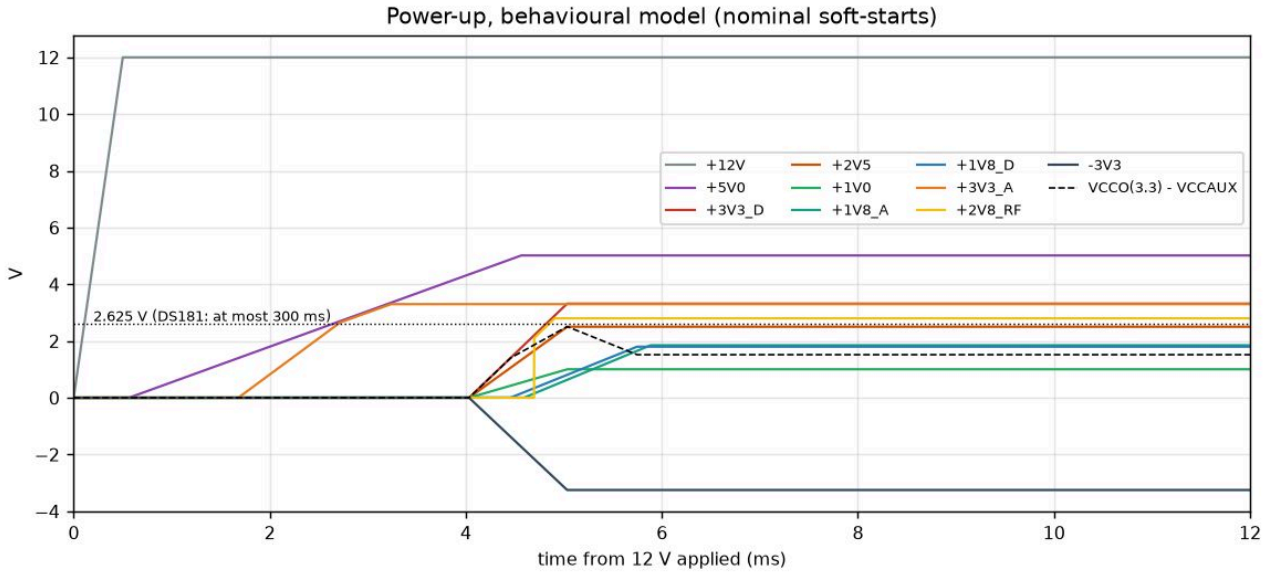
2.3 Input current and F1001

The board is a constant-power load to the input. The worst case draws 1.12 A at 12 V, 1.28 A at 10.5 V (engine off, a tired battery) and 1.49 A at 9 V. A polymer PTC's hold current falls with its own temperature [E: an 1812 series' derating table]:

PTC at	25 °C	40 °C	56 °C	70 °C	85 °C
1.5 A part (as audited) holds	1.48 A	1.32 A	1.15 A	0.99 A	0.83 A
2.0 A part (mSMD200-24V, now) holds	1.97 A	1.76 A	1.54 A	1.32 A	1.10 A

With the 1.5 A part, the worst-case load tripped it above 60 °C at 12 V and above 44 °C at 10.5 V. The PTC sits inside an enclosure rated to 56 °C ambient. With the 2.0 A part the same load trips it above 84 °C at 12 V and above 73 °C at 10.5 V. The typical load never trips it below 85 °C. A 2920 part would hold more, but its courtyard overlaps `J1001`, `Q1001`, `R1004` and `TP4`.

2.4 Start-up



Power-up, behavioural model

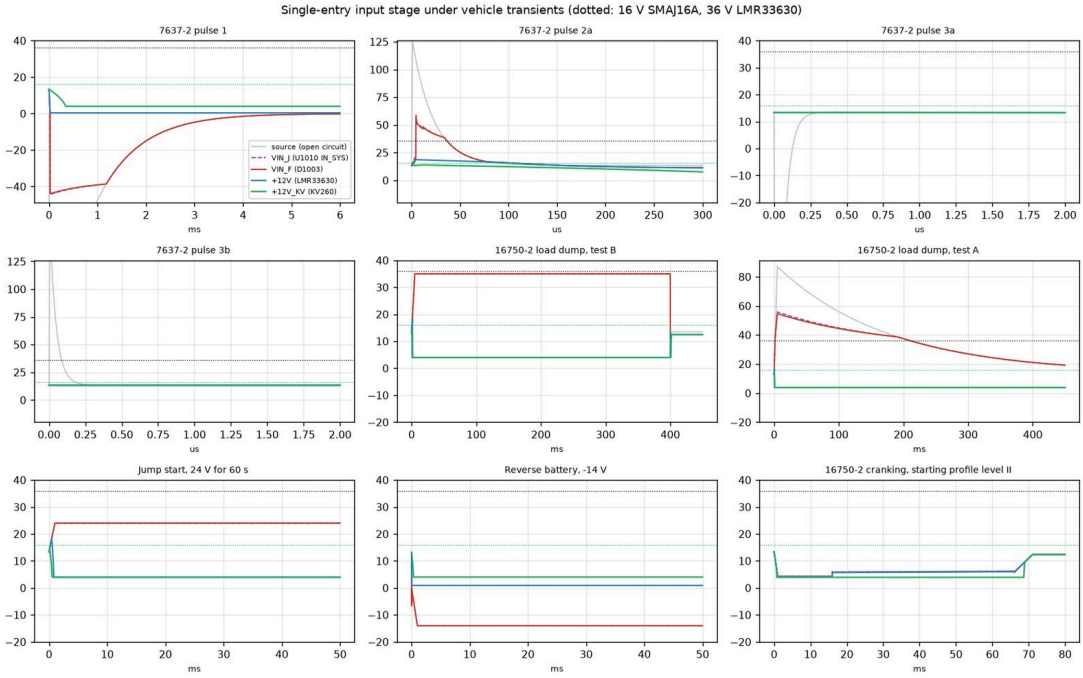
The model has 12 V applied at t = 0 and:

- the LMR33630's 4 ms soft-start (2.9-6 ms);
- the three bucks waking at 4.1 V of +5V0, then 1 ms of soft-start;
- the TPS7A8300s ramping by 6.2 µA (4.0-9.0) into their 10 nF;
- the LP5907, the charge pump and the divider following their inputs.

Run at nominal and at both soft-start corners:

- **Order:** VCCINT, VCCO_34 and VCCO_14/15 together at about 5 ms, then VCCAUX 0.4-1.4 ms later, then the ADCs' AVDD. DS181's order (VCCINT, VCCAUX, VCCO) is a recommendation for minimum inrush, not a requirement.
- **The one hard rule:** VCCO − VCCAUX > 2.625 V is allowed for at most 300 ms per power cycle. It happens for at most 0.26 ms (slow LDO corner).
- **The ADC inputs:** they are AC-coupled (100 nF) from AD8352s on +5V0, which comes up first. The coupled current is C × dV/dt = 62 µA over the 4 ms ramp, so nothing reaches the AD9484's input clamps.
- **The camera, link and PHY:** no other constraint applies. The link is AC-coupled, and the PHY has its own RC power-on reset (`R1214`/`C1216`), which the FPGA can extend through `ETH_RSTN`.

2.5 Vehicle transients



Input stage under vehicle transients

Each pulse is applied at `J1001` through its source resistance and 1 µH of harness. The model is time-stepped with backward Euler and Newton, and includes:

- the PTC;
- `D1003` (SMCJ33CA: VBR 36.7-40.6 V, 53.3 V at 28.2 A, 1500 W);
- `C1090`;
- the LM74502-Q1: OV cut-off at 18.3 V with its 1 µs turn-off and 10 µs turn-on, reverse polarity;
- two DMT10H015LFG (13.5 mΩ each);
- `D1001` (SMBJ18CA) and the +12V capacitors, derated 50 % for DC bias;
- the board as a constant-power load.

Pulse	VIN_F	+12V	FET VDS	TVS energy (limit, Wunsch-Bell [E])	
ISO 7637-2 pulse 1, −150 V, 10 Ω, 2 ms (supply cut)	−44.0 V	falls to 0.4 V (board resets)	44 V	D1003 0.19 J (2.1 J)	Pass
Pulse 2a, +112 V, 2 Ω, 50 µs	+59.1 V	18.6 V	41 V	D1003 0.016 J (0.33 J)	Pass
Pulses 3a / 3b, −220 / +150 V, 50 Ω, 0.1 µs	±0.1 V (C1090 absorbs them)	unchanged	0	none	Pass
ISO 16750-2 load dump B, suppressed to 35 V, 400 ms	35.0 V	18.3 V, then the FETs open (board resets)	32 V	none (below 36.7 V)	Pass
Load dump A, 87 V **unsuppressed**, 1 Ω, 400 ms	+54.6 V	18.3 V, FETs open	51 V	**D1003 116 J (30 J)**	**Fail** (known: POWER_SPEC 1.1)
Jump start, 24 V for 60 s	24.0 V	FETs open	20 V	none	Pass (board off while over 18.3 V)
Reverse battery, −14 V	−27.8 V (harness ringing)	0.8 V	29 V	none	Pass

Limits held in every passing case:

- +12V stays under the LMR33630's 36 V;
- VIN_F stays inside the LM74502-Q1's ±65 V;
- the FETs stay under 100 V;
- the 25 V capacitors on +12V see at most 18.6 V.

Unsuppressed load dump is the one case the board cannot take. Every car built in the last twenty years has central suppression (test B). For an old vehicle, fit a load-dump TVS (a DO-218 SM8S33A class) at the harness.

2.6 Outward supplies, and the lines between the boards

Fault	Limiter	Result
`J961` bias tee shorted	AP22652, 95-155 mA, fault flag	Safe; FB1302 (250 mA) and L1301 (170 mA) are rated above the limit
GPS supply on `J1503` shorted	F1501, 0.2 A hold	Trips; +3V3_D sags briefly
Fan shorted	F1002, 0.5 A hold	Trips; +5V0 holds
CAN wire to the battery or a 24 V jump start (P1)	**TCAN3403-Q1, ±58 V**	Survives; the TCAN330 (±14 V) would not have
USB host, board off	LP5907 from VBUS, 1 k to the FPGA	≤ 3 mA into the FPGA

Line to the other board, one side unpowered	Current	
Pmod, eight 3.3 V lines, 0 Ω both ends (P2)	up to about 100 mA a line if a board drove into an unpowered one	**No line is driven high toward an unpowered board**: `kria_present` / `adapter_alive` gating and `PMOD_SPARE2` open-drain
GPS PPS to J9 pin 12, through **330 Ω**	7.6 mA while the pulse is high (100 ms a second)	Under 10 mA
CAN RX to J9 pin 8 through 1.8 k / 1 k	0.9 mA	OK
IAS1 LVDS	AC-coupled	OK
IAS1 I²C (open drain), PROG_B (74LVC1G07, Ioff)	none	OK
IAS1 FPGA_IRQ, 1.8 V push-pull, idle low	none: driven only after link training	OK

3. What changed, by file

- **Schematic:**
- RX_VU (`rx_vu_spec.py`, regenerated): the high-pass, `+2V8_RF`, `U1315` LP5907MFX-2.8, and `C1305` kept DNP by the generator;
- STATUS (`status_spec.py`): `U1506` TCAN3403DDFRQ1 with its pin 5 on +3V3_D (a new symbol, TCAN330's drawing with pins 5 VIO and 8 STB), `R1542`/`R1543` 330 Ω;
- POWER (`rev08_audit_sch.py`): `U1002` TPS563201, `R1031` 3.24 k, `F1001` PTC 2A hold, `U1006` pin 5 to ground.
- **Board** (`rev08_audit_pcb.py`, LAYOUT 6.9):
- the high-pass in frame A;
- the two pin-5 stubs;
- values and the rail's name.
- **BOM** (`lcsc_select.py` rules): TCAN3403DDFRQ1 C35926232, TPS563201DDCR C116592, LP5907MFX-2.8 C186700, mSMD200-24V C143954, LQW15AN24NG00D C167472. Quote in **JLCPCB_QUOTE.md**.
- **Gateware** (**FPGA_GATEWARE.md**):
- the Pmod gates on both FPGAs, `PMOD_SPARE2` open-drain;
- `FPGA_IRQ` after training;
- the LNA held in on the LFCN path;
- the band table from 300 MHz.
- **Docs:** RX_VU_SPEC 1.5, POWER_SPEC, POWER_AND_STACKUP, SIGNAL_INTEGRITY 4.4, RFFC5072_PROGRAMMING 6, REV08_PLAN 11.10, LAYOUT 6.9, BOARD_MANUAL, INTEGRATIONS 2.2.

4. How to re-run

```
python _work/power_budget.py           # the budget, with the Vivado figures
python _work/power/power_audit.py      # the eight power checks, about 20 s; docs/sim/power_*.png, power_audit.json
python _work/sim/rev08_rf_audit.py     # the preselection and the high-pass; docs/sim/rf_audit_uhf_path.png, rf_audit.json
python _work/rev08_audit_pcb.py <audited board> <out>   # the board edits, from the commit before them
```

To repeat the Vivado power report:

- open `fpga/artix/.build_rev06/artix_top_routed.dcp`;
- run `set_operating_conditions -grade industrial -ambient_temp 70 -process maximum -board_layers 8to11`;
- run `report_power`.

5. The final re-audit (19 November 2026)

The owner asked for one more full pass once everything above was in, before the tag. It covered RF, power, thermal, the board's DRC, ERC and parity, the BOM and the gateware. It ran on `main` from `c1e6b1c`, the audit's fixes, onwards. Anything it found was fixed before going on.

5.1 What it found and fixed

#	Found	Fix	Where
F1	**Two vias of `Net-(C1414-Pad2)` 0.10 mm apart, drill to drill** (the rule is 0.25 mm), beside `C1415`. DRC had carried it as an accepted warning since Rev04. One net, so no short, but a drill that can break through	One via goes; `C1415` joins the other on L8	Board, `_work/rev08_final_cleanup.py`, LAYOUT 6.10
F2	15 more copper warnings carried as accepted: four vias in pads that reached no other layer (on `XO_SDA`, `U902` RFOUT2, `VU_LP1G_IN`, `VU_ATT_IN`), three through vias used only to join two tracks on one layer, eight dead stubs	Removed, or replaced by short tracks. No copper warning is left	Board, LAYOUT 6.10
F3	`PMOD_CS_N` had no pull on the Artix. The Artix sets `kria_present`, and so drives `PMOD_MISO`, after 1 ms of CS high. A line left floating by an unpowered K26, or by one that still holds its outputs high-Z, could read high and defeat the P2 gate	`PULLDOWN` on `pmod_cs_n` in `xc7a50t.xdc`. It sinks, so it never sources current into the other board	Gateware
F4	The Ethernet build (`build_rev06.tcl`) missed timing after the audit's gateware gates. It failed by 0.186 ns at first, then by 0.013 and 0.055 ns on paths that moved from one build to the next	The eye finder rotates its mask instead of indexing it (no 32:1 mux). The IDDR pipe flops take the IDDR's own edge, so ILOGIC to fabric gets a full cycle. The AERIS NCO reset's fanout is capped at 8. **WNS +0.007 ns**, 0 failing; `build.tcl` **+0.035 ns**	Gateware, FPGA_GATEWARE 4
F5	Vivado's power reports used the commercial grade: "junction temperature exceeded" at 70 °C and a pessimistic static power	Reported for the fitted industrial grade: 1.223 / 1.446 W. The budget and the CFD keep 1.25 / 1.60 W as an upper bound	`build_rev06.tcl`
F6	P6 left open: the XC7A50T at 102 °C at 70 °C ambient without `HS4`	CFD cases with `HS4`: 93.4 °C (94.2 °C clogged). See P6	`mech/v2_cfd`, ENCLOSURE_V2_THERMAL 8
F7	**The book's build ran away**, to 47 GB. MuPDF's Story never finishes a table chunk whose last row ends flush with the foot of a page; the BOM table of JLCPCB_QUOTE hit it after the audit's new rows	`export_documentation.py` stops a layout that makes no progress and moves that cut one row up. All 32 documents settle; `pdf_table_check` 0 defects	Tooling
F8	FABRICATION still gave the BOM of 17 November (214 lines, 739 parts)	224 lines, 770 parts; CPL 770, the same references as the BOM	Docs

5.2 What it checked and left as it was

- **The board.** DRC with zones refilled and schematic parity: 0 errors, 0 unconnected, 0 parity problems, and no copper warnings. What is left is silkscreen and library notices (LAYOUT 6.10). ERC gives the same 7 `pin_to_pin` warnings. `make_fab.py`: 0 errors, 0 unrouted. 222 of 224 BOM lines have an LCSC code with stock; the other two, `Y401` and `T1301`, are consigned.
- **The parts the audit changed, pin by pin against their data sheets:**
- `U1506` TCAN3403: VCC and VIO on +3V3_D, STB to ground;
- `U1002` TPS563201: the TPS562201's pin-out and its 0.768 V reference, so the same divider. Its SRP7028A 3.3 µH carries the 3 A part's current with room to spare;

- `U1315` LP5907MFX-2.8: EN tied to IN.
- **Capacitor voltage ratings against their rails**, with every capacitor's LCSC part. No rail capacitor runs above 50 % of its rating at the nominal voltage. The worst transient puts +12V at 18.6 V (pulse 2a and the suppressed load dump), 74 % of the 25 V parts there. VIN_F's are 100 V.
- **RF.** `rev08_rf_audit.py` and `txrx_isolation.py` re-run on the cleaned board: unchanged. R2 to R8 stand as notes (section 1.3).
- **Thermal margins at 70 °C**, from the CFD:
- the LMR33630 at 117.7 °C (limit 125 °C);
- `U1006` at 111 °C (limit 125 °C);
- the K26I at 99.2 °C (limit 100 °C).

The enclosure's rated ambient is 63.3 °C, not 70 °C; all three have more room there.

- **Gateware.** All the benches pass, among them `tb_system` at 500 and 400 MHz. The four gate mutations fail as they should. `cargo test`: 61 of 61.
- **The K26 build** (`fpga/kria/bd.tcl`) re-run on the gateware of section 5.1: `WNS +1.043 ns`, `WHS +0.010 ns`, 0 failing endpoints of 188,554, 53,336 LUT. The CDC report gains one synchroniser, `PMOD_SPARE2`'s. The other crossings are the ones of 18 November (**FPGA_GATEWARE.md §3.3**).
- **The front end with the 300 MHz high-pass** (`rev08_filters_mc.py`, `rev08_frontend.py`). The filter passes all 3,000 Monte Carlo runs: loss 1.52 dB at p99, rejection 51.7 dB at p1 against the 50 dB mask. It costs the converted modes 1.1 dB: ADS-B noise figure 7.1 to 7.9 dB, UHF 3.7 to 4.2 dB. The direct modes do not change (**RX_VU_SPEC.md**).
- **The documents.** Stale figures swept and every em-dash removed from the public `.md` files. The book is rebuilt: 278 pages, `pdf_table_check` 0 defects.

6. Addendum: ground offset and earth loops between the two boards (19 November 2026)

The owner asked whether two supplies, one for each board, could hurt the module: in a car, each board grounded at a different point; at home, two earthed wall adapters. The answer had to come with numbers, so it was modelled (`_work/power/ground_offset.py`, `docs/sim/ground_offset.png` and `.json`), and the design was changed to remove the problem.

6.1 What was wrong

The two boards share their ground through the 22 ground contacts of the BM20 connectors `J101`/`J102`, the FFC and the Pmod cable: 1.3 mΩ in all `[V/E]`, 94 % of it in the BM20s, each rated 0.3 A `[V]` (Hirose D47513). With each board on its own supply, any voltage between the two return points drives current through that link:

Wiring before the change	Per BM20 ground contact	Against 0.3 A
Both grounds to the same point, 1 m wires	40 mA	Pass
Two points, 1 V apart (ISO 16750-2 section 4.8), 1 m wires	411 mA	**Fail from 0.75 V**
Two points, 1 V apart, 0.3 m wires	714 mA	**Fail from 0.40 V**
Home, two earthed supplies, 1 V between the earths (50 Hz)	148 mA	Pass, but 3.5 A of loop current

The KV260 also cuts off above 13.2 V (its MP5016 eFuse, XTP682 page 3) `[V]`: it cannot share the adapter's 18.3 V input window.

6.2 What changed

- **Single power entry** (sheet KVPWR, **POWER_SPEC section 1.4**). `J1001` feeds the whole module. `L1004`, a 6 A common-mode choke, sits on both lines. The KV260 is fed from the adapter's `J1004` through `U1010` TPS26631 (OVP 14.4 V, UVLO 8.0 V, current limit 3.0 A, −60 V reverse with `Q1010`) by a short jumper to its `J12`. There is no second supply and no second ground wire.
- **The current limit is the BM20 limit too.** With a single entry, nearly all the KV260's own return (96 %) crosses to the adapter through the BM20 link, because the link is 1.3 mΩ against the jumper's 33 mΩ. So `R1043` sets 3.0 A, the KV260's own brick rating (2.77 to 3.19 A at ±7 %), not the 3.6 A first drawn: at 3.6 A, a contact with half the others' resistance would have carried 305 mA.
- **The RJ45's shield** goes to ground through `R1218` 1 MΩ in parallel with `C1223` 1 nF 2 kV. It was the only DC path to an earthed switch or PC at the far end of an Ethernet cable. USB is not treated the same way: its ground is a conductor of the cable, so a shield RC would not open the loop.

6.3 The result, as built

Case, single entry, worst currents	Per BM20 ground contact (worst one)	Heat in that contact, in all 22	Result
Any voltage between vehicle ground points (there is one entry)	132 mA at 3.19 A	0.53 mW, 11.6 mW	Pass
Typical load (KV260 0.92 A)	38 mA		Pass
All contacts at their 100 mΩ maximum	109 mA	1.19 mW, 26.2 mW	Pass
Jumper's ground contact open (all the return through the link), contacts at maximum	122 mA (138 mA at typical)	1.48 mW, 32.5 mW	Pass
One contact at half the others' resistance, at 3.19 A	254 mA	0.97 mW, 11.2 mW	Pass
One contact at a third of the others' (15 against 45 mΩ), at 2 A	219 mA		Pass
The same at 3.19 A	352 mA	1.86 mW, 14.9 mW	Pass on heat, over 0.3 A
One at a third, the other 21 at their 100 mΩ maximum, at 3.19 A	306 mA	3.13 mW, 25.0 mW	Pass on heat, over 0.3 A
Home: one earthed supply, an earthed monitor on DisplayPort, 1 V between the earths	189 mA (rms, with the DC load)		Pass

Uneven sharing and the 0.3 A figure. The rating is a heating limit: Hirose derives its current ratings from the temperature rise measured under current, less a 20 % margin (Hirose, "Connector derating curves"), and the BM20's operating range includes that rise `[V]` (catalogue D47513). Current gathers in one contact only because that contact's resistance is low, so its heat, I²R, is the quantity to compare, not its current. The references: a typical 30 mΩ contact at 0.3 A makes 2.7 mW, a contact at its specified 100 mΩ maximum, still rated 0.3 A, makes 9.0 mW, and all 22 at 0.3 A make 59 mW. Every case is below the 9.0 mW and the 59 mW. All but one are below 2.7 mW as well. The exception (3.13 mW) needs 21 contacts worn to their maximum and one still new, at the KV260's worst current limit. `_work/power/ground_offset.py` reports these figures (`single_entry.heat` in `docs/sim/ground_offset.json`).

Input current at `J1001` (5 A rated): 1.12 A for the adapter plus 3.19 A for the KV260, 4.31 A at worst. `L1004` (6 A, 2 × 8 mΩ) dissipates 0.30 W there.

Board: DRC 0 errors and 0 unconnected with schematic parity, on the refilled copy as `make_fab.py` checks it; ERC the 7 known `pin_to_pin` warnings. `_work/kvpwr_pcb.py` and `_work/ethshield_pcb.py` rebuild the edits from the board before them.

6.4 What it does not do

- `L1004` attenuates the supply's common-mode noise by 3 to 10 dB (2.9 dB at 65 kHz, 9.5 dB at 100 MHz, `docs/sim/cm_noise.json`). It does not open an earth loop closed through another cable.
- Such loops remain where a cable carries ground as a conductor: DisplayPort to an earthed monitor (in rating, the table above), USB to an earthed PC (use a USB isolator or a laptop on battery for the debug port). They are installation matters, in **BOARD_MANUAL section 6**.
- In a car, the module needs a regulated 12 V converter upstream (12.0 V, at least 5 A, output under 13.2 V) behind a 5 A fuse. That converter is also what covers the unsuppressed load dump (test A), which exceeds `D1003`'s energy rating, as it did before this change.

7. Addendum: the PSU board and the project name (19 November 2026)

- **The PSU board** (**PSU_SPEC**, `psu/`) feeds both boards from the battery or a bench supply, each by its own cable from one ground: 38 mA a BM20 ground contact at the worst load, against 132 mA through the adapter's own single entry (`ground_offset.py`, section 7). With it, the adapter's KV260 branch (`U1010` to `J1004`) is not needed. The PSU has its own audit (PSU_SPEC section 10, `_work/psu/psu_audit.py`): every IC pin against its data sheet, every part against the worst voltage of its nets, every resistor's dissipation. It changed one part (`R4`, an anti-surge resistor) and turned the two output connectors to face the board edge. ERC 0; DRC with the zones refilled and schematic parity 0 errors, 0 unconnected.
- **The project name.** The KiCad project kept the original's name, `CSI2-KRIA-KV260_Rev01`, and its sheets sat in `rev03/`; both reached the exported sheets. It is now `KV260-IAS2RF.*` with the sheets in `sheets/`, and every title block carries the revision (Rev08.1). The netlist is the same apart from the title block, and the board re-checked after the rename: DRC with the zones refilled and schematic parity 0 errors, 0 unconnected, 0 parity issues; ERC the same 7 `pin_to_pin` warnings. The original Allied Vision Altium project stays in `PCB/` under its own name.

Source: docs/3D_MODELS.md

3D Model Audit & Mapping (`KV260-IAS2RF.kicad_pcb`)

1. Audit Summary

> **Rev08 (17 November 2026).** The board now has **771** footprints. The Rev08 parts' land patterns came from LCSC through easyeda2kicad (`_work/rev08_footprints.py`), with EasyEDA models that the library copy had dropped. `_work/rev08_models.py` writes them back into the board as text: **22 parts** now have their model (`J103`, the front end's `U1301`–`U1311`, `U1313`, `U1314`, `FL1301`–`FL1303`, `T1301`, `T1302`, `Y1301`, and `U1501`, `U1502`), from `_work/mech/cache/models3d` (outside git, like the other EasyEDA models). EasyEDA paints ceramic bodies pure white and the filters a light grey that the top view burns out, so the script gives both an off-white ceramic tone (0.62, 0.60, 0.55). Still without a model, counted on the final file: the 28 intentionally unmodelled items (6 fiducials, 5 mounting holes, 15 test points, 2 solder jumpers) and the shield frames' copper walls `SH1`, `SH2`. `J1501`, now the HRO TYPE-C-31-E-17 (18 Nov, LAYOUT 6.8), has no EasyEDA or KiCad model either; its model is drawn from the maker's drawing by `_work/mech/usbc_hro_model.py` (housing, steel shell, seal ring, tongue, contacts) and, being ours, is in the repository: `mech/models3d/USB_C_HRO_TYPE-C-31-E-17.wrl`. `J1502`, the 15-way FPC receptacle, uses its EasyEDA model from the cache, and so does `J1503` (LCSC C160392, toned by `_work/rev08_final_models.py`: KiCad's has a pure white housing); `U1505`, `D1530`, `F1501` and the passives use KiCad's. In the single-power-entry update, `L1004` (`mech/models3d/CMC_9070_SMD-4P_9.0x7.0mm.step`, `_work/mech/cmc_9070_model.py`) and `J1004` (`mech/models3d/JST_VH_B2PS-VH_1x02_P3.96mm_Horizontal.step`, `_work/mech/jst_vh_model.py`) use project parametric CAD models in `mech/models3d/`, while `U1010` uses KiCad 10's base `HTSSOP-20-1EP_4.4x6.5mm_P0.65mm_EP3.4x6.5mm.step`. The audit below is the Rev06 one (570 footprints).

An automated audit of **KV260-IAS2RF.kicad_pcb** under **KiCad 10.0.6** (KiCad's stock `share/kicad/3dmodels` library) identified:

- **Total footprints:** 570
- **Broken `${KICAD10_3DMODEL_DIR}` model references: 19** footprint instances whose `.step` path does not exist in the KiCad 10 standard installation (`Xilinx_FTG256`, `Mini-Circuits_CD542_H2.84mm`, `Oscillator_SMD_SI570_SI571_Standard`, `L_Bourns_SRP7028A_7.3x6.6mm`, `BarrelJack_CUI_PJ-102AH_Horizontal`, `Fuse_1812_4532Metric`, `HTSOP-8-1EP_...`, `QFN-20-1EP_...`, `QFN-48-1EP_...`, `LFCSP-32-1EP_...`, `LFCSP-56-1EP_...`).
- **Missing functional 3D models: 7** functional component instances without any `(model ...)` tag (`U901`–`U904` `M3SWA2-34DR+`, `J101`–`J102` `BM20B(0.8)-34DP`, `J1201` `HR911130C`).
- **Non-functional omitted items (27):** Test points (`TP*`), fiducials (`FID*`), mounting holes (`MH*`), and solder jumper (`JP1101`) remain intentionally unmodeled.

All **26** missing or broken functional component instances (across **14** unique package geometries) have been resolved with real 3D CAD models: **no synthetic boxes or block placeholders are used**.

2. Storage & Licensing Split

Bucket	Path	Contents / Licensing
Redistributable (Git)	**mech/models3d/**	8 KiCad 10 official STEP models (CC-BY-SA 4.0 / CERN-OHL compatible) + machine-readable **mapping.json**
Third-Party Vendor Cache (outside Git)	`../kv260-ias2rf/_work/mech/cache/models3d/`	7 EasyEDA / LCSC fetched `.wrl` + `.step` pairs (`easyeda2kicad` v1.0.1) whose upstream license terms prevent direct repo redistribution

> [!NOTE] For EasyEDA-sourced parts (`T701`/`T801`/`T802`, `Y401`, `F1001`, `L1001`–`L1030`, `J1001`, `J101`–`J102`, `J1201`), **mapping.json** points to the `.wrl` file because `easyeda2kicad`'s raw `.step` exports retain an internal `AXIS2_PLACEMENT_3D` construction Z-offset, whereas the `.wrl` geometry is pre-normalized to `Z = 0.00 mm` at the board surface. Both `.wrl` and `.step` remain cached side-by-side in `_work/mech/cache/models3d/`.

3. Component Mapping Table (26 Instances)

Refs	Part / Value	Footprint	Source / LCSC ID	Bucket	Offset (mm)	Rotate (deg)	Verification Notes
U1001	LMR33630ADDA	Texas_HSOP-8-1EP_3.9x4.9mm_P1.27mm	HSOP-8-1EP_3.9x4.9mm_P1.27mm_EP2.41x3.1mm.step (KiCad 10)	repo	0, 0, 0	0, 0, 0	Gull-wing leads & Pin-1 dot aligned
U1101	XC7A50T-2FTG256I	Xilinx_FTG256	BGA-256_17.0x17.0mm_Layout16x16_P1.0mm_Ball0.5mm_Pad0.4mm_NSMD.step (KiCad 10)	repo	0, 0, 0	0, 0, 0	17×17 mm body, A1 corner dot aligned
U1005–U1007	TPS7A8300RGR	QFN-20-1EP_3.5x3.5mm_P0.5mm_EP2x2mm	Texas_VQFN-RGR-20-1EP_3.5x3.5mm_Pitch0.5mm.step (KiCad 10)	repo	0, 0, 0	0, 0, 0	Pin-1 dot & all 20 pads aligned
U401	ADCLK948BCPZ	LFCSP-32-1EP_5x5mm_P0.5mm_EP2.7x2.7mm	LFCSP-32-1EP_5x5mm_P0.5mm_EP3.6x3.6mm.step (KiCad 10)	repo	0, 0, 0	0, 0, 0	Pin-1 dot & 32 pads aligned
U501	AD9484BCPZ-500	LFCSP-56-1EP_8x8mm_P0.5mm_EP5.1x5.1mm	QFN-56-1EP_8x8mm_P0.5mm_EP4.5x5.2mm.step (KiCad 10)	repo	0, 0, 0	0, 0, 0	8×8 mm QFN-56 seated on pads
U601	AD9253BCPZ-125	QFN-48-1EP_7x7mm_P0.5mm_EP5.6x5.6mm	TQFN-48-1EP_7x7mm_P0.5mm_EP5.1x5.1mm.step (KiCad 10)	repo	0, 0, 0	0, 0, 0	7×7 mm TQFN-48 aligned
U1201	RTL8211FSI-CG	QFN-48-1EP_6x6mm_P0.4mm_EP4.4x4.4mm	UQFN-48-1EP_6x6mm_P0.4mm_EP4.45x4.45mm.step (KiCad 10)	repo	0, 0, 0	0, 0, 0	Pin-1 dot matches silkscreen triangle
U901–U904	M3SWA2-34DR+	MiniCircuits_DQ3005	WQFN-16-1EP_3x3mm_P0.5mm_EP1.6x1.6mm.step (KiCad 10)	repo	0, 0, 0	0, 0, 0	Pin-1 dot matches silkscreen circle; all 16 RF switch pads aligned
T701, T801, T802	ADT2-1T+	Mini-Circuits_CD542_H2.84mm	SMD-6_L7.9-W5.6-P2.54-LS7.0-BL.wrl (LCSC C3304975, ADT1.5-17+ CD542)	cache	0, 0, 0	0, 0, 0	Exact CD542 height (2.84 mm) & 6-lead span (7.87 mm) seated flush on pads
Y401	Si549 XO	Oscillator_SMD_SI570_SI571_Standard	OSC-SMD_8P-L7.0-W5.0-BL.wrl (LCSC C2027087, Si570 7050-8P)	cache	0, 0, 0	0, 0, 0	7.0×5.0 mm 8-pad crystal/XO envelope (H = 1.65 mm)
F1001	PTC 2A hold	Fuse_1812_4532Metric	F1812_L4.5-W3.2-H1.0.wrl (LCSC C369174)	cache	0, 0, 0	0, 0, 0	4.5×3.2 mm 1812 fuse seated on pads
L1001, L1010, L1020, L1030	SRP7028A-*	L_Bourns_SRP7028A_7.3x6.6mm	IND-SMD_SRP7028A-8R2M.wrl (LCSC C2041815)	cache	0, 0, 0	0, 0, 0	Centered inside silkscreen & gold pads (H = 2.80 mm)
J1001	12V IN (PJ-102AH)	BarrelJack_CUI_PJ-102AH_Horizontal	DC-IN-TH_PJ-102AH.wrl (LCSC C3096093)	cache	2.25, -3.0, 0	0, 0, 180	Barrel opening faces -X board edge; all 3 TH pins pass cleanly through plated slots
J101, J102	BM20B(0.8)-34DP	J-BM20B(0.8)-34DP	CONN-SMD_34P-P0.40_BM20B-0.8-34DP-0.4V-51.wrl (LCSC C424540)	cache	0, 0, 0	0, 0, 0	Bottom-side IAS1/MIPI B2B plugs centered in silkscreen & 34 pads
J1201	HR911130C	RJ45_Hanrun_HR911130C	RJ45-TH_HR911130C.wrl (LCSC C50933)	cache	0, 0, 0	0, 0, 180	RJ45 port opening faces +X board edge; mounting bosses & 16 TH pins centered in plated holes

4. Verification Procedure

All placements, orientations (`rotate_deg`), offsets (`offset_mm`), pin-1 polarity indicators, and board-edge connector protrusions were visually inspected by patching a temporary copy of `KV260-IAS2RF.kicad_pcb` outside the repository and running `kicad-cli pcb render` (top-down, bottom-side, isometric, and zoomed close-ups on `U1101`/`T701`/`Y401`/`U501`, `U1001`/`U1007`/`F1001`/`L1010–L1030`/`J1001`, `U1201`/`J1201`, `U901–U904`, and `J101`/`J102`). Real repository `*.kicad_pcb` files were left untouched.

The models in `mech/models3d/` are copies of KiCad 10's official 3D library (KiCad libraries licence: CC-BY-SA 4.0 with the KiCad libraries exception), kept here because the installed KiCad on the build machine has no 3D-model package; attribution: the KiCad Library Team.

Applied (14 Nov 2026, Rev06): all 26 mappings are written into `KV260-IAS2RF.kicad_pcb`. Models in the repo are referenced as `${KIPRJMOD}/mech/models3d/...`; the EasyEDA ones as `${KIPRJMOD}/_work/mech/cache/models3d/...` (git-ignored: a fresh clone renders those parts without a body until `easyeda2kicad` fetches them again).

Blender renders: STEP placement and colours (14 November)

KiCad's own 3-D view and `kicad-cli pcb render` load the `.wrl` files above; `kicad-cli pcb export glb --subst-models` (the source of `board.glb` for the mount and enclosure renders) swaps in the `.step` of the same name. EasyEDA centres its `.step` on the part's bounding box but not its `.wrl`. As a result the Blender renders showed:

- `J1001` 2.1 mm and 3.5 mm off its footprint;
- `J1201` 2.2 mm off;
- the SRP7028A inductors 0.5 mm deep in the board.

`_work/mech/step_align.py` re-places those `.step` files in their `.wrl`'s frame, keeping their colours (OCP/XDE, originals kept as `*.easyeda.step`). The `.wrl` and `.step` bounds now agree to 0.02 mm.

The stand-in box the mount used to draw for the RJ45 (`build_mount.py`, from when `J1201` had no model) is gone: the renders now show HR911130C's own model, with its opening.

White parts. Some EasyEDA `.wrl` files use pure white (1, 1, 1), which KiCad's raytracer burns out:

- in the five cached `.wrl` files, pure white is toned to grey;
- the CD542 transformer cases (`T701`/`T801`/`T802`) are set to a warm grey (originals kept as `*.wrl.easyeda`).
- metal parts that the raytracer still rendered near-white are set to a nickel grey (0.40–0.50) in both the `.wrl` and the `.step`: the Si549's lid (`Y401`, `OSC-SMD_8P-L7.0-W5.0-BL`) and the RJ45's shell (`J1201`). Its amber LED, pale yellow in the model, is amber.
- the PHY's crystal `Y1201` uses a copy of KiCad's `Crystal_SMD_3225-4Pin_3.2x2.5mm.step` in `mech/models3d/` with its lid at the same nickel grey (KiCad's own is 0.82, near-white in the renders).

RJ45 orientation. `J1201`'s latch faces the board (tab down). That is the HR911130C itself, not the model: it is a tab-down part, unlike the KV260's tab-up jack. The plug's latch end sits about 4 mm outside the enclosure wall, so it can be pressed from below.

Blender materials. In the renders, **`_work/mech/matfix.py`** replaces the STEP importer's every-material-is-metal defaults:

- **Adapter:** the mask is the KV260 carrier's own green, translucent over an ENIG-toned copper, so tracks and pours read through it.
- **KV260:**
- its connector shells, which the STEP leaves without any material, are nickel;
- its laminate is satin.
- **White plastics:** a dark ivory, so that they never read white.
- **Reflections:** a soft-box world, so that metals reflect a horizon instead of a flat grey.

Part V: Mechanical Integration, Heatsinks & Enclosure v2

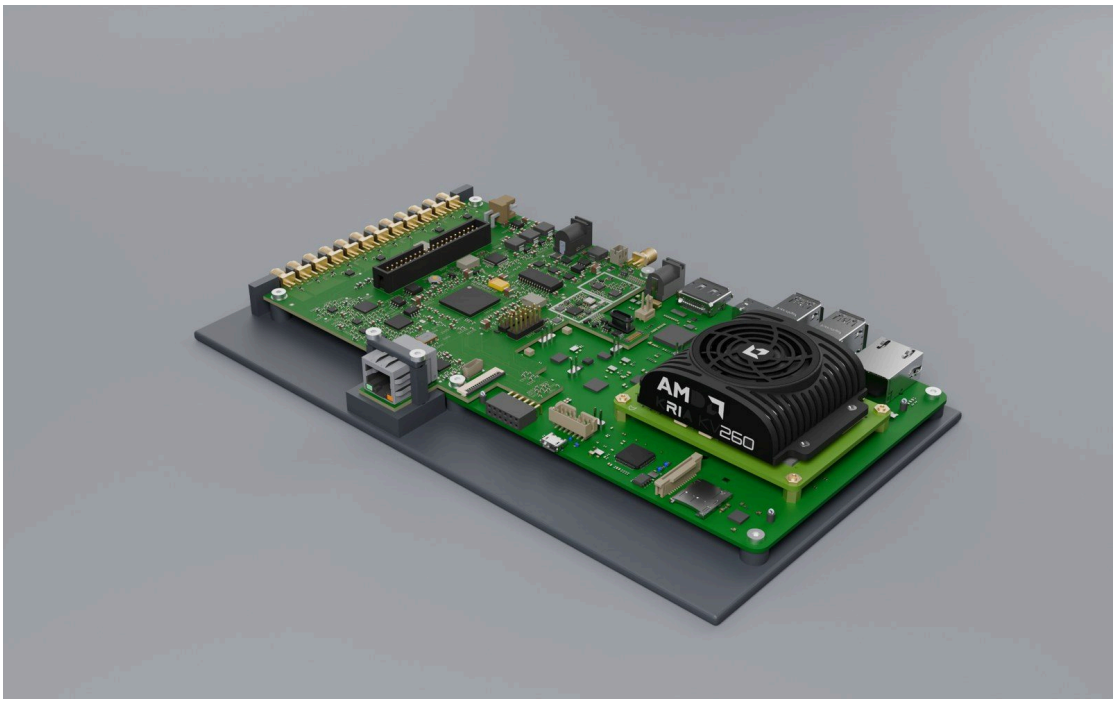
3 technical document(s)

Source: docs/MECHANICAL.md

Mounting the adapter on the KV260

13 November 2026

The adapter plugs into the KV260's two IAS connectors (Hirose BM20B, 0.8 mm mated height), screws through the carrier's two corner holes beside them (H1, H2), and overhangs the carrier's side by 97 mm, where three supports (H3–H5) carry it. A 0.8 mm connector stack and two screws do not make a rigid assembly for a board with thirteen SMAs and an RJ45 on a tab. This is a printed base that holds the KV260 and the adapter together, takes the connectors' forces, and stands on the bench.

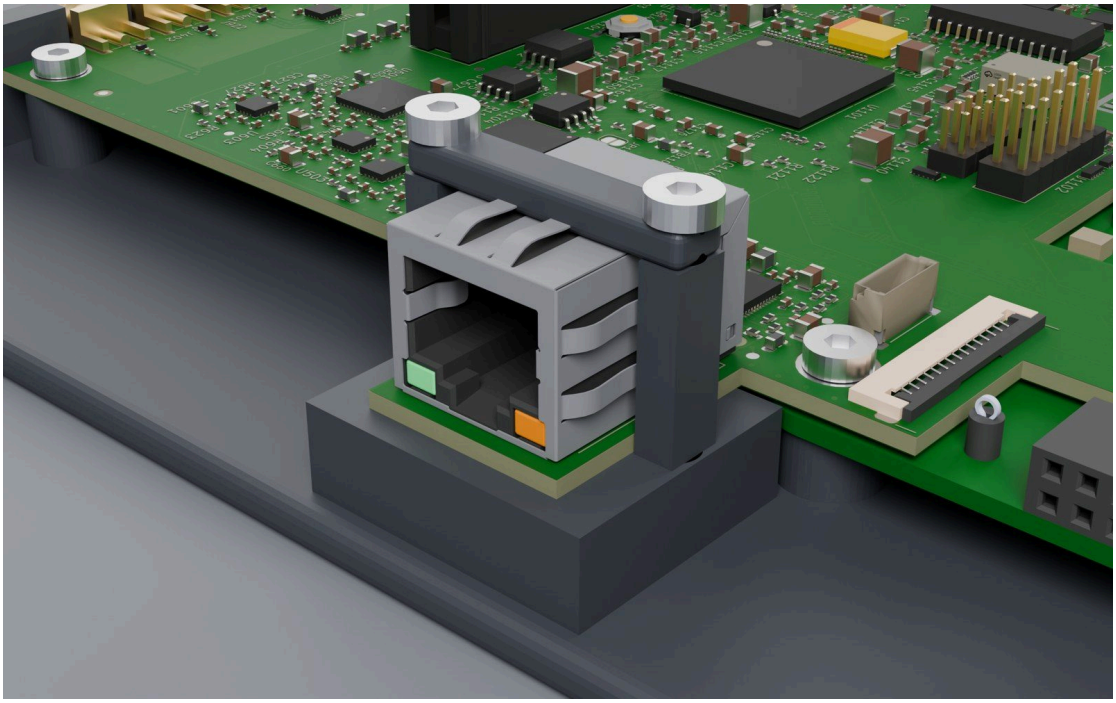


The KV260 and the adapter on the printed base

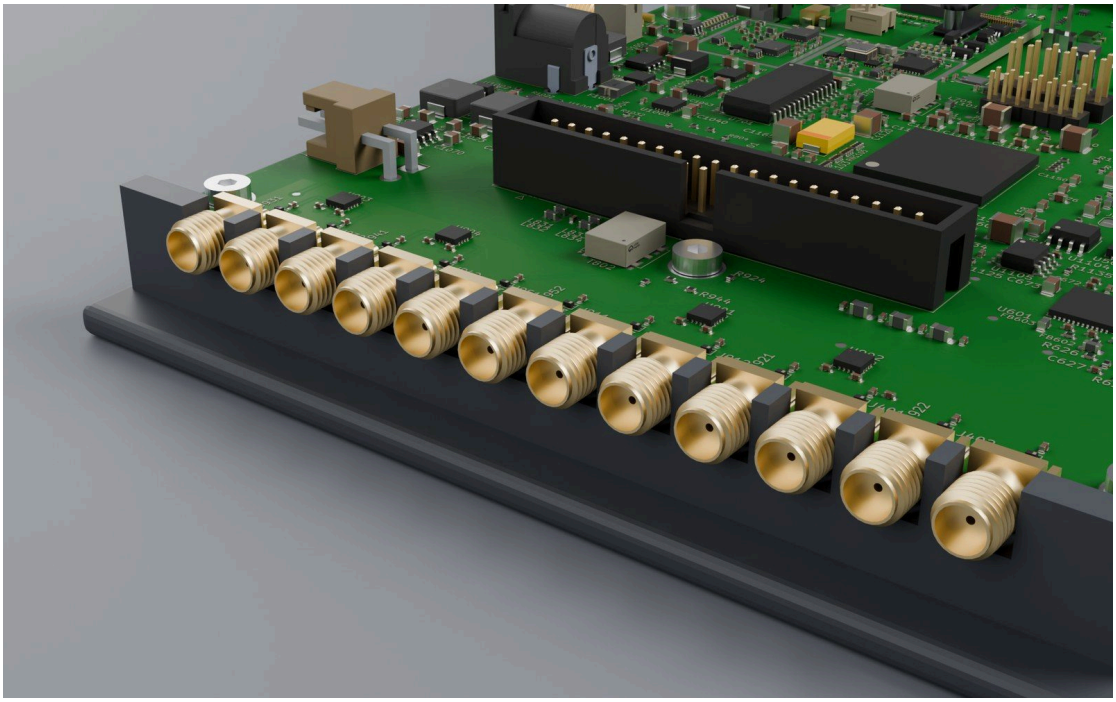
1. What it is

One printed base plate, 254 × 149 mm, 4 mm thick, whose top face is the plane the KV260 stood on (the bottom of its rubber feet, Z −7.11 in AMD's model). On it:

Part	Where	What it does
4 carrier posts, Ø9 mm, 5.5 mm tall	Under the carrier's four corner holes, in place of its rubber feet	Hold the KV260; an M3 heat-set insert in each
3 adapter posts, Ø8 mm, 7.9 mm tall	Under H3, H4, H5	Carry the overhang (LAYOUT §2: the supports were sized for 8 mm standoffs to this same plane)
SMA front wall, 4 mm thick, 12 slots	Just past the adapter's outer edge, around each SMA's 6.35 mm square body, below its thread	Takes the torque of tightening an SMA cable, so it does not reach the board or the solder joints. The slots are open at the top: the board drops in
RJ45 pedestal	Under the Ethernet tab, from the plate to the tab's underside	Supports the tab from below; a pocket clears the jack's through-hole pins
RJ45 strap (separate part)	Over the jack, screwed into the pedestal either side of the tab	Clamps the jack and the tab onto the pedestal: plugging and unplugging a cable loads the strap, not the tab's neck
2 windows	Under the carrier and under the adapter's open middle	Air for the carrier's underside; less plastic



The RJ45 tab on its pedestal, under its strap



The SMA wall

2. Assembly

1. Peel the KV260's four rubber feet off.
2. Press M3 heat-set inserts (M3 × 5.7 mm, Ø4.0 mm hole) into the seven posts and the pedestal's two holes.
3. KV260 on the carrier posts; **M3 × 6** at its two far corners (the ones the adapter does not use).
4. Adapter onto the IAS connectors, with a **0.8 mm spacer** (M3 washer, Ø6 mm) between the adapter and the carrier at H1 and H2: the board sits 0.8 mm above the carrier there, and the screw must not pull it down onto the connectors. **M3 × 8** through the adapter, spacer and carrier into the posts.
5. **M3 × 6** at H3, H4 and H5.
6. The strap over the RJ45, **2 × M3 × 20** into the pedestal.

Nothing on the adapter changes: H1–H5 and their positions are as in LAYOUT §2.

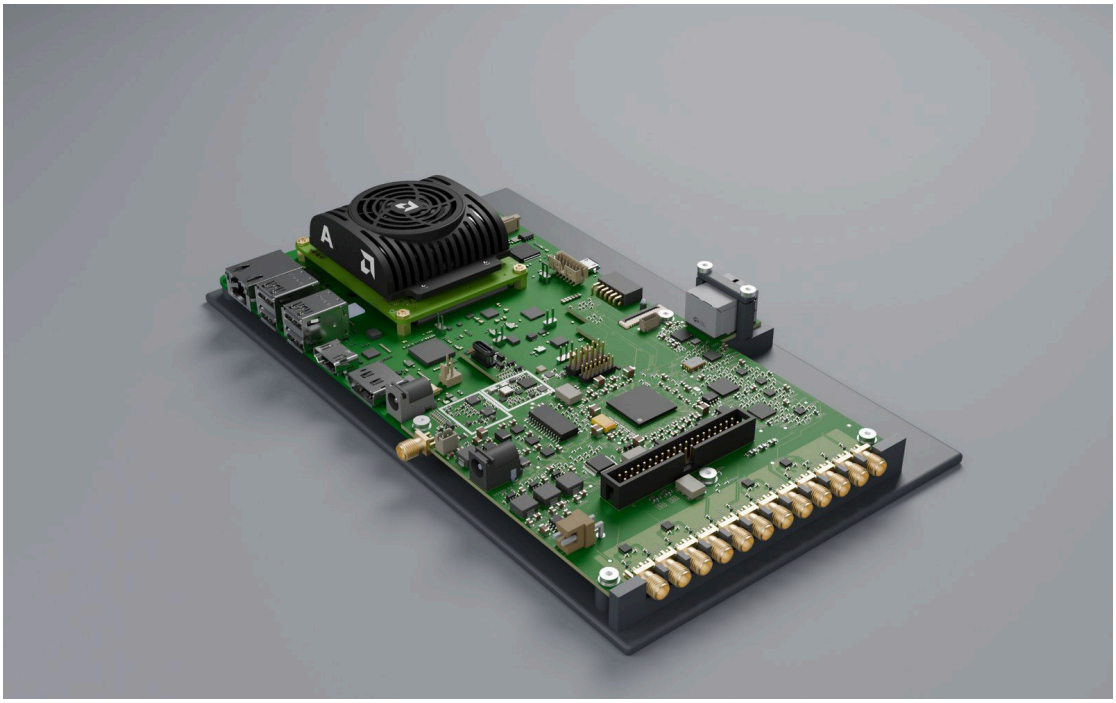
3. How it was made, and how far to trust it

- **The KV260** is AMD's own model (XTP679, `KV260V2-Starter-Kit.stp`). It is not redistributed here; download it from AMD to rebuild. The adapter is placed on it by INTERFACE_SPEC §5.3's registration (the two IAS connectors; the corner holes land within 5 µm).
- **The heights come from that model**: the carrier's PCB at Z −1.59…0, its rubber feet down to −7.11, its lowest underside part at −4.7 (well clear of the plate), nothing past its front edge where the pedestal stands (one connector, P1, sticks out 1.6 mm, 50 mm away).
- **The RJ45** is drawn at the HR911130C's data sheet size (15.9 × 21.3 × 13.5 mm): its footprint has no 3D model. Check the strap's height on a real part before printing it.
- **The SMA wall** is placed from KiCad's 3D model of the SMA (Samtec SMA-J-P-H-ST-EM1): its body and thread are both 6.35 mm across, from the board edge out to 9.5 mm. Check that the wall sits on the body, not on the thread, with the real part.
- **Not checked:** print tolerances (the slots are 6.7 mm for a 6.35 mm body), the bed size (254 mm needs a 256 mm bed; otherwise split the plate at the carrier's edge, X −10, with a lap joint), and the KV260's fan airflow with the base under it (the fan blows up, away from the plate).

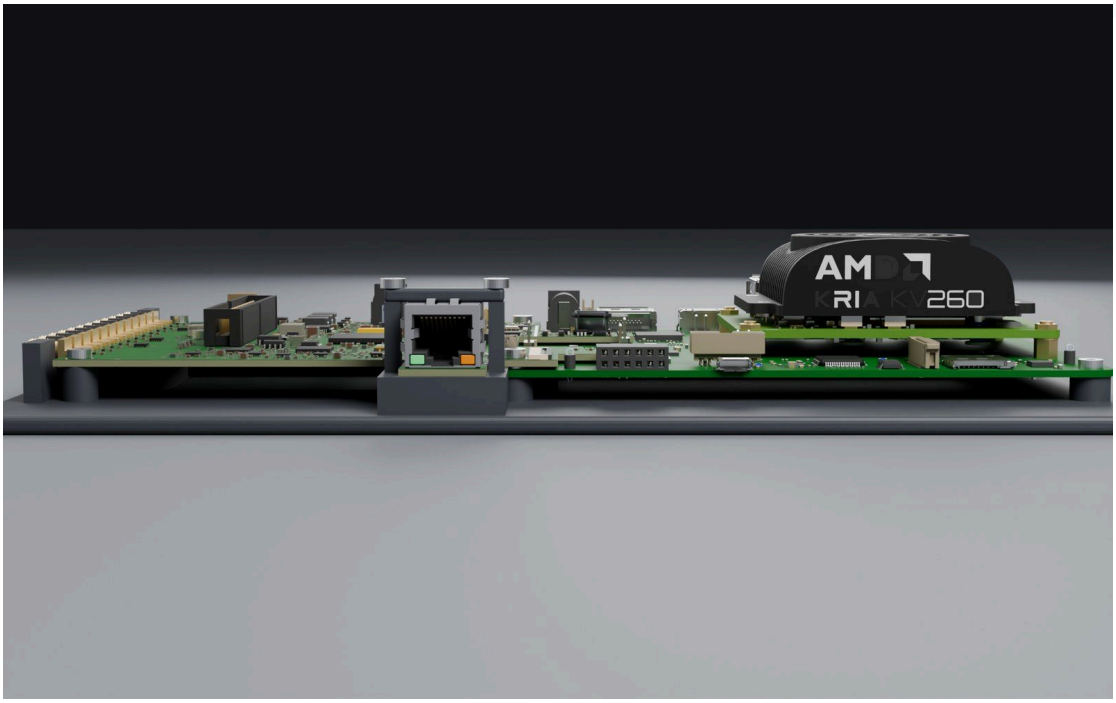
4. Files and rebuilding

`mech/mount_base.stl`, `mech/mount_rj45_strap.stl`	The two printed parts, in mm. PETG, 0.2 mm layers, 4 perimeters, 30 % infill
`_work/mech/build_mount.py`	Builds the scene in Blender (KV260, adapter, mount) and writes the STLs
`_work/mech/render_mount.py`	The renders (Cycles, GPU)
`_work/mech/step2glb.py`	AMD's STEP to glTF, with its colours (OpenCascade's Python bindings, `pip install cadquery-ocp`)

```
python _work/mech/step2glb.py KV260V2-Starter-Kit.stp _work/mech/cache/kv260.glb 0.08
kicad-cli pcb export glb --subst-models --include-tracks --include-pads --include-zones \
  --include-silkscreen --include-soldermask --user-origin 0x0mm -o _work/mech/cache/board.glb \
  KV260-IAS2RF.kicad_pcb
blender -b --factory-startup --python _work/mech/build_mount.py -- --stl mech
blender -b _work/mech/cache/assembly.blend --python _work/mech/render_mount.py -- iso,iso_back,rj45,sma,side
```



From the other side



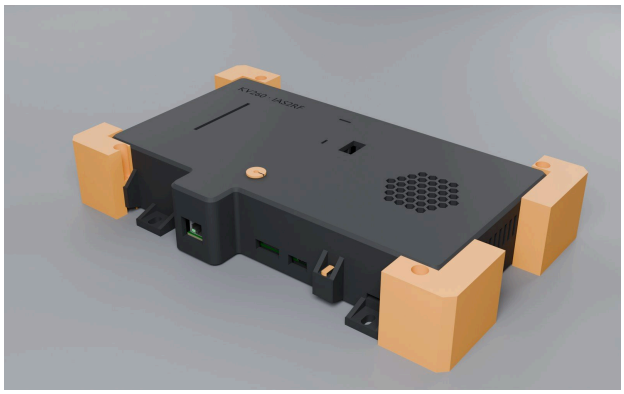
Side view

Source: docs/ENCLOSURE.md

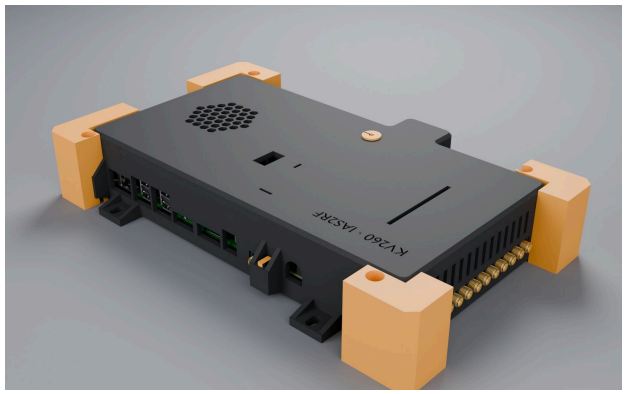
Enclosure: design, printing and simulation

13 November 2026 · `_work/mech/build_case.py` (Blender, exact booleans) · STLs in `mech/`

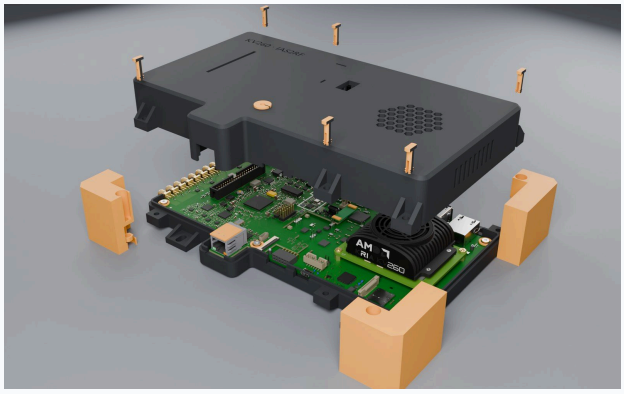
A closed, printed enclosure for the KV260 with the adapter on top. It is meant for a vehicle on expedition roads: vibration, heat in a parked car, and knocks. It has a tray and a lid that close on six lugs, either with printed snap pins (to try the fit without tools) or with stainless M4 screws. Optional TPU bumpers protect the corners. Every board rests on a honeycomb or on a clamp post with a TPU pad, so nothing rattles.



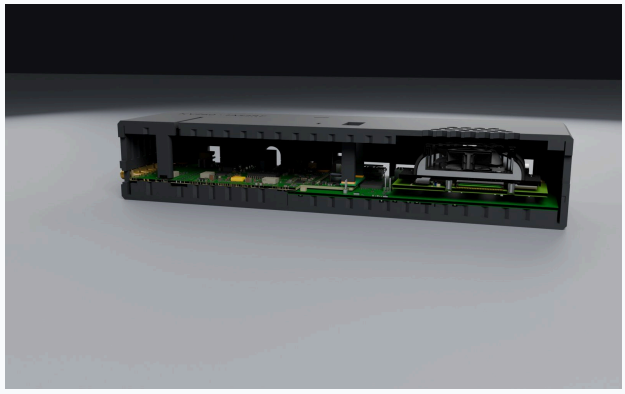
closed



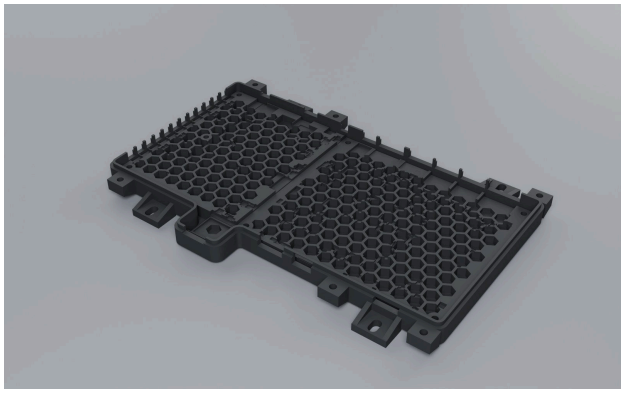
closed, back



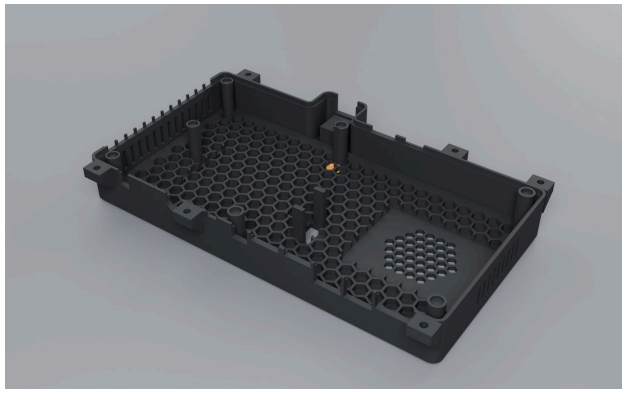
open



section



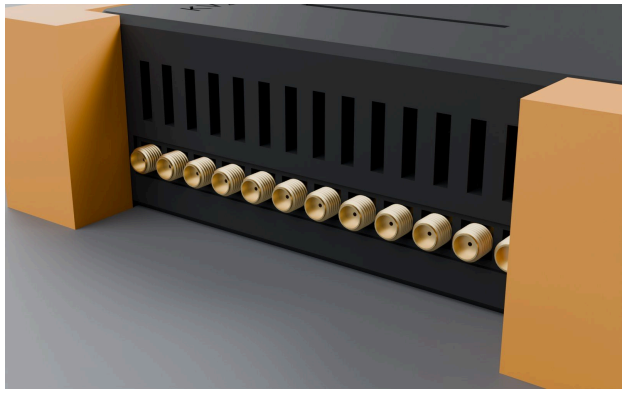
tray



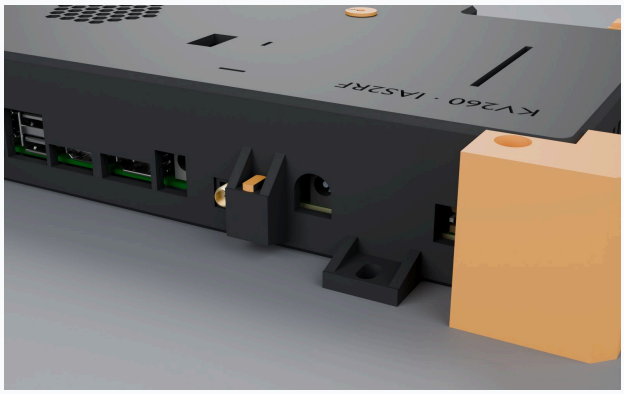
lid, inside



KV260 side: its connectors



SMA side



adapter's 12 V jack J1001

1. Parts

STL	Qty	Material	Printer	Orientation
`case_bottom.stl` (tray, 248.1 × 166.3 × 16.8 mm)	1	PETG-CF (or ASA, PAHT-CF; §4)	Bambu A1 (256 mm bed)	Floor on the bed
`case_lid.stl` (248.1 × 161.3 × 34.8 mm)	1	same as the tray	Bambu A1	Exported upside down: the top on the bed. The lugs have 45° ribs above them, so no supports
`case_pin.stl`	6	PETG or PA (not PLA: it creeps)	A1, or the Saturn 4 Ultra in a tough resin for a fit test	Exported on its flat side, so the split prongs bend across the layers
`case_pad_ring.stl`, `case_pad_rj45.stl`	7 + 1	TPU 95A	A1, from the external spool (TPU does not go through the AMS Lite)	Flat
`case_grommet.stl`	1	TPU 95A	A1, external spool	Flange down. Split, so the crimped cable from `J1503` slips in sideways
`case_bumper_l/rfront/back.stl`	4 (optional)	TPU 95A, gyroid 20 %	A1, external spool	As exported
Stainless M4 × 16 (M4 × 20 where a bumper is), DIN 934 nuts, Loctite 243	6	A2/A4	n/a	The nuts drop into the hex traps under the tray's lugs
M5 screws for the vehicle ears	4	A2/A4	n/a	Through rubber isolators (§3.3)

The Saturn 4 Ultra cannot print the shells: its build volume (about 218 × 123 mm) is smaller than either part, and the resins it prints lose most of their stiffness at 70 °C (§4).

2. Geometry

- **Outline.** Orthogonal, with a nose around the adapter's RJ45 tab. Walls are 3.5 mm thick; the SMA wall is 4 mm, because twelve SMA bodies are clamped in it.
- **Split plane** at the SMA centre line (Z = 2.84 mm above the carrier's top face). Each SMA's square body sits half in the tray, half in the lid, so closing the lid clamps them.

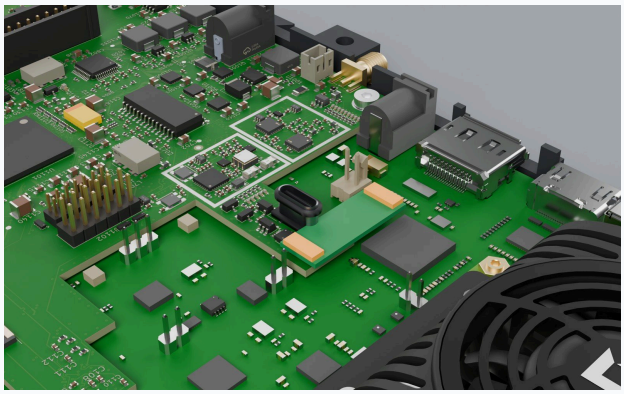
- A 1 mm recess band along the SMA row lets the plugs' coupling nuts seat on the connectors, not on the wall.
- A 1.6 × 3 mm tongue with a 0.2 mm gap seals the split line against dust and splashes.
- **Openings.**
- **KV260 rear I/O.** One cut-out per connector: the DC jack, DisplayPort, HDMI, the two USB stacks and the RJ45. Each is 1 mm larger than its connector's face, for the plugs' moulded bodies. Between neighbours the wall stays closed with a rib of at least 1.6 mm (14 Nov; the first version left one long window).
- **Front:** J4, J11 and J2.
- **Adapter's RJ45:** its window.
- **Adapter's 12 V jack J1001:** a 12 mm round-topped U up from the shells' joint, centred on the barrel. The jack sits 3.5 mm inside the wall, so a 5.5/2.1 plug's moulded body has to go into the wall for the barrel to seat.
- **Ribbon to AERIS-10's ADAR1000 boards:** a 54 × 2.6 mm slot in the lid right above the IDC header J1103, for the 40-way ribbon. The plug is fitted before the lid goes on.
- **The twelve SMA notches** in the front wall; the thirteenth SMA, `J961`, has its own notch in the back wall (Rev08, below).
- **Left inside:** JTAG, Pmod and the fan header, which are reached with the lid off.
- The rear lug beside J1001 moved from X −40 to −20 to clear it, and in Rev08 to −27 (below).
- **Rev08 (17 Nov, REV08_PLAN §9).**
- `J961`, the thirteenth SMA (VHF/UHF antenna), comes out of the back wall at X −14.05. Its notch is split at the SMA's centre line like the other twelve, so the two shells clamp its body.
- **The back-wall lug** moves from X −20, where the notch now is, to −27: 2.6 mm of wall to the notch on one side and to the 12 V jack's opening on the other. East of the notch the gap to the KV260's opening is 11.5 mm, too narrow for a 14 mm lug. The lug's face is 6 mm from `J961`'s axis: the plug's coupling nut turns by hand, and a spanner goes on from the east side. The nine back-wall slots stay where they were, above the notch.
- **Two LED slots in the lid**, 1.6 mm wide: one over the nine status LEDs north of `J961`, one over the five rail LEDs on the tongue.
- **The camera on the tongue.** An IAS camera module plugs into `J103`. The lid has a 10 × 17 mm window for its lens and two clamps on the module's ends, each with a TPU pad (`case_pad_camera.stl`, 2 off). The module's outline is the catalogue's 8.74 × 24.18 mm, taken from the connector at one end towards +Y, clear of the carrier's `J18`; check it against a module in hand before printing the lid.
- **The GPS and vehicle CAN cable (18 Nov).** `J1503` is now a vertical JST-SH, so its plug goes in from above and the cable rises straight to the lid, about 23 mm. It leaves through an 8.2 mm hole in the lid top, 2.9 mm from the plug's axis (X −3.5, Y 5.0), with a split TPU grommet (`case_grommet.stl`: 8 mm body, 12 mm flange outside, 10 mm lip inside, 3.2 mm bore for the six 28 AWG wires, a 0.8 mm slit to slip the crimped cable in from the side). The lip sits in a 10.6 mm seat, 1.4 mm deep, under the lid. The hole clears the corner clamp at (−5, −5) and v2's filter recess (X −69 to −11). The clamp gives way above the receptacle, where the plug stands. Fit the plug before the lid goes on, as the ribbon.
- **Single power entry (`J1004`, `L1004` and KV260 eFuse branch, 19 Nov, Rev08 final placement).**
- **`J1004` opening** (`JST B2PS-VH` + `VHR-2N` plug, `7.8 × 9.0 mm` housing with top latch, `0.5 mm` clearance per side): cut at `X −88.1` to `−79.3 mm`, `Z 2.24` to `13.40 mm` in the back wall beside `J1001`.
- **Back-wall west lug** moved from `X −95` to **`X −100`** (span `−107` to `−93 mm`, full `14 mm` width kept): `4.9 mm` of solid wall clear of `J1004`'s opening, inside the flat outer wall (`X −107.6`) and fully inside `bumper_lback`. On v2, the two back-wall exhaust slots above `J1004` (`X −85` and `−79`) start at `z = 16 mm` instead of `10 mm` (`2.6 mm` lintel above `J1004`).
- **Tray pockets** under the adapter honeycomb (`Z_FLOOR −8.0 mm`, `Z_BOT −11.0 mm`, `3.0 mm` solid outer floor): `pk_l1004` (`5.3 mm` deep under `L1004`'s `4.8 mm` body -> floor `Z −4.5 mm`, leaving **`3.5 mm` honeycomb web / `6.5 mm` total remaining tray thickness**); `pk_kvpwr` (`2.8 mm` deep under `U1010`, `Q1010`, `Q1011`, `D1004` `2.3 mm` max, `C1094`, `C1095`, `R1040`–`R1043`, `C1093`) and `pk_j1004_pins` (`2.8 mm` deep under `J1004`'s through-hole leads) -> floor `Z −2.0 mm`, leaving **`6.0 mm` honeycomb web / `9.0 mm` total thickness**. Under the RJ45 `J1201` tab, the bottom-side shield RC parts `C1223` (`1 nF 2 kV 1206`, up to `1.8 mm` tall) and `R1218` (`1 MOhm 0603`) sit completely inside the existing `4.5 mm`-deep `pk_rj45` pocket and below `case_pad_rj45`.
- All STLs rebuild with `0` non-manifold edges; `check_case.py` re-verified with the real `J1004` and `U1010` 3-D models reports `15` intended contacts (v1) and `16` (v2), and zero interference with `J1004`, `L1004`, `U1010`, `Q1010`, `Q1011`, `D1004`, `C1223`, or `R1218`.
- Mated `VHR-2N` plug (`7.8 × 9.0 × 13.3 mm`, straight insertion with `bumper_Lback` fitted) and dual 18 AWG jumper leads (`R = 10 mm` bend radius to KV260 `J12` at `90.2 mm` X span, `111.9 mm` routed path vs `150 mm` jumper): `0` overlaps in `check_case.py` (`VHR-2N` plug `3.97 mm` clear of `bumper_Lback`, `0.50 mm` to lid opening side walls, `0.10 mm` to tray lip; straight plug-in corridor `3.97 mm` clear of `bumper_Lback`; 18 AWG wire bend `4.79 mm` clear of `bumper_Lback`, `3.92 mm` to tray, `2.57 mm` to lid).



Rev08: J961's notch and the lug at X −27



Rev08: the lens window and the LED slots



Rev08: the camera module on the tongue, lid off

- **Cooling.**
- A hex grille over the KV260's fan (r 27 mm).
- 9 vent slots in the right wall beside the fan-sink.
- 14 slots above the SMAs, so air also crosses the adapter.
- **Board support, no play.**
- The tray's floor is a honeycomb (10 mm cells, 1.6 mm walls) that touches the underside of both boards.
- The honeycomb is pocketed 0.8 mm clear of every part that hangs below a board, 0.6 mm deeper than the part.
- Until Rev08 the adapter's own back layers were taken for one more such part, and the honeycomb under the whole adapter sat 0.67 mm low: the adapter rested on the slab's rims only. Found by the 3-D FEA (§5.3), fixed on 17 Nov: the adapter now rests on 3,950 mm² of honeycomb, four times the area it had.
- That includes the adapter's Rev05 input protection on its underside (**POWER_SPEC.md** §1.1).
- In the lid, clamp posts press each board down through 1 mm TPU 95A pads, compressed about 0.2 mm. They sit over the mounting holes H1–H5, the carrier's corners and the RJ45.
- Each clamp is notched around taller parts. `_work/mech/check_case.py` checks the shells against every board mesh. Re-run on the Rev08 build (17 Nov): 15 contacts for v1, 16 for v2, all intended. They are the honeycomb under both boards (five board-layer meshes), the lid clamp on the RJ45 `J1201`, the four TPU bumpers over the corners (tray and lid each), the v2 lid's fan, and `Z4`, a 0.6 × 0.3 mm feature 30 µm thick on the carrier's underside that touches the tray floor. None involves a Rev08 part (camera module, `J961`, the LEDs).
- **Label.** "KV260 · IAS2RF" debossed 0.6 mm in the lid, behind the ribbon slot (Y 96).

3. Closing and mounting

3.1 Two ways to close it

- **Without tools, to try the fit.** Six printed snap pins go through both lugs. Their split barbs catch on the ceiling of the nut trap. Pull them out with pliers.
- **For the vehicle.**
- Six stainless M4 screws, with DIN 934 nuts in the hex traps and threadlocker.
- M4 × 16 normally; M4 × 20 where a bumper is fitted, since it adds 3 mm under the head.

3.2 Bumpers (optional, recommended for handling)

- **Shape.** An L-shaped TPU 95A block on each corner, 18 mm thick outside the walls, from the floor to the lid top. It wraps over the corner lug and its ribs, which sit in a pocket inside it.
- **Fitting.** Slide it on from the front or back. The lug's own M4 screw goes through it, so it cannot come off.
- **Why.** §5 shows they are what makes a 1 m drop survivable.
- **Clearance.** They stay clear of the SMA band, the side vents and every connector opening: each arm along the front or rear wall stops 4 mm short of that wall's openings. The right-rear one is therefore shorter (11.3 mm instead of 22 mm), so the KV260's RJ45 plug goes in freely (13 Nov, found in the KV260-side render).

3.3 In the vehicle

- **Mounting.** Four ears at the floor have M5 slots.
- **Isolators.** Mount the case on rubber isolators (for example M5 cylindrical, about 40 Shore A). Their resonance, a few tens of Hz, sits far below the case's first mode (§5). Above about 1.4 times that resonance, vibration reaching the case is attenuated rather than amplified. This is the cheapest margin against off-road vibration.

---

4. Materials

Material	Printer notes	Heat (HDT)	Verdict
PETG-CF	A1 with a hardened nozzle; dry it	74 °C	**Default.** Stiff, easy, good to 70 °C with margin in shock
ASA	A1 possible; the open frame warps large ASA parts (brim, draft shield, warm room)	100 °C	Best for UV and heat on a dashboard
PAHT-CF	A1 with a hardened nozzle, dried; an enclosed printer is better	194 °C	Strongest; the choice if it prints flat
PETG	A1	~70 °C	Fine indoors, marginal in a hot car
PLA	A1	~55 °C	Not for a vehicle: it softens below 70 °C (§5)
Resin ABS-like	Saturn 4 Ultra (small parts only)	~50–60 °C	Fit-test pins and small parts only

The FEA in §5 assumes **solid walls**: print the shells with walls enough to be solid, because the walls are 3.5 mm, about 8 perimeters at 0.42 mm. Use 0.2 mm layers and 100 % infill where anything remains. Loads that pull layers apart are checked against the across-layer strength.

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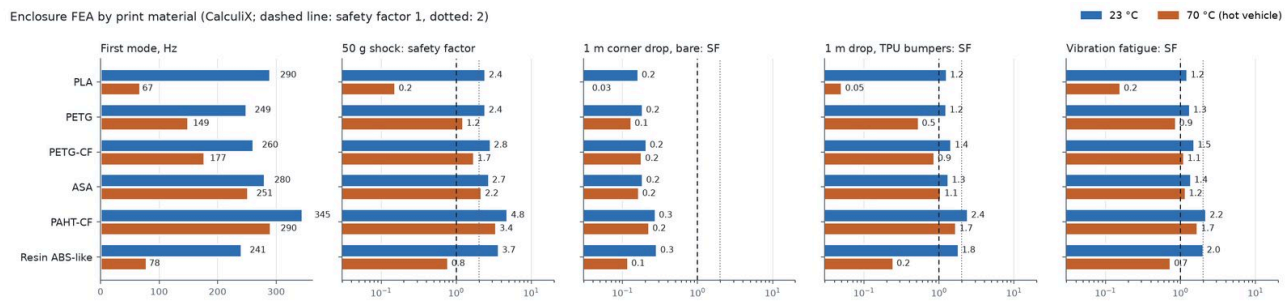
5. Simulation (CalculiX)



FEA by material

`_work/mech/fea_case.py` and `post_fea.py`; raw results in **`sim/case_fea.json`**.

Model.

- The tray, lid, pads and the three boards are meshed conformally (gmsh, 10-node tetrahedra).
- Printed plastic is orthotropic: in-layer E and strength, plus across-layer values.
- The honeycomb is homogenised as ρ = *0.29 of solid:* $E_3 = \rho E$ along the cells and $2.3\rho^{*3}E$ across them.
- The boards are elastic plates carrying their masses. The masses (KV260 90 g, adapter 110 g, SOM 120 g) are inferred.

- Each material is run at 23 °C and at 70 °C (a parked vehicle in the sun), with the strength kept at 70 °C inferred per material.
- Mesh convergence: the first mode of the PETG-CF case is 262.8 / 260.8 / 261.0 Hz with 5 / 4 / 3 mm elements.

Load cases. Each is an engineering estimate, with its assumption stated:

Case	Method
First mode	Modal analysis, 10 modes
50 g shock	Static 1 g in each axis, scaled ×50, against the across-layer strength
1 m corner drop, bare	Held at the struck corner and pushed towards it by g; the drop energy stored elastically gives the peak g. The 15 mm crushed around the corner are left out. **Deliberately pessimistic** (rigid floor, no local yielding)
1 m drop, bumpers	18 mm of gyroid TPU crushing over 60 % of its thickness at near-constant force (efficiency 0.8) stops the case at about 116 g; the stress per g from the bare case
Vibration fatigue	Miles' equation at the first mode, Q = 10, on an assumed off-road envelope of 0.04 g²/Hz from 10 to 500 Hz (about 4.4 g rms). The 3σ stress is checked against 0.3 × the across-layer strength

Results (safety factors; ≥ 1 passes, ≥ 2 is comfortable):

Material	T	Mass	f_1	50 g shock	Drop, bare	Drop, bumpers	Vibration
PETG-CF	23 °C	0.85 kg	260 Hz	2.8	0.2	1.4	1.5
PETG-CF	70 °C		177 Hz	1.7	0.2	0.9	1.1
ASA	23 °C	0.76 kg	280 Hz	2.7	0.2	1.3	1.4
ASA	70 °C		251 Hz	2.2	0.2	1.1	1.2
PAHT-CF	23 °C	0.77 kg	345 Hz	4.8	0.3	2.4	2.2
PAHT-CF	70 °C		290 Hz	3.4	0.2	1.7	1.7
PETG	70 °C	0.86 kg	149 Hz	1.2	0.1	0.5	0.9
PLA	70 °C	0.84 kg	67 Hz	0.2	0.03	0.05	0.2
Resin ABS-like	70 °C	0.80 kg	78 Hz	0.8	0.1	0.2	0.7

What this says:

- **Shock and vibration.** PETG-CF, ASA and PAHT-CF pass at both temperatures. PETG passes cold only. PLA and the resin fail hot.
- **First mode.** Above 170 Hz for the good materials, so rubber isolators (§3.3) decouple it cleanly.
- **Drop.** A bare corner hitting concrete from 1 m exceeds every material by this pessimistic method. With the TPU bumpers:
- PAHT-CF and ASA pass at both temperatures;
- PETG-CF passes cold and falls just short (0.9) hot.
- A drop is a handling event, normally not at 70 °C.

5.3 3-D model of the case as built, with both boards in it (14 Nov, Rev08 17 Nov)

The model above simplifies the shells to check every material. This one meshes the printed geometry, with every rib, honeycomb, lug, clamp post, vent and cut-out, together with the boards themselves.

Model.

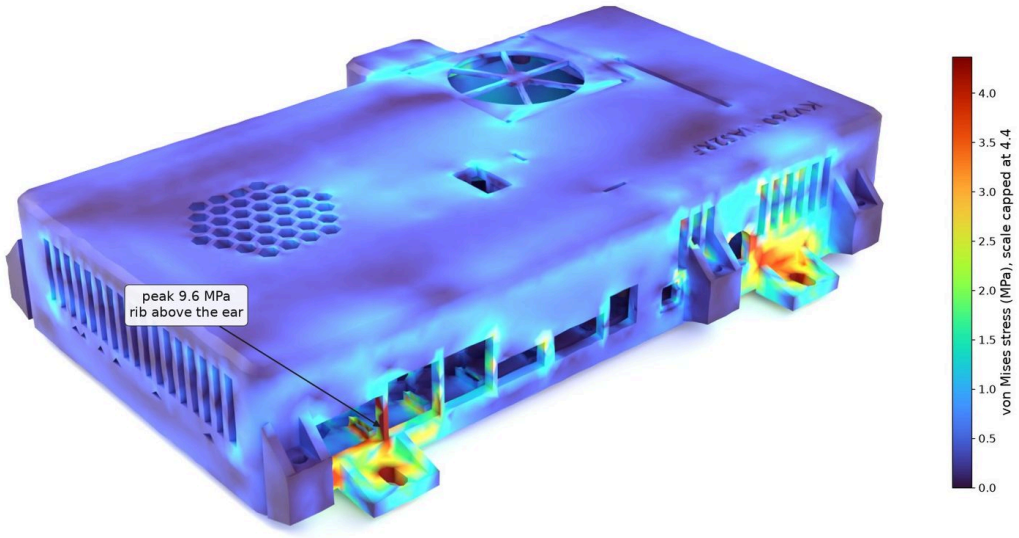
- **Boards:** the adapter's FR-4 body (from KiCad's 3-D export of the final 8-layer board) and the KV260 carrier's PCB.
- **Joints between the boards:** the two 0.8 mm spacers at H1/H2 and the mated Hirose pair.
- **Bonding:** everything is united into one bonded body (fTetWild).
- Each board is bonded where it rests on the honeycomb and the posts.
- The TPU-padded clamp posts above the boards are left out, which is conservative for the boards.
- **Mesh:** CalculiX, 10-node tetrahedra, about 197 k tets and 362 k nodes (v2).
- **Masses** ride on the boards: adapter 110 g, carrier 90 g plus the K26 SOM with its fan-sink 120 g.
- **Loads:** 50 g quasi-static shocks down, sideways and fore-aft.
- **Supports:** the four ears held at their M5 washers.
- **Case:** von Mises stress, against PETG-CF's across-layer strength: 29 MPa at 23 °C, 17.4 MPa at 70 °C.
- **Boards:** the largest principal strain, against the usual 500 με guide for BGA solder joints under shock.

Load case	Case, 99.7th pct / peak	Safety factor 23 °C / 70 °C	Adapter / carrier strain, 99.7th pct	At the BGAs (U1101, U501, U601)	Max displacement
v2 Rev08, 50 g down	3.5 / 9.6 MPa	8.3 / 5.0	168 / 394 με	80 / 96 / 69 με	0.25 mm
v2 Rev08, 50 g sideways (X)	2.2 / 5.2 MPa	13.2 / 7.9	81 / 199 με	38 / 63 / 27 με	0.08 mm
v2 Rev08, 50 g fore-aft (Y)	1.9 / 3.5 MPa	15.5 / 9.3	95 / 101 με	48 / 50 / 52 με	0.12 mm
v2 Rev07, 50 g down (adapter on the rims only)	3.5 / 9.3 MPa	8.3 / 5.0	431 / 344 με	162 / 162 / 127 με	0.25 mm
v1, 50 g down	3.5 / 9.2 MPa	8.3 / 5.0	417 / 326 με	159 / 159 / 130 με	0.22 mm

The two maps rendered on the parts themselves (Cycles; colours are the solver's, scale as in the plots below):

Enclosure v2, 50 g downwards: stress in the printed case

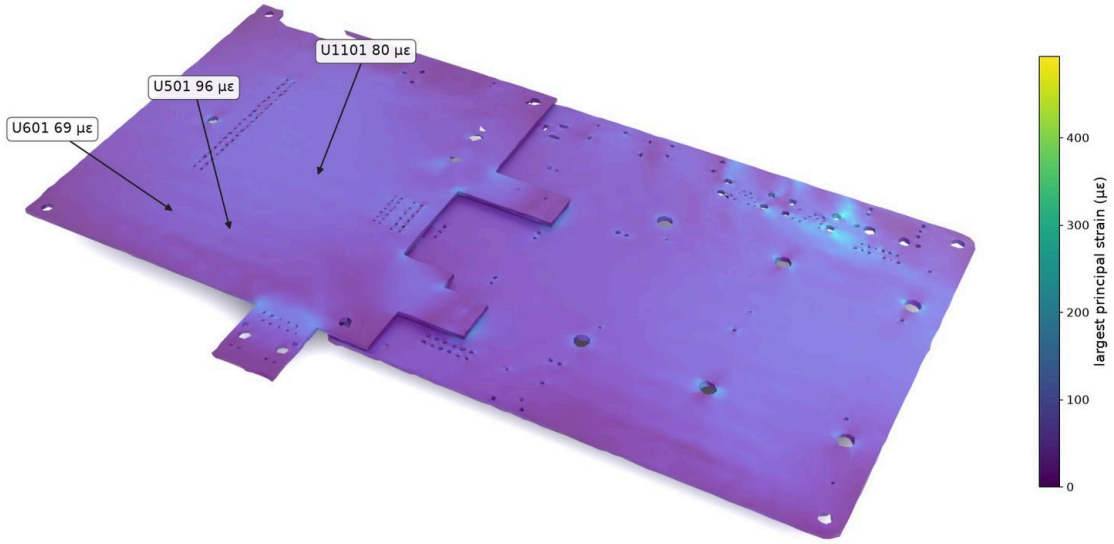
PETG-CF, both boards inside, held at the four M5 ears. 99.7 % of the case below 3.5 MPa; safety factor 8.3 at 23 °C, 5.0 at 70 °C. Max displacement 0.25 mm.



v2, 50 g down: stress in the case

Enclosure v2, 50 g downwards: strain in the two boards

Adapter bow 113 µm, KV260 carrier 92 µm. At the BGAs at most 96 µε against a 500 µε guide for solder joints under shock.

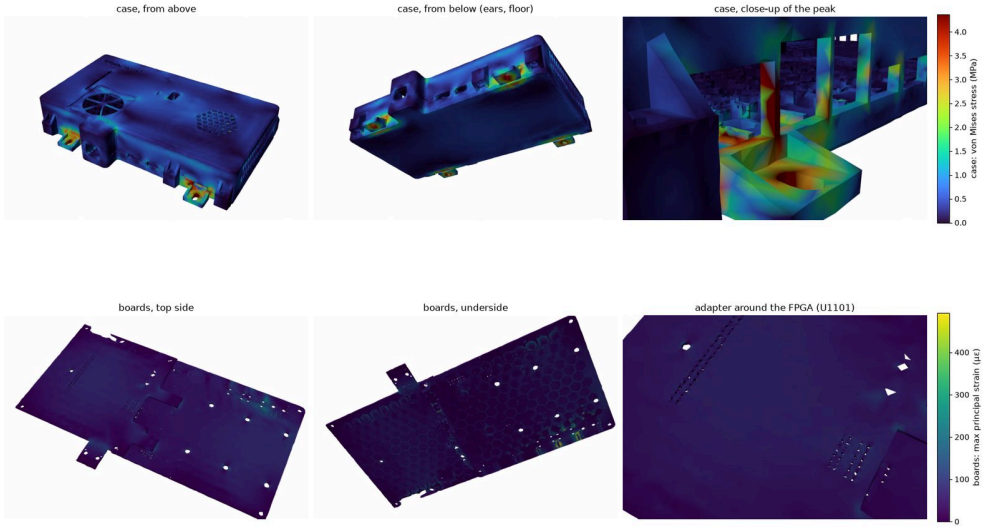


v2, 50 g down: strain in the boards

Every load case, from six angles each:

Enclosure v2 with both boards: 50 g down, quasi-static. PETG-CF case, FR-4 boards, ears held at the M5 washers. 196,708 tets, 356,163 nodes

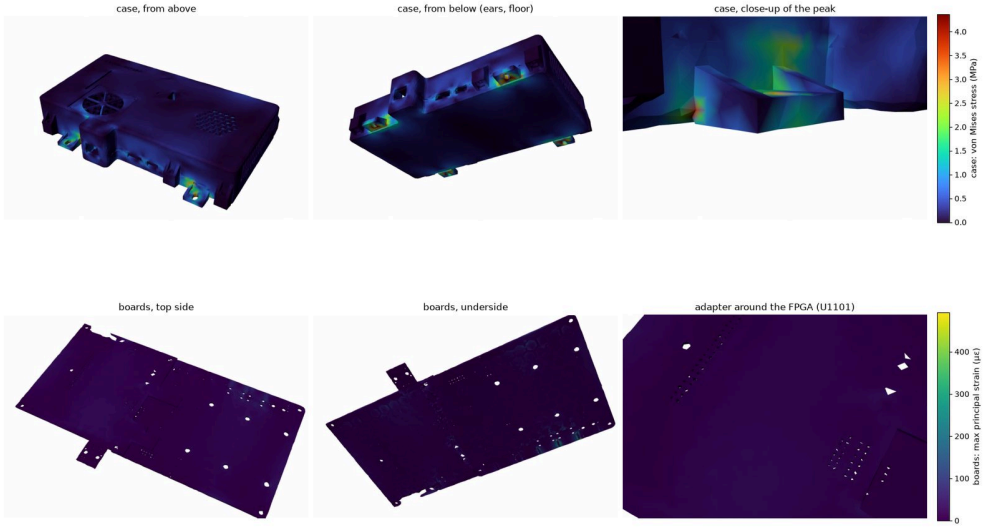
Case: 99.7th pct 3.5 MPa (peak 9.6 at (96, 116, 3)), safety factor 8.3 at 23 C / 5.0 at 70 C on the across-layer strength. Max displacement 0.25 mm.
Boards: adapter 168 με (peak 264), bow 113 μm; KV260 carrier 394 με (peak 1022), bow 92 μm; at the BGAs: U1101 80 με, U501 96 με, U601 69 με. Guide for BGA joints under shock: 500 με.



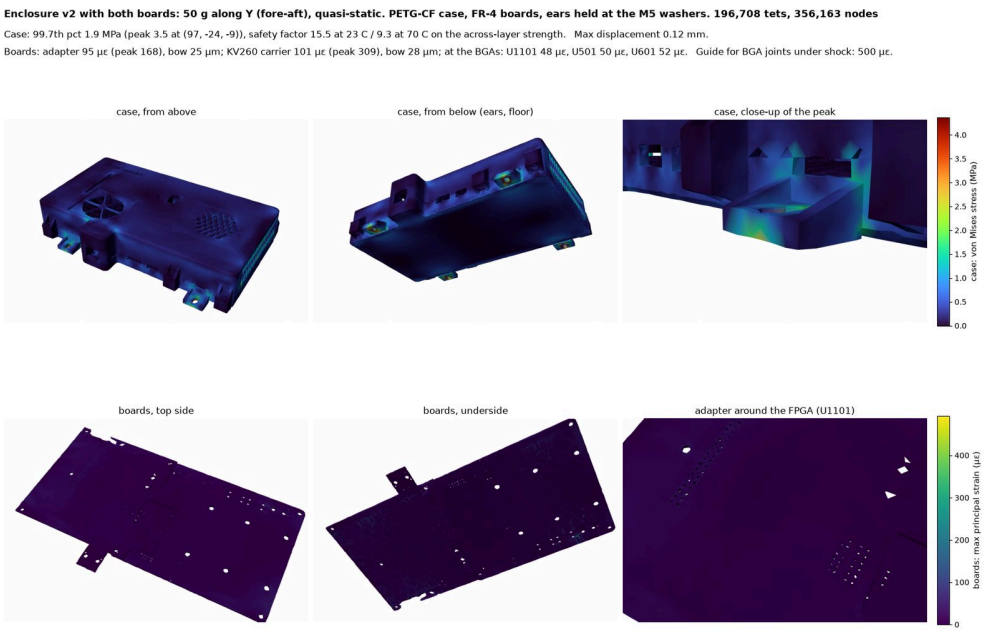
v2, 50 g down

Enclosure v2 with both boards: 50 g along X (sideways), quasi-static. PETG-CF case, FR-4 boards, ears held at the M5 washers. 196,708 tets, 356,163 nodes

Case: 99.7th pct 2.2 MPa (peak 5.2 at (-61, -20, -11)), safety factor 13.2 at 23 C / 7.9 at 70 C on the across-layer strength. Max displacement 0.08 mm.
Boards: adapter 81 με (peak 134), bow 67 μm; KV260 carrier 199 με (peak 539), bow 47 μm; at the BGAs: U1101 38 με, U501 63 με, U601 27 με. Guide for BGA joints under shock: 500 με.



v2, 50 g sideways



v2, 50 g fore-aft

v1 for comparison: **down**, **sideways**, **fore-aft**. Raw numbers: `sim/case3d_v2.json`, `sim/case3d_v1.json`.

What it shows.

- **The case.**
- The load goes into the vehicle through the four ears.
- The part that works hardest is the rear wall above the right-rear ear: the ribs between the KV260's RJ45 and USB cut-outs carry the load into the ear.
- Its peak, about 9.6 MPa, is a sharp inside corner: the real corners are rounded and the value is mesh-dependent.
- Even that peak leaves a safety factor of 3.0 at 23 °C and 1.8 at 70 °C. The 99.7th percentile leaves 8 and 5.
- Rev08's notch, moved lug, LED slots, lens window and camera clamps change nothing measurable either.
- The fan duct, the open spoke intake, the 17 right-wall and (since 15 Nov, re-run) 9 back-wall exhaust slots of v2 change nothing measurable.
- **The boards.**
- Down is the worst direction.
- Both boards bend over the honeycomb by about 0.1 mm (adapter 0.11, carrier 0.09 mm).
- The strain stays at or under 96 με at every BGA, a fifth of the guide. Before the Rev08 honeycomb fix (§2) the adapter rested on its rims only: 162 με at the BGAs and 431 με across the adapter, now 168 με.
- Higher values, up to about 1000 με, sit only where a board's bonded edge meets a honeycomb wall or a post (the carrier's rear edge). That is a modelling singularity of the bonded contact, away from any part. The real TPU-padded contact spreads it.
- **The mesh.** fTetWild's 0.45 mm envelope smooths features finer than that, and the boards are one or two elements thick. This model ranks and locates; §5's material table remains the reference for fatigue and drop.

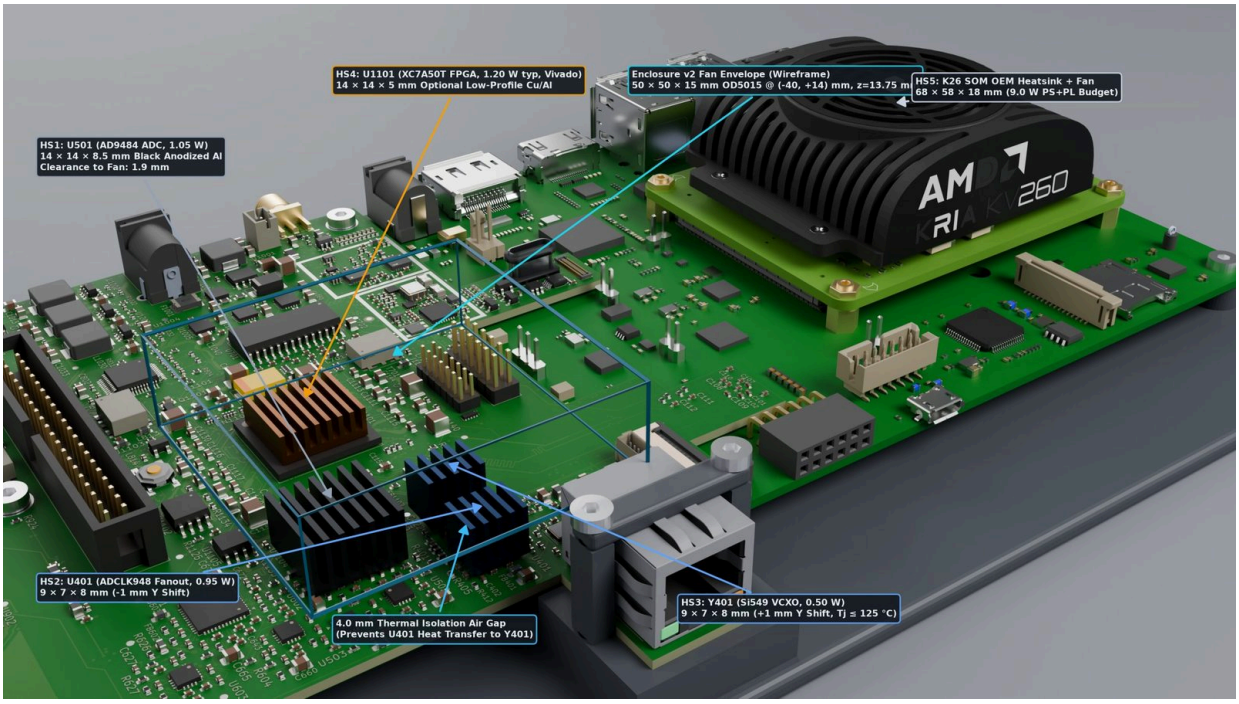
What is not established.

- **Material data.** Every value marked [I] in `fea_case.py` (for example the 70 °C strengths and the resin data) is inferred, not measured.
- **Inputs.** The vibration envelope and Q are assumptions. The board masses are inferred.
- **The bumper case** is analytical, not a contact simulation.
- **What would settle it.** A printed tray in PETG-CF, a drop test with and without bumpers, and a shaker or drive test.

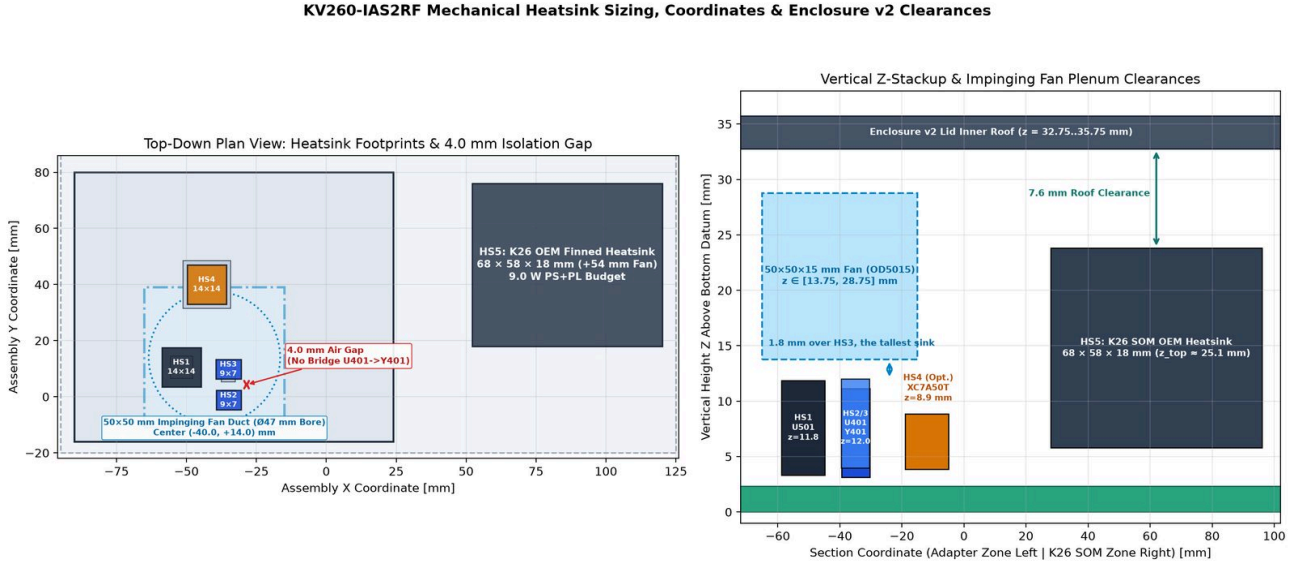
Heatsink Placement & Mechanical Sizing (`HS1`–`HS5`)

Five heatsinks are specified across the assembly, clear of the lid-mounted `50 × 50 × 15 mm` intake fan (`fan2_vis` at `z = 13.75–28.75 mm`); the three under the fan were made taller on 15 Nov:

Heatsink	Target Component	Dimensions (L × W × H)	Assembly centre (X, Y, case frame)	Vertical Envelope & Clearance
HS1	U501 (AD9484 400 MSPS ADC)	**14 × 14 × 8.5 mm** (black anodized Al, 0.18 mm TIM)	(-51.8, +10.55) mm	Fin top 11.8 mm (1.9 mm below the fan at z = 13.75 mm)
HS2	U401 (ADCLK948 LVPECL fan-out)	**9 × 7 × 8 mm** (blue anodized Al, -1.0 mm Y shift)	(-34.9, -1.20) mm	Fin top 11.2 mm (y_max = +2.3 mm)
HS3	Y401 (Si549 Programmable XO)	**9 × 7 × 8 mm** (blue anodized Al, +1.0 mm Y shift)	(-35.0, +9.80) mm	Fin top 12.0 mm, 1.8 mm under the fan (y_min = +6.3 mm -> **4.0 mm thermal gap** to HS2)
HS4	U1101 (XC7A50T Artix-7, fit it in a vehicle: 102.1 -> 93.4 °C at 70 °C, AUDIT_Rev08 P6)	**14 × 14 × 5 mm** (low-profile Cu/Al)	(-42.75, +40.0) mm	Fin top ~9.0 mm
HS5	K26 SOM (XCK26 OEM cooler)	**68 × 58 × 18 mm + 54 mm fan**	(+86.1, +47.0) mm	Fin top ~25.1 mm (7.6 mm to Enclosure v2 roof)



Annotated heatsink placement over KV260 + IAS2RF

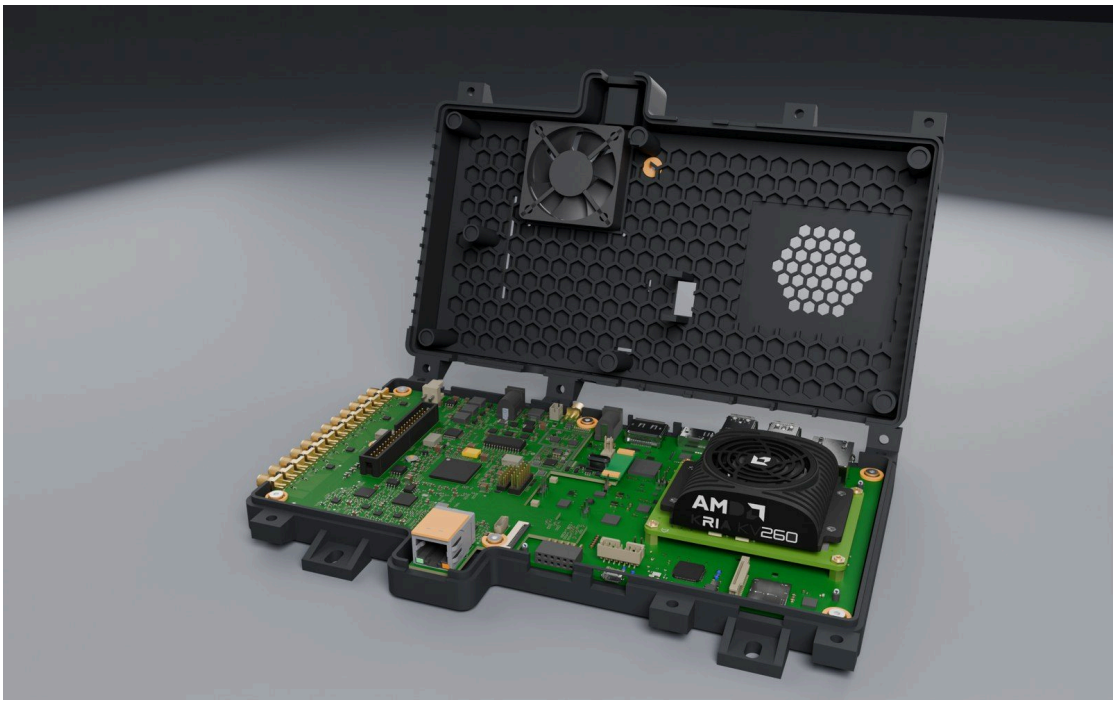


Mechanical heatsink keep-out & clearance drawing

High-resolution 4K views (`board_heatsinks_4k.jpg`, `board_heatsinks_closeup_4k.jpg`, `case_v2_closed_4k.jpg`, `case_v2_open_4k.jpg`, `case_v2_section_4k.jpg`) are stored in **`docs/img/highres/renders/`**.

6. Version 2: a fan for the adapter, for dusty roads

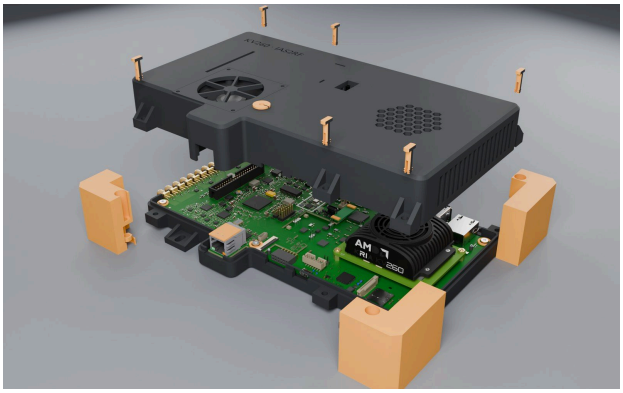
v1 stays as it is (above). **v2** is the same tray, lid and bumpers with active cooling for the adapter, from the CFD study in **ENCLOSURE_V2_THERMAL.md**. It uses the adapter's `J1002` header to give the fan 5 V.



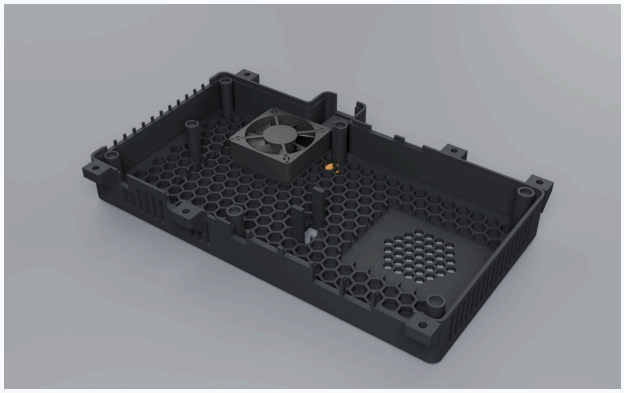
v2, the lid lifted: the fan over the adapter's hot strip



v2 closed



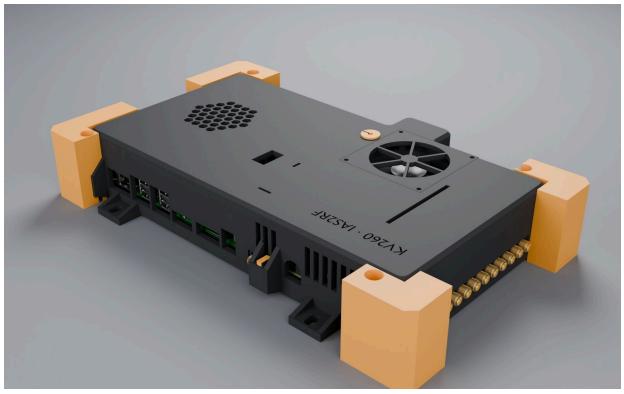
v2 open



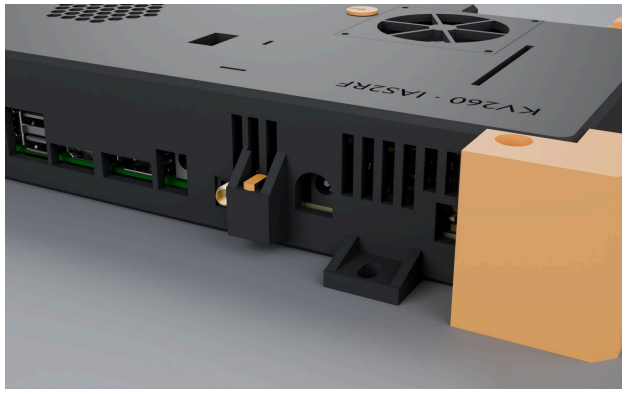
v2 lid, inside: the fan in its duct



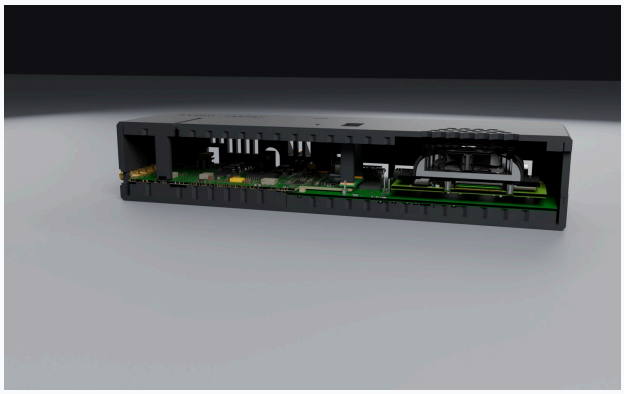
v2, KV260 side



v2, back



v2, the 12 V jack J1001



v2 section



v2, SMA side

What changes from v1.

- **A 50 × 50 × 15 mm 5 V fan** (Orion OD5015-05HB: 14 CFM, 50 Pa, 0.13 A; a 5010 until 15 Nov) blowing down onto the adapter's hot strip along its front edge: U401 (ADCLK948), Y401 (Si549), U501 (AD9484), U502/U503 (AD8352) and U1201 (the Ethernet PHY). It hangs from the lid in a 1.2 mm square duct whose top stands 4 mm below the ceiling, a plenum under the grille, so the fan can only draw through the grille. Four M3 self-tapping fan screws go from below into bosses in the duct's corners.
- **An open intake** over the fan: its whole 47 mm bore, crossed only by six 1.6 mm spokes and a 10 mm hub (86 % open). Outside it, a 58 × 58 × 1.2 mm recess holds a **100-mesh stainless filter**, clamped between the lid's spokes and those of a printed frame (`case_v2_filter_frame.stl`) with four M2.5 × 6 screws: the filter comes out for cleaning without opening the case. (The first build used a 7 mm honeycomb here, as over the KV260's fan; the CFD of the built v2 found it choked the fan, below.)
- **The SMA wall has no slots**: with the fan blowing in, the box runs at a slight overpressure (CFD: about +11 Pa), so air leaves through the vents and dust does not come in at the seams.
- **Right-wall exhaust along the whole wall**: 17 slots of 3.5 × 21 mm (y 4 to 103.5 mm, z 7.5 to 28.5 mm, 1.5 mm above the tongue's groove) instead of v1's 9 of 3 × 14 mm, and **9 back-wall slots** of 3.5 × 18 mm (z 10 to 28 mm; the two above `J1004` at x −85 and −79 start at z 16 mm) over the adapter's regulators, none between x −51.5 and −31 mm where the J1001 jack's opening is (15 Nov). In the CFD they carry 5.2 of the 7.5 CFM the fan blows in.
- **The "KV260 · IAS2RF" label** is kept, at its new place behind the ribbon slot (as v1).
- **Stick-on aluminium heatsinks** in the fan's jet (bought parts, thermally conductive epoxy rather than tape for vibration): 14 × 14 × 8.5 mm on U501, and on U401 and Y401 an 8 mm tall 9 × 9 mm sink **cut down to 9 × 7 mm**. U401 and Y401 sit only 9 mm apart: two full 9 × 9 sinks touch, and U401's (0.95 W) then heats the Si549's instead of cooling it. Fit each cut sink with its cut edge towards the other and 1 mm off its package's centre, away from the other, for a 4 mm air gap between them. Their tops sit 1.8–1.9 mm below the fan: no taller sinks.

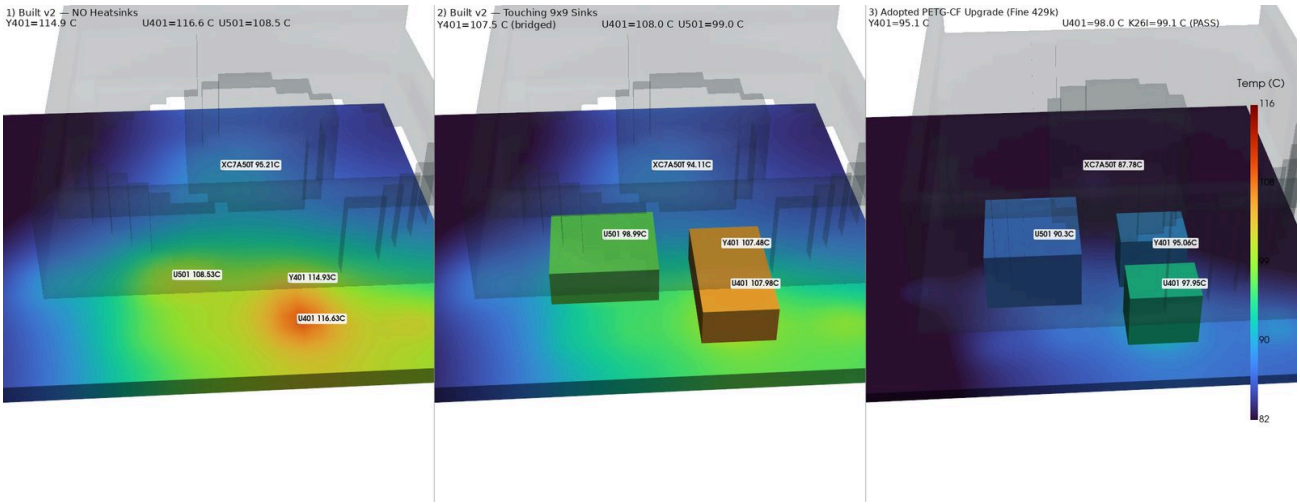
Parts to buy. An Orion OD5015-05HB fan (50 × 50 × 15 mm, 5 V, 0.13 A, well inside F1002's 0.5 A) with a 2-pin JST PH plug fitted; a 100-mesh stainless sheet cut to 56 × 56 mm; the three heatsinks; 4 × M3 × 20 self-tapping fan screws and 4 × M2.5 × 6.

Thermal result (3-D CFD of v2 as built, ENCLOSURE_V2_THERMAL.md).

- **25 °C and 45 °C ambient:** every adapter IC and the K26 stay safely under their limits, even with the filter half clogged. As first built, the honest continuous ambient rating is **~50 °C** on the stock commercial `KV260` (`XCK26-C` hits `Tj = 85 °C` at

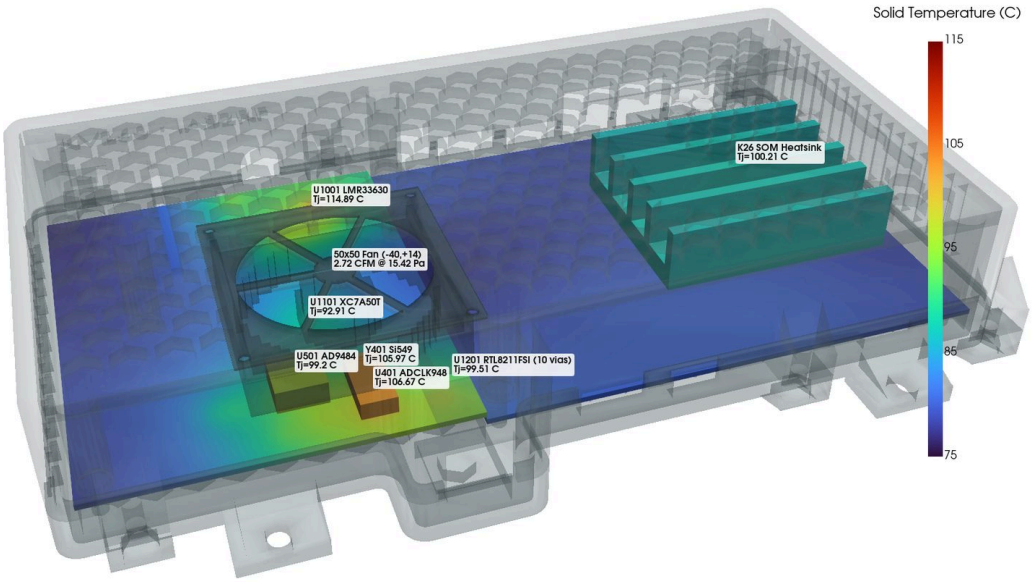
`51.27 °C` ambient; board-surface `TA = 85 °C` ICs cross `85 °C` PCB temperature starting at `54.2 °C` for `U401`, `57.3 °C` for `Y401`, and `60.3 °C` for `U501`), or **`~66–70 °C`** on adapter silicon `Tj` (`U1101` `75.8 °C`, `U1001` `80.5 °C`, `Y401` `125 °C` grade up to `87.2 °C` with `0.44 W` Si549 + `0.06 W` `R402/R403`).

- **70 °C ambient (a vehicle parked in the sun), as first built (clean fine mesh):**
- `XCK26` reaches `100.21 °C` (over commercial `85 °C` and `0.21 °C` over industrial `100 °C` `K26I`);
- `LMR33630` reaches `114.89 °C` (`10.11 °C` margin to `125 °C`), `XC7A50T` `92.91 °C`, `PHY` `99.51 °C`, and `Y401` `105.97 °C` (under `125 °C` silicon `Tj_max`, though board-surface `TA = 85 °C` parts `U401` `106.67 °C` and `U501` `99.20 °C` exceed `85 °C` local PCB/board temperature);
- Cause: the 39-cell intake honeycomb (`23.6%` open area) and 13 narrow exhaust slots hold the stock 5010 blower to `2.72 CFM` (`15.42 Pa`).
- **70 °C, with the combined upgrade (`v2_opt_combined_fine_70C`):** `Orion OD5015` 50×15 mm blower + wide `66%`-open intake grille + widened rear/right exhaust slots + tall sinks + thermal pads to lid:
- the fan reaches **`7.50 CFM` at `24.25 Pa`** and **`+5.13 Pa`** cavity overpressure (positive dust seal);
- **`K26I` drops to `97.96 °C`** (`+2.04 °C` margin to the `100 °C` industrial limit; commercial `XCK26-C` `85 °C` still requires shading or throttling above `~51 °C`);
- `Y401` drops to `94.72 °C`, `U401` to `97.80 °C`, `U501` to `90.26 °C`, `LMR33630` to `104.35 °C`, `XC7A50T` to `87.15 °C`, and `PHY` to `91.53 °C`.
- **The upgrade as built (printed lid, no aluminium, no pads; ENCLOSURE_V2_THERMAL §7):** the OD5015 fan, the spoke intake, the 17 right-wall and 9 back-wall slots and the taller sinks give 7.5 CFM and +5.3 Pa. With the Vivado `XC7A50T` power (`1.249 / 1.604 W`) and audited regulator losses, **rated ambient is 55.9 °C with the stock KV260** (its commercial K26 reaches its 85 °C junction limit there; UG1090), **62.5 °C** by the adapter's own parts on their board temperature (`Tb <= 85 °C`), and **68.2 °C with an industrial K26I SOM** without `HS4` (down from 70.9 °C because `XC7A50T` reaches 101.81 °C clean / 102.24 °C clogged at 70 °C; `K26I` stays 99.20 °C). At 70 °C `LMR33630` reaches 114.55 °C and `U1006` reaches 110.06 °C (of 125 °C). The aluminium-lid study (pads from U1001 and the K26 to a metal top) is in the report, not built.
- **Rev08 (ENCLOSURE_V2_THERMAL §8):** re-run with the front end's 0.8 W, the camera module (0.35 W, estimated), the adapter's real outline and the lens window and LED slots, plus Vivado FPGA power and audited regulator losses: **56.1 °C with the stock KV260, 63.3 °C by the adapter's own parts (`Tb <= 85 °C`, `U401`), and 70.9 °C with a K26I when `HS4` is fitted** (68.0 °C without `HS4`, where `XC7A50T` hits 102.08 °C at 70 °C; fitting `HS4` brings `XC7A50T` down to **93.38 °C clean / 94.24 °C clogged**). At 70 °C with `HS4` fitted the `LMR33630` sits at 117.71 °C (of 125 °C), `U1006` at 111.09 °C, and the `RFFC5072` at 91.37 °C junction. The camera module sits about 17 °C above ambient, so a sensor rated 70 °C sets its own, lower limit.



Built v2 at 70 °C: no heatsinks, touching sinks, and the changes

Built Enclosure v2 — 3D CHT Thermal Cutaway (Ta = 70 C, Fine Mesh 432k air cells)



Built v2, 3-D thermal cut-away at 70 °C

7. Rebuilding

```
blender -b _work/mech/cache/assembly.blend --python _work/mech/build_case.py -- --stl mech           # v1
blender -b _work/mech/cache/assembly.blend --python _work/mech/build_case.py -- --v2 --stl mech      # v2
blender -b _work/mech/cache/case.blend --python _work/mech/check_case.py
blender -b _work/mech/cache/case.blend --python _work/mech/render_case.py -- closed,closed_back,open,tray,lid,section,sma,kria,power
blender -b _work/mech/cache/case_v2.blend --python _work/mech/render_case.py -- closed,closed_back,open,tray,lid,section,sma,kria,power,fan --prefix case_v2_
blender -b _work/mech/cache/case_v2.blend --python _work/mech/fea3d_export.py -- v2                  # 3-D FEA, §5.3
micromamba run -n fea python _work/mech/fea3d_case.py v2 --h 4 --eps 0.0015                         # WSL
blender -b --python _work/mech/render_fea3d.py -- v2
micromamba run -n fea python _work/mech/compose_fea3d.py v2
blender -b --python _work/mech/render_fea3d_hero.py -- v2 Zm                                          # the two renders
micromamba run -n fea python _work/mech/compose_fea3d_hero.py v2 Zm
FEA_OUT=$HOME/fea micromamba run -n fea python _work/mech/fea_case.py --h 4      # WSL, about 3 min per material
micromamba run -n fea python _work/mech/post_fea.py $HOME/fea
```

`assembly.blend` holds the KV260 from AMD's STEP model, which is proprietary and not in this repository (`_work/mech/cache` is git-ignored). The STLs are this project's own geometry.

Source: docs/ENCLOSURE_V2_THERMAL.md

KV260-IAS2RF Enclosure v2: 3D Conjugate Heat Transfer (CHT) CFD Report

Date: 2026-11-14, Rev08 re-run 2026-11-17 (section 8) **Solver:** OpenFOAM v2412 `chtMultiRegionSimpleFoam` (steady-state compressible buoyant CHT, `kOmegaSST` RAS turbulence, coupled air + solid PCB/heatsink/spreader regions) **Scripts & Data:** **`mech/v2_cfd/run_cfd.py`**, **`mech/v2_cfd/make_plots.py`**, **`mech/v2_cfd/results.json`**

1. Problem Statement

Enclosure v1 wraps the KV260 Starter Kit (K26 SOM + OEM carrier/finned heatsink) and the IAS2RF Rev01/v2 adapter PCB inside an inner cavity of **240.6 × 124.2 × 40.75 mm** (`x ∈ [-109.6, +131.0] mm`, `y ∈ [-12.2, +112.0] mm`, `z ∈ [-8.0, +32.75] mm`), printed in PETG-CF (`k = 0.25 W/m·K`). Open SMA-side slots and unbaffled top/side openings admit road dust in automotive/field operation (`T_amb = 25 °C / 45 °C / 70 °C`), while closing the openings without thermal management risks over-temperature on tight-limit silicon, most notably **`Y401` Si549 (`Tj,max = 105 °C`)** and **`U1101` XC7A50T / K26 SOM (`Tj,max = 100 °C`)**.

This 21-case 3D CHT CFD study evaluates sealed vs. filtered-ventilation vs. lid-fan and conductive-spreader configurations against dust ingress protection and junction-temperature limits up to `T_amb = 70 °C`.

2. Thermal Model, Boundary Conditions & Power Budget

- **Total system dissipation: 18.50 W typical** (`7.50 W` adapter PCB + `9.00 W` K26 SOM + `2.00 W` KV260 carrier; `FAN_40/50` adds `0.15 W` fan motor load when present). Worst-case overdrive (`fan50_imp_maxpwr_70C`) raises the K26 SOM to `12.00 W` and scales the adapter PCB by `8.8 / 7.5 = 1.173×` (**22.95 W** total excl. fan motor, `+ 0.15 W` fan).
- **Coupled regions:**
- `air` (buoyant compressible ideal-gas/Boussinesq coupled enthalpy, `kOmegaSST`)
- `adapter_pcb` (`x ∈ [-107.2, -10.0] mm`, `y ∈ [-9.7, +108.7] mm`, `z ∈ [0.8, 2.4] mm`)
- `kv260_carrier` (`x ∈ [-9.7, +129.7] mm`, `y ∈ [-9.7, +108.7] mm`, `z ∈ [-1.6, 0.0] mm`)
- `k26_sink` (base `x ∈ [52, 120] mm`, `y ∈ [18, 76] mm`, `z ∈ [4, 10] mm`; 5 fins to `z = 22 mm`; `K26_R_JC = 1.4 °C/W`, `Tj,max = 100.0 °C`)
- `spreader_al` (Option 3 only: internal aluminum plate + IC pedestals to top lid)
- **Fans & filters modeled:**
- KV260 OEM heatsink fan at `(86.1, 47.0) mm`, `R = 27.0 mm` (active in all vented cases; sealed recirculation in sealed cases)
- Option 4a: 40×40×10 mm 5 V fan (`FAN_40_PQ`: Noctua NF-A4x10 curve, `4.8 CFM` free-air / `17.5 Pa` shutoff) over adapter `(-45.0, +45.0) mm`
- Option 4b: 50×50×10 mm 5 V fan (`FAN_50_PQ`: Sunon MF50100V1-1000U curve, `8.5 CFM` free-air / `22.0 Pa` shutoff) over adapter `(-45.0, +45.0) mm`
- Removable 100-mesh dust filter (`filter_clog_factor = 1.0` clean, `2.0` dust-loaded)

Component Power & Junction-Limit Inputs (`run_cfd.py`)

Designator / Group	Typ Power (W)	θ_JB (°C/W)	θ_JC,top (°C/W)	Tj,max (°C)	Notes
`U501` AD9484	1.05	8.5	1.7	125.0	Primary 500 MSPS ADC
`U401` ADCLK948	0.95	8.8	12.0	150.0	Clock fanout buffer
`U1001` LMR33630	0.88	13.6	22.0	150.0	12V→5V buck regulator
`U1101` XC7A50T-FTG256	0.73	8.4	4.24	100.0	Front-end FPGA
`Y401` Si549	0.50	20.0	25.0	**105.0**	Tightest adapter IC limit
`U1201` RTL8211FSI	0.50	12.0	18.0	125.0	Gigabit Ethernet PHY
`U1005..U1007` TPS7A8300	0.50 / 0.35 / 0.17	12.3	25.0	125.0	Low-noise analog LDOs
`U601` AD9253	0.46	12.0	7.1	125.0	Quad 125 MSPS ADC
`U1002..U1004` TPS562201	0.41 / 0.20 / 0.10	15.0	28.0	125.0	POL bucks

Designator / Group	Typ Power (W)	θ_JB (°C/W)	θ_JC,top (°C/W)	Tj,max (°C)	Notes
AD8352 drivers	0.40	14.0	20.0	125.0	Differential ADC drivers
AD9708 + AD9767	0.30	18.0	30.0	125.0	TX DACs
K26 SOM + KV260 Carrier	9.00 + 2.00	n/a	1.4 (K26_R_JC)	**100.0**	SOM + OEM heatsink

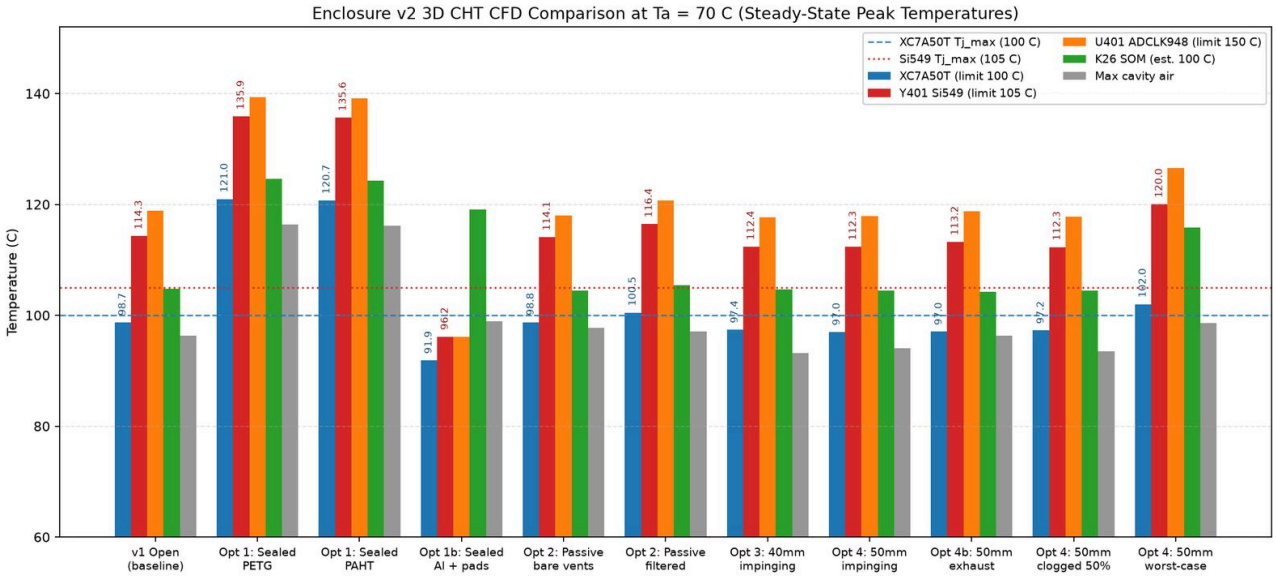
3. Complete 21-Run Simulation Matrix & Key Results

Case	T_amb (°C)	Mesh (air + solid)	T_air,max (°C)	U_max (m/s)	p_cav (Pa)	K26 Tj (°C)	XC7A50T Tj (°C)	ADCLK948 Tj (°C)	Si549 Tj (°C)	AD9484 Tj (°C)	Hottest IC (Tj)	kv / adapt / R / L Flow (CFM)
v1_open_25C	25	102,802 + 5,198	49.75	8.21	4.9	59.30	52.76	72.73	68.09	68.79	U401_ADCLK948 (72.73)	-8.44 / none / +3.56 / +4.88
v1_open_45C	45	102,802 + 5,198	70.37	8.47	4.9	79.51	73.18	93.25	88.63	89.28	U401_ADCLK948 (93.25)	-8.72 / none / +3.68 / +5.05
v1_open_70C	70	102,802 + 5,198	96.29	8.79	4.9	**104.76**	98.73	118.85	**114.27**	114.84	U401_ADCLK948 (118.85)	-9.06 / none / +3.82 / +5.24
sealed_petg_25C	25	102,802 + 5,198	69.00	7.81	7671.4	77.97	74.14	92.46	88.89	88.51	U401_ADCLK948 (92.46)	Sealed
sealed_petg_45C	45	102,802 + 5,198	89.85	8.08	7344.0	98.71	94.95	113.24	**109.76**	109.30	U401_ADCLK948 (113.24)	Sealed
sealed_petg_70C	70	102,802 + 5,198	116.42	8.35	6985.3	**124.57**	**120.95**	139.39	**135.90**	**135.37**	U401_ADCLK948 (139.39)	Sealed
sealed_paht_70C	70	102,802 + 5,198	116.16	8.37	6910.8	**124.31**	**120.68**	139.15	**135.63**	**135.11**	U401_ADCLK948 (139.15)	Sealed
sealed_alu_25C	25	93,572 + 5,198	52.60	7.82	5812.8	72.99	46.46	50.69	50.77	47.87	U1001_LMR33630 (52.84)	Sealed
sealed_alu_45C	45	93,572 + 5,198	73.20	8.06	5522.3	93.49	66.66	70.88	70.96	68.07	U1001_LMR33630 (73.03)	Sealed
sealed_alu_70C	70	93,572 + 5,198	98.96	8.37	5192.9	**119.05**	91.86	96.08	96.15	93.26	U1001_LMR33630 (98.23)	Sealed
hex2_passive_bare_70C	70	102,802 + 5,198	97.70	8.74	4.5	**104.40**	98.76	117.99	**114.06**	114.34	U1001_LMR33630 (118.98)	-8.90 / +5.05 / +3.85 / –
hex2_passive_filt_70C	70	102,802 + 5,198	97.08	8.50	6.8	**105.41**	**100.46**	120.66	**116.44**	116.50	U401_ADCLK948 (120.66)	-7.08 / +3.00 / +4.08 / –
fan40_imp_filt_70C	70	102,802 + 5,198	93.22	8.42	9.2	**104.67**	97.37	117.70	**112.37**	113.10	U1001_LMR33630 (119.08)	-7.01 / -1.50 / +8.51 / –
fan50_imp_filt_25C	25	102,802 + 5,198	47.88	7.74	10.8	58.86	51.17	72.07	66.54	67.32	U1001_LMR33630 (72.64)	-5.53 / -2.82 / +8.35 / –
fan50_imp_filt_45C	45	102,802 + 5,198	68.42	7.97	10.8	79.08	71.54	92.41	86.86	87.65	U1001_LMR33630 (93.18)	-5.74 / -2.87 / +8.61 / –
fan50_imp_filt_70C	70	102,802 + 5,198	94.04	8.27	10.7	**104.43**	96.97	117.89	**112.33**	113.08	U1001_LMR33630 (118.62)	-6.00 / -2.92 / +8.92 / –
fan50_exh_filt_70C	70	102,802 + 5,198	96.33	9.03	2.2	**104.26**	97.03	118.80	**113.21**	114.61	U401_ADCLK948 (118.80)	-10.72 / +4.57 / +6.15 / –

Case	T_amb (°C)	Mesh (air + solid)	T_air,max (°C)	U_max (m/s)	p_cav (Pa)	K26 Tj (°C)	XC7A50T Tj (°C)	ADCLK948 Tj (°C)	Si549 Tj (°C)	AD9484 Tj (°C)	Hottest IC (Tj)	kv / adapt / R / L Flow (CFM)
fan50_imp_clogged_70C	70	102,802 + 5,198	93.54	8.29	10.4	**104.45**	97.25	117.77	**112.29**	113.09	U1001_LMR33630 (119.12)	-6.22 / -2.61 / +8.84 / –
fan50_imp_maxpwr_70C	70	102,802 + 5,198	98.63	8.28	10.7	**115.80**	**101.98**	126.55	**120.01**	120.89	U1001_LMR33630 (126.61)	-5.99 / -2.92 / +8.91 / –
conv_coarse_70C	70	43,746 + 2,584	90.67	8.51	10.5	**109.19**	97.28	122.55	**113.53**	112.08	U401_ADCLK948 (122.55)	-6.04 / -2.95 / +9.00 / –
conv_fine_70C	70	262,778 + 14,086	92.44	8.96	10.8	**102.05**	93.73	110.72	**107.66**	106.80	U1001_LMR33630 (111.65)	-6.91 / -2.75 / +9.66 / –

(Bold entries exceed the corresponding IC/SOM `Tj,max`: `100 °C` for `K26` and `XC7A50T`, `105 °C` for `Si549`, `125 °C` for `AD9484`. Flow sign convention: negative = intake into enclosure, positive = exhaust out to ambient.)

4. Comparison of Enclosure Options at 70 °C



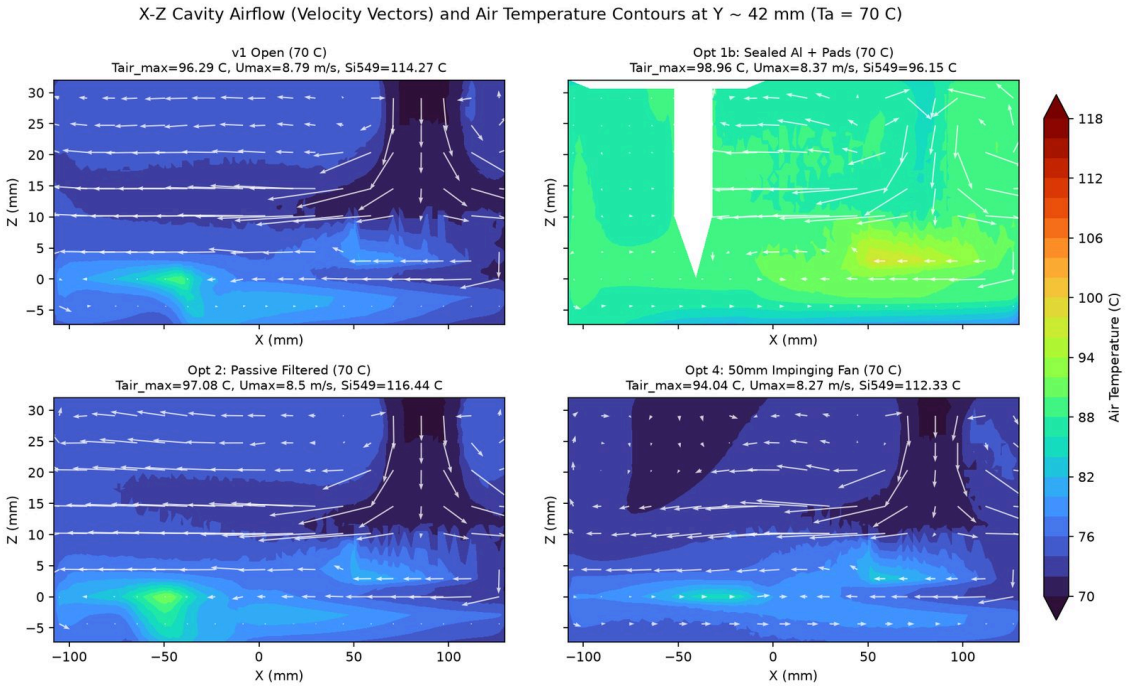
70 C Comparison of Enclosure Options

1. **Option 1 (`v1_open_70C`):** The KV260 OEM fan pulls `9.06 CFM` in through the top grille and exhausts `3.82 CFM` right + `5.24 CFM` left past the SMA bay. Even without dust filtration, `Si549` reaches `114.27 °C` (`-9.27 °C` margin) and `K26` reaches `104.76 °C` (`-4.76 °C` margin).
2. **Option 2 (`sealed_petg_70C`, `sealed_paht_70C`):** Sealing the `0.25–0.35 W/m·K` polymer shell eliminates fresh-air exchange and traps recirculating air at `116.42 °C`. `ADCLK948` hits `139.39 °C`, `AD9484` `135.37 °C`, `Si549` `135.90 °C`, `XC7A50T` `120.95 °C`, and `K26` `124.57 °C` (`>20 °C` over limit on multiple ICs; fails already at `45 °C` where `Si549 = 109.76 °C`). Switching from PETG-CF (`k=0.25`) to PAHT-CF (`k=0.35`) helps by `< 0.3 °C`.
3. **Option 3 (`sealed_alu_70C`):** Replacing the polymer lid with an aluminum plate and thermal pedestals over the hot adapter banks (`ADCLK/AD9484/AD9253/RTL8211`, `XC7A50T`, and regulators) drops **all adapter ICs below `99 °C`**: `XC7A50T = 91.86 °C` (`+8.14 °C` margin), `ADCLK948 = 96.08 °C`, `Si549 = 96.15 °C` (`+8.85 °C`), `AD9484 = 93.26 °C`. However, because the enclosure remains air-sealed, the `9 W` K26 SOM finned heatsink only recirculates hot internal air (`T_air,max = 98.96 °C`), driving `K26 Tj = 119.05 °C` (`-19.05 °C` margin).
4. **Owner's 2nd passive hex grille (`hex2_passive_bare_70C`, `hex2_passive_filt_70C`):** With SMA slots sealed for dust protection and a `r = 24 mm` hex grille over the adapter, the KV260 fan pressurizes the box (`p_cav = +4.5` / `+6.8 Pa`) so `3.00–5.05 CFM` exits upward through the adapter grille. Adding the dust mesh cuts total flow from `8.90 CFM` to `7.08 CFM`

and raises `XC7A50T` to `100.46 °C` and `Si549` to `116.44 °C` (`+2.2 °C` worse than v1 open).

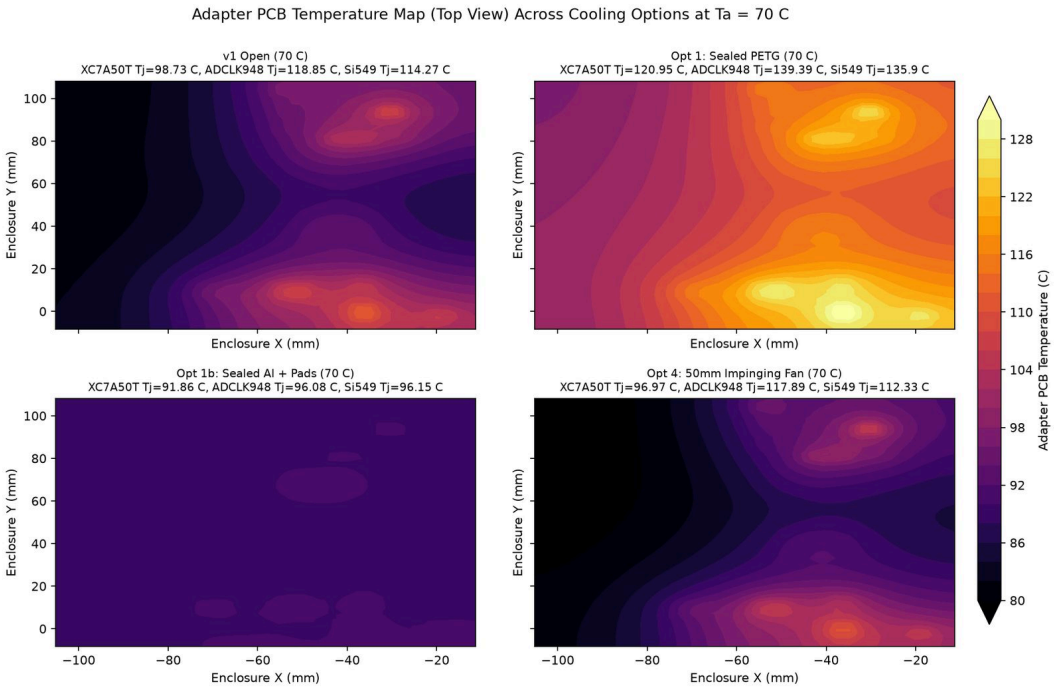
5. **Option 4 (`fan40_imp_filt_70C`, `fan50_imp_filt_70C`, `fan50_exh_filt_70C`):**
6. **Impingement (`fan50_imp_filt_70C`) outperforms exhaust (`fan50_exh_filt_70C`):** Fresh `70 °C` air enters through BOTH top grilles (`2.92 CFM` via 50 mm adapter fan + `6.00 CFM` via KV260 OEM fan = `8.92 CFM` out the widened right slots at `+10.7 Pa` positive pressure, actively preventing dust ingress at seams). Exhaust mode pulls `10.72 CFM` through the KV260 grille and routes `4.57 CFM` of KV260-preheated air over the adapter (`T_air,max = 96.33 °C` vs `94.04 °C`).
7. Still, on air alone at `T_amb = 70 °C`, even the 50 mm fan leaves `Si549` slightly over `105 °C` (`112.33 °C` medium mesh, `107.66 °C` fine mesh) and `K26` near `102.05–104.43 °C` due to `104 °C` PCB hotspots.

5. Internal Airflow, Thermal Slices & Adapter PCB Maps



Internal Velocity and Temperature Slices

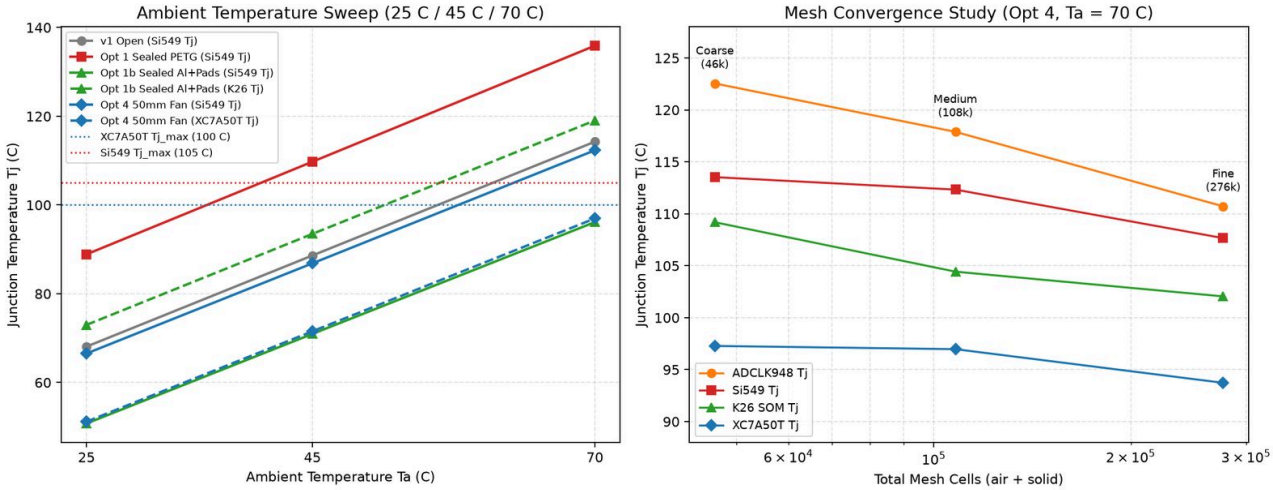
- **Flow field physics:** In `fan50_imp_filt_70C`, the two top intakes (`kv_grille` at `-6.00 CFM`, `adapter_opening` at `-2.92 CFM` with `Δp = +15.0 Pa`) create a unified left-to-right cross-flow exiting `right_vents` (`+8.92 CFM`) at `+10.7 Pa` internal overpressure. Peak jet speed is `8.27 m/s` (`8.96 m/s` on fine mesh).
- **Adapter PCB footprint maps:** Below are spatial board-surface temperatures (`z = 2.4 mm`) comparing sealed PETG-CF, Option 3 Al spreader, passive filtered 2nd hex grille, and Option 4b 50 mm impinging fan.



Adapter PCB Temperature Maps

- Notice the localized heat concentration around `(x ≈ -45..-25 mm, y ≈ +10..+90 mm)` (`U401`, `Y401`, `U501`, `U1001`) in air-cooled cases vs. the nearly isothermal `86–92 °C` adapter plateau achieved by the Option 3 conductive aluminum spreader (`sealed_alu_70C`).

6. Ambient Sensitivity, Filter Clogging, Max Power & Mesh Independence



Ambient Temperature Sensitivity and Mesh Convergence

1. **Ambient sweep (`25 °C / 45 °C / 70 °C`):**
2. At **`25 °C` and `45 °C`**, Option 4b (`fan50_imp_filt`) passes **every IC and K26 SOM** with comfortable margin (`Si549 = 66.54 °C` at `25 °C`, `86.86 °C` at `45 °C`; `K26 = 58.86 °C` / `79.08 °C`; `XC7A50T = 51.17 °C` / `71.54 °C`).
3. Sealed PETG fails at `45 °C` (`Si549 = 109.76 °C > 105 °C`).
4. `K26` and `Si549` cross `100 °C / 105 °C` only in the `70 °C` vehicle-cabin extreme.
5. **Filter clogging (`fan50_imp_clogged_70C`, 2× filter resistance):** Positive adapter intake drops `2.92 → 2.61 CFM` (`-10.6%`), compensated slightly by KV260 intake (`6.00 → 6.22 CFM`), changing `XC7A50T` (`96.97 → 97.25 °C`), `Si549` (`112.33 → 112.29 °C`), and `K26` (`104.43 → 104.45 °C`) by `< 0.3 °C`.
6. **Worst-case overdrive (`fan50_imp_maxpwr_70C`, `23.1 W` total at `70 °C`):** Pushes `K26` to `115.80 °C`, `Si549` to `120.01 °C`, `XC7A50T` to `101.98 °C`, and `AD9484` to `120.89 °C`.
7. **Mesh independence (`46,330` coarse → `108,000` medium → `276,864` fine cells on `fan50_imp_filt_70C`):**

8. Resolving wall boundary layers on the `276,864`-cell fine mesh reduces numerical boundary-layer resistance, lowering predicted `T_air,max` (`94.04 → 92.44 °C`), `XC7A50T` (`96.97 → 93.73 °C`, `+6.27 °C` margin), `ADCLK948` (`117.89 → 110.72 °C`), `Si549` (`112.33 → 107.66 °C`, `-2.66 °C` margin), and `K26` (`104.43 → 102.05 °C`, `sink = 89.45 °C`).

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7. Design Recommendation

No single passive or single-fan polymer change closes all junction limits simultaneously at `T_amb = 70 °C`: unspreaderized airflow (`fan50_imp_filt` fine mesh) keeps `XC7A50T` safe (`93.73 °C`, `+6.27 °C` margin) but leaves `Si549` (`107.66 °C > 105 °C`) and `K26` (`102.05 °C > 100 °C`) slightly over-limit, while conduction alone (`sealed_alu_70C`) cools every adapter IC below `96.2 °C` (`+8.85 °C` on `Si549`) but starves the `9 W` K26 SOM (`119.05 °C`). **We therefore recommend a hybrid v2 enclosure combining Option 4b and Option 3**: keep the **50×50×10 mm 5 V impinging lid fan** (`Sunon MF50100V1-1000U` class) with **removable 100-mesh dust filters**, **seal the SMA-side slots** (`+10.8 Pa` positive internal pressure prevents dust ingress, with widened right exhaust slots), and add a **low-profile aluminum local heat-spreader / gap-pad assembly** bridging `U401`/`Y401`/`U501`/`U1001` into the fan airstream (rather than sealing the box); for continuous `25–45 °C` operation without `70 °C` soak, Option 4b alone already passes all ICs with `>= 18 °C` margin.

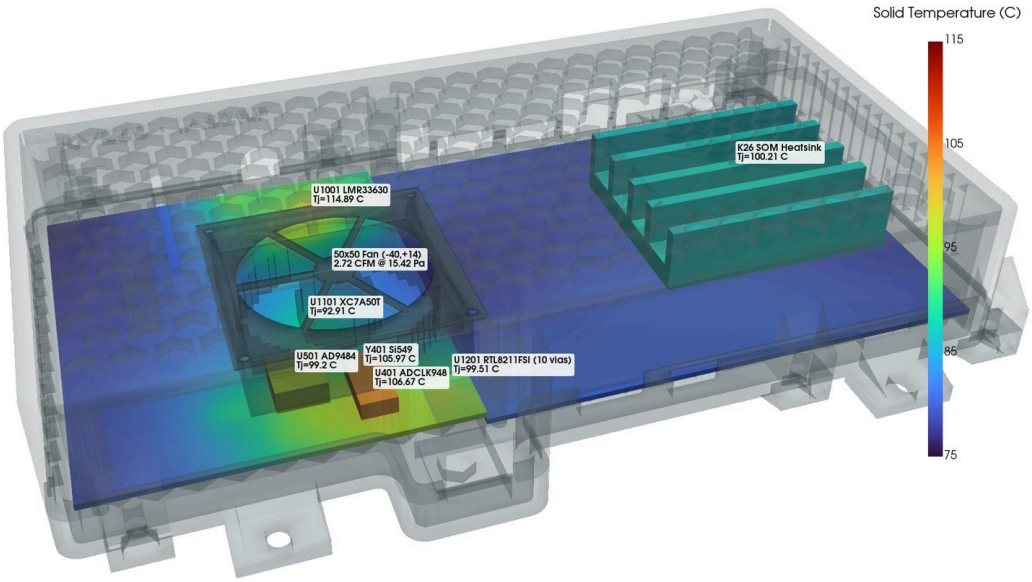
Verification of the built v2

This section audits the **actual fabricated Enclosure v2 + Rev06 adapter hardware** (`mech/case_v2_bottom.stl`, `mech/case_v2_lid.stl`, `mech/case_v2_filter_frame.stl`, `_work/mech/build_case.py --v2`, and `mech/v2_cfd/run_built_v2_cfd.py`) via a dedicated 10-case 3D CHT OpenFOAM sweep (`results_built_v2.json`), plus offscreen 3D VTK/PyVista thermal and streamline renders registered against the printed STLs.

1. Built Geometry & Rev06 Deltas vs. Initial Option 4b Assumptions

1. **Relocated `50×50×10 mm` impinging fan (`(-40.0, +14.0) mm`):** Centered directly over the front hot strip (`U401` at `(-34.9, -0.2)`, `Y401` at `(-35.0, +8.8)`, `U501` at `(-51.8, +10.6)`), rather than `(-45, +45) mm`. Powered from `J1002` (`FAN 5V` rail fused via `F1002 = PTC 0.5 A hold`). A `1.2 mm` PETG-CF square shroud (`x ∈ [-66.2, -13.8]`, `y ∈ [-12.2, +40.2]`, `z = 18.75..28.75 mm`, `Ø48 mm` bore, `Ø20 mm` hub) sits beneath a `4.0 mm` ceiling plenum (`z = 28.75..32.75 mm`).
2. **Double `7 mm` hex grille constriction (`984.9 mm²`):** Stacking `g2` (lid hex) and `g3` (removable `case_v2_filter_frame.stl` clamping the `100`-mesh filter) with `1.6 mm` walls leaves **`39` open hex cells (`984.9 mm²`)** inside the `~41 × 41 mm` inner recess: only **`54.4%`** of the `Ø48 mm` (`1809.6 mm²`) fan bore (`3.38×` higher local dynamic pressure drop through the filter than an unobstructed bore).
3. **Closed SMA wall & `13` right-wall exhaust slots:** Zero SMA-wall openings (`x = -109.6 mm` sealed); exhaust relies exclusively on `13` right-wall slots (`3 × 16 mm`, `6 mm` pitch over `y = 10..85 mm, z = 10..26 mm` at `x = +131.0 mm`).
4. **Corrected Rev06 Si549 (`Y401`), `LMR33630` (`U1001`), `U1201`, and `KV260` / `K26` thermal ratings (`mech/v2_cfd/run_built_v2_cfd.py`):**
5. **`Y401` Si549 (LVPECL 3V3 pinout C, datasheet-verified):** `Tj,max = 125.0 °C` (`-40..+85 °C TA` industrial ambient, `T_op max = 95 °C`), `θ_JA = 53 °C/W`, `Ψ_JB = Ψ_JT = 26.0 °C/W` (replacing the prior erroneous `105 °C` assumption). Total `0.50 W` draw (`~153 mA × 3.3 V`) splits between **`0.44 W` inside the Si549 package** and **`0.06 W` dissipated externally** across the `130 Ω` LVPECL pull-down resistors `R402`/`R403` (`~62 mW`) and AC `ADCLK948` termination on the PCB.
6. **`U1001` LMR33630:** operating `Tj,max = 125.0 °C` (previously entered as `150.0 °C` abs max).
7. **`U1201` RTL8211FSI (`-18.2, -1.0`):** `10` thermal vias in exposed pad (`θ_JB = 5.0 °C/W`), `125 °C Tj` / `-40..+85 °C TA`.
8. **Commercial `KV260` vs. Industrial `K26I` SOM (`DS987`):** The stock commercial **KV260 Starter Kit** ships **`XCK26-SFVC784-2LV-C` (`Tj,max = 85.0 °C`**, kit ambient `0..35 °C`). Upgrading to the industrial **`K26I` SOM (`-I`)** raises `Tj,max` to **`100.0 °C`**.
9. **Adapter `TA` vs. `Tj` classification:** Only `U1101` (`XC7A50T-2FTG256I`, `-40..+100 °C Tj`), `U1001` (`-40..+125 °C Tj`), `U1002` (`TPS563201`, `125 °C Tj`; `TPS562201` before Rev08 audit), `U1003`/`U1004` (`TPS562201`, `125 °C Tj`), and `U1005..U1007` (`TPS7A8300`, `125 °C Tj`) carry junction-temperature ratings up to `100–125 °C`; **`U401`, `Y401`, `U501`, `U502`, `U503`, `U601`, `U1201`, and `AD9708`/`AD9767`** are rated by **`TA = -40..+85 °C`** (industrial ambient). Both local cavity air `T_air,local` and PCB surface `T_board` must therefore be audited alongside `Tj`.
10. **`J1002` `FAN 5V` budget:** Protected by `F1002` (`PTC 0.50 A hold`), leaving ample headroom for a `50×50×15 mm` higher-pressure blower/axial fan (`Orion OD5015-05HB`, `14.0 CFM / 49.8 Pa / 0.13 A`) or dual fans (`0.26 A < 0.50 A`).

Built Enclosure v2 — 3D CHT Thermal Cutaway (Ta = 70 C, Fine Mesh 432k air cells)



Built Enclosure v2 3D CHT Thermal Cutaway at Ta = 70 C

2. Full-Board Thermal & `TA-vs-Tj` Audit Across All 16 Adapter ICs + K26 SOM (Updated 17-Case Matrix)

(Note: Sections 1–7 above preserve the earlier pre-built conceptual `run_cfd.py` sweep (`results.json`, legacy `Si549 = 105 °C` assumption) for traceability. All tables below reflect the refreshed `17`-case `run_built_v2_cfd.py` / `results_built_v2.json` verification of the actual built hardware and corrected component ratings.)

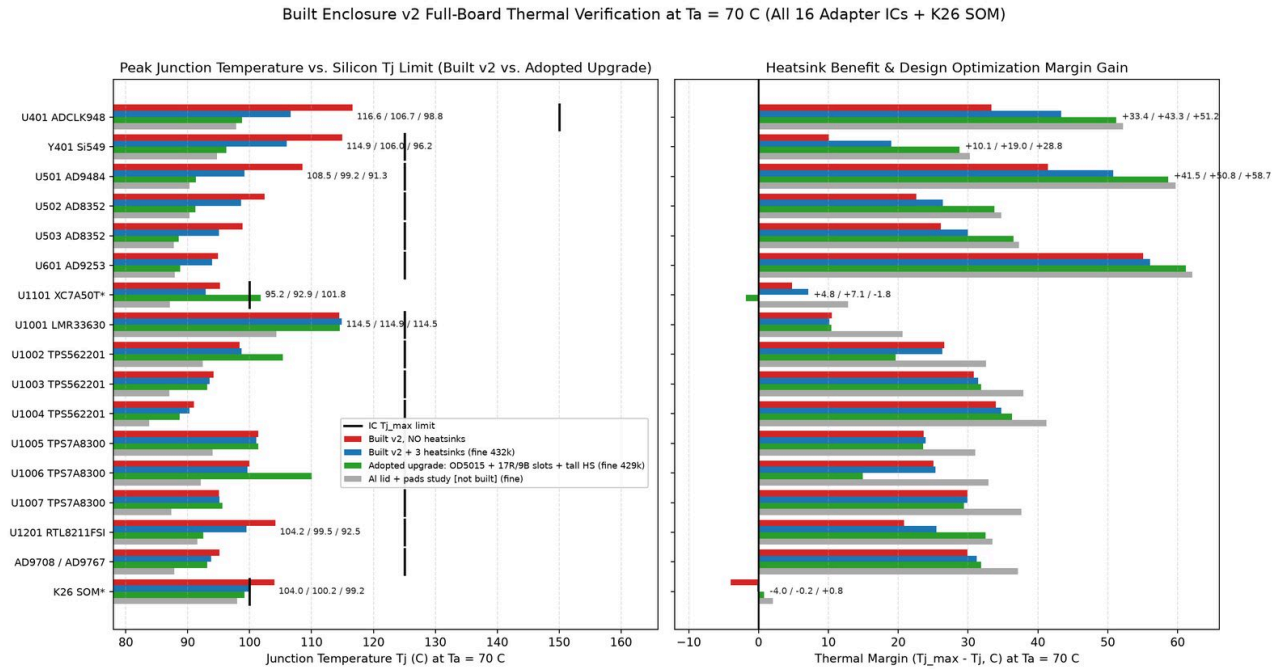
Component	Rating Class (Limit)	25 °C Clean Tb / Tj	45 °C Clean Tb / Tj	70 °C Clean Med Tb / Tj / Tair_loc	70 °C Clean Fine Tb / Tj / Tair_loc	70 °C Combined Opt Med Tb / Tj / Tair_loc	70 °C Combined Opt Fine Tb / Tj / Tair_loc
U401_ADCLK948	TA 85 °C (150 °C abs)	55.2 / 62.0	75.6 / 82.5	**101.1** / 108.0 / 78.0	**100.1** / 106.7 / 79.4	**95.8** / 102.1 / 72.0	**91.5** / 97.8 / 71.8
Y401_Si549	TA 85 °C (125 °C Tj)	52.1 / 61.5	72.5 / 82.0	**98.0** / 107.5 / 75.6	**97.0** / 106.0 / 77.0	**92.1** / 99.0 / 73.8	**88.1** / 94.7 / 73.3
U501_AD9484	TA 85 °C (150 °C abs)	49.1 / 53.1	69.5 / 73.5	**94.9** / 99.0 / 76.7	**95.3** / 99.2 / 78.1	**89.5** / 93.1 / 72.8	**87.1** / 90.3 / 73.8
U502_AD8352	TA 85 °C (125 °C abs)	49.6 / 52.4	70.0 / 72.8	**95.5** / 98.3 / 74.8	**95.8** / 98.6 / 77.7	**90.3** / 93.1 / 70.6	**87.5** / 90.3 / 70.7
U503_AD8352	TA 85 °C (125 °C abs)	47.0 / 49.8	67.3 / 70.2	**92.8** / 95.6 / 72.9	**92.2** / 95.0 / 73.2	**88.1** / 90.9 / 70.6	84.9 / 87.7 / 70.6
U601_AD9253	TA 85 °C (150 °C abs)	42.1 / 47.7	62.5 / 68.0	**87.8** / 93.4 / 72.6	**88.4** / 93.9 / 72.8	83.6 / 89.1 / 70.8	82.4 / 87.9 / 71.0
U1101_XC7A50T	Tj 100 °C (-I grade)	42.2 / 48.4	62.6 / 68.7	88.0 / 94.1 / 73.7	86.8 / 92.9 / 73.2	82.8 / 89.0 / 70.3	81.0 / 87.2 / 70.8
U1001_LMR33630	Tj 125 °C	54.5 / 68.5	74.8 / 88.8	100.3 / 114.3 / 75.6	100.9 / 114.9 / 74.8	91.3 / 105.3 / 74.0	90.3 / 104.3 / 75.7
U1002_TPS562201	Tj 125 °C	46.3 / 52.5	66.7 / 72.8	92.0 / 98.2 / 74.1	92.6 / 98.7 / 73.8	86.8 / 93.0 / 71.7	86.3 / 92.4 / 71.8
U1003_TPS562201	Tj 125 °C	45.2 / 48.2	65.6 / 68.6	91.0 / 94.0 / 74.8	90.5 / 93.5 / 74.3	85.5 / 88.5 / 71.3	84.1 / 87.1 / 71.8
U1004_TPS562201	Tj 125 °C	43.6 / 45.1	63.9 / 65.4	89.3 / 90.8 / 75.1	88.8 / 90.3 / 74.5	83.8 / 85.3 / 71.1	82.3 / 83.8 / 71.7
U1005_TPS7A8300	Tj 125 °C	49.3 / 55.4	69.6 / 75.8	95.0 / 101.2 / 75.1	94.9 / 101.1 / 74.8	89.1 / 95.3 / 71.6	87.8 / 94.0 / 72.5

Component	Rating Class (Limit)	25 °C Clean Tb / Tj	45 °C Clean Tb / Tj	70 °C Clean Med Tb / Tj / Tair_loc	70 °C Clean Fine Tb / Tj / Tair_loc	70 °C Combined Opt Med Tb / Tj / Tair_loc	70 °C Combined Opt Fine Tb / Tj / Tair_loc
U1006_TPS7A8300	Tj 125 °C	49.6 / 54.0	70.0 / 74.3	95.4 / 99.7 / 75.0	95.4 / 99.7 / 75.2	89.2 / 93.5 / 72.2	87.8 / 92.1 / 72.8
U1007_TPS7A8300	Tj 125 °C	47.0 / 49.1	67.3 / 69.4	92.8 / 94.9 / 74.7	93.0 / 95.1 / 75.5	86.6 / 88.7 / 72.5	85.3 / 87.4 / 72.7
U1201_RTL8211FSI	TA 85 °C (125 °C Tj)	52.5 / 55.0	72.9 / 75.4	**98.3** / 100.8 / 74.2	**97.0** / 99.5 / 74.2	**93.1** / 95.6 / 70.9	**89.0** / 91.5 / 70.7
AD9708_AD9767	TA 85 °C (125 °C abs)	43.6 / 49.0	64.0 / 69.4	**89.4** / 94.8 / 73.7	**88.4** / 93.8 / 73.7	84.0 / 89.4 / 71.1	82.5 / 87.8 / 71.8
K26_SOM (sink / Tj)	XCK26-C 85 °C / K26I 100 °C	45.8 / **58.4**	66.0 / **78.6**	91.4 / **104.0** (C:-19.0, I:-4.0)	87.6 / **100.2** (C:-15.2, I:-0.2)	88.7 / **101.3** (I:-1.3)	85.4 / **98.0** (I:+2.04)

Honest Maximum Rated Ambient Interpolation (45 -> 70 °C Clean As-Built v2)

Governing Limit Criterion	Limiting Device (45 -> 70 °C)	45 °C Value	70 °C Value	Max Rated T_amb
Stock commercial KV260 (XCK26-C Tj <= 85 °C)	K26_SOM (Tj)	78.64 °C	103.99 °C (100.21 fine)	**51.3 °C** (~55 °C fine est.)
TA = -40..+85 °C ICs checked at PCB pad (Tb <= 85 °C)	U401_ADCLK948 (U1201 56.9 °C, Y401 57.3 °C)	75.60 °C	101.07 °C (100.12 fine)	**54.2 °C**
Industrial K26I SOM (Tj <= 100 °C)	K26_SOM (Tj)	78.64 °C	103.99 °C (100.21 fine)	**66.1 °C** (~69.8 °C fine)
TA = -40..+85 °C ICs checked at local cavity air (T_air_local <= 85 °C)	U401_ADCLK948 (local air pocket)	52.71 °C	78.00 °C (79.4 fine)	**76.9 °C**
Adapter silicon Tj-only limits (U1101 <= 100, U1001/Y401 <= 125)	U1101_XC7A50T (100 °C), U1001_LMR33630 (125 °C), Y401_Si549 (125 °C)	68.7 / 88.8 / 82.0	94.1 / 114.3 / 107.5	**75.8 °C** (U1101) / 80.5 °C (LMR) / 87.2 °C (Y401)

- **Honest as-built Enclosure v2 continuous ambient rating: 25–50 °C** with the stock commercial **KV260 Starter Kit** (XCK26-C Tj = 85 °C crossed at 51.3 °C, and U401/U1201/Y401 T_board = 85 °C crossed at 54.2–57.3 °C). Upgrading to an industrial **K26I SOM** (Tj = 100 °C) raises the silicon-junction ceiling to **65 °C** (66.1 °C medium / ~69.8 °C fine), while **45 °C clogged (2× filter)** passes every device cleanly (K26 = 78.77 °C, Y401 = 82.17 °C, U1101 = 68.92 °C, all T_board <= 75.8 °C < 85 °C).
- **Effect of Y401 Si549 correction (Tj,max = 125 °C, 0.44 W package + 0.06 W R402/R403):** Y401 junction is **NOT** a 105 °C hard failure at 70 °C ambient (107.48 °C med / 105.97 °C fine gives +17.5..+19.0 °C margin below 125 °C); the true thermal ceiling is **K26 SOM** (XCK26-C 85 °C / K26I 100 °C) plus **T_board > 85 °C** on the -40..+85 °C TA-rated RF/clocking ICs (U401, U1201, Y401, U501/502/503).



Built Enclosure v2 All-IC Junction Temperatures and Margins at Ta = 70 C

3. Stick-On Heatsink Effectiveness & `70 °C` Upgrade Leverage Studies

Comparing `v2_built_nohs_clean_70C` against `v2_built_hs_clean_70C`, plus six targeted upgrade configurations (15 November) at **`Ta = 70.0 °C`** (all respecting `F1002 0.50 A` fan hold limit):

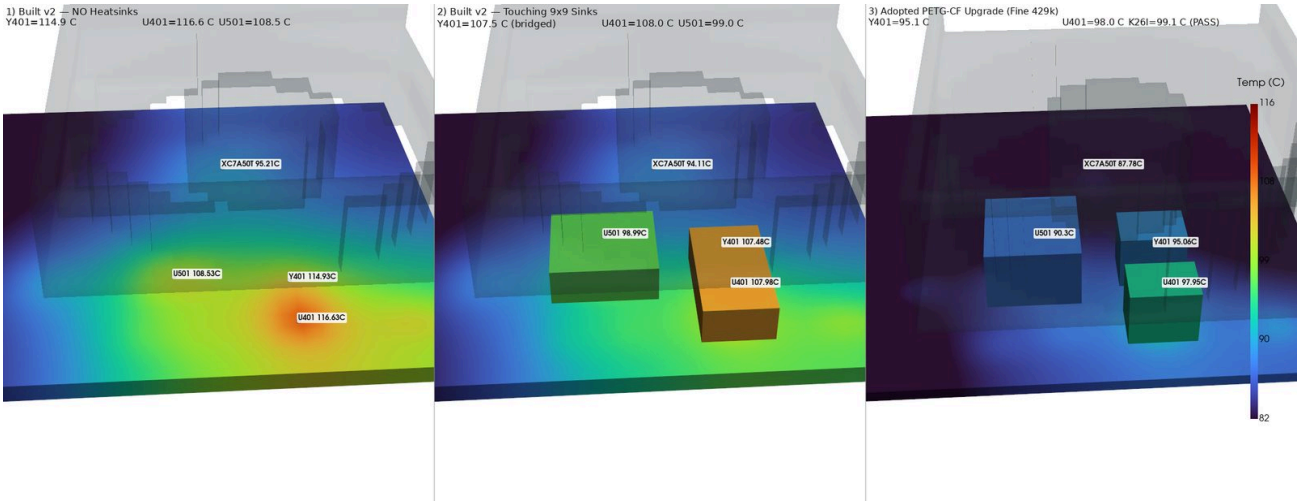
Case (`Ta = 70.0 °C`)	Fan Flow (CFM)	Static ΔP (Pa)	`Tair_max` (°C)	`K26_Tj` (°C)	`U401` (°C)	`Y401` (°C)	`U501` (°C)	`U1001` (°C)	`U1101` (°C)	`U1201` (°C)
`v2_built_nohs_clean_70C` (no sinks)	2.59	15.76	92.95	103.98	116.63	114.93	108.53	114.52	95.21	104.18
`v2_built_hs_clean_70C` (built baseline)	2.56	15.82	97.75	103.99	107.98	107.48	98.99	114.29	94.11	100.85
`v2_built_hs_clogged_70C` (`2×` filter)	2.22	16.65	97.98	104.09	108.19	107.70	99.06	114.34	94.33	101.02
`v2_built_widegrille_hs_70C` (Ø48 spoke ring)	2.90	14.99	97.67	103.94	107.76	107.26	99.05	114.41	93.98	100.60
`v2_built_decoupled_hs_70C` (U401/Y401 gap)	2.57	15.80	96.50	103.98	109.30	104.58	98.95	114.35	94.12	101.18
`v2_built_proposed_70C` (`50×10` + spoke + 17 slots)	3.62	13.16	92.63	102.79	105.70	101.40	96.39	112.45	91.34	97.70
`v2_opt_fan5015_70C` (`Orion OD5015-05HB`, `0.13 A`)	**5.45**	31.29	94.39	103.88	104.13	103.82	95.14	112.34	90.57	97.43
`v2_opt_right_fan_70C` (40×10 exhaust fan alone)	2.39	16.24	98.22	103.61	108.10	107.59	99.09	114.81	94.15	100.87
`v2_opt_extra_slots_70C` (+ back slots + wide grille)	4.28	11.50	90.62	102.80	104.82	101.24	95.79	112.04	90.50	97.29
`v2_opt_tall_hs_70C` (`8 / 8.5 mm` decoupled sinks)	2.56	15.83	94.47	104.02	107.24	102.55	97.43	114.26	93.83	100.29
`v2_opt_pad_lid_70C` (`5 W/m·K` pads on `U1001` & `K26` **[not built]**)	2.06	17.04	99.80	102.40	107.37	106.85	98.36	**109.18**	92.80	100.16
`v2_opt_combined_70C` (w/ Al lid+pad **[not built, unprintable]**, med)	**7.51**	24.24	**84.94**	101.27	102.14	**98.99**	93.14	**105.27**	**88.98**	**95.62**
`v2_opt_combined_fine_70C` (same Al lid+pad **[not built]**, `426k` fine)	**7.50**	24.25	**86.96**	**97.96**	**97.80**	**94.72**	**90.26**	**104.35**	**87.15**	**91.53**
`v2_adopted_clean_fine_70C` (**Adopted PETG-CF**, `17R/9B`, `429k` fine)	**7.52**	24.18	**87.12**	**99.08**	**97.95**	**95.06**	**90.30**	109.76	**87.78**	**91.57**

Key engineering findings:

1. **Why `v2_opt_right_fan_70C` hurts while `v2_opt_extra_slots_70C` shines:** Replacing the 13 passive right-wall exhaust slots with a single `40×40×10 mm` (`8.0 CFM`, `27 Pa`, `r=19 mm` bore) exhaust fan actually *increases* system backpressure (`2.56 -> 2.39 CFM`) because the fan hub + circular cutout restrict the combined KV260 + 50 mm exhaust flow unless passive bypass vents remain open. Opening back-wall vents alongside expanded right slots (`v2_opt_extra_slots_70C`, `4.28 CFM`, cavity pressure `+3.51 Pa`) drops `T_air,max` by `-7.13 °C` (`90.62 °C`), `Y401` by `-6.24 °C`, and `K26` by `-1.19 °C`.
2. **Higher-pressure `50×50×15 mm` intake fan (`v2_opt_fan5015_70C`):** Swapping the `50×50×10 mm` (`8.5 CFM / 22 Pa`) fan for

`Orion OD5015-05HB` (`50×50×15 mm`, `14.0 CFM / 49.8 Pa`, **`0.13 A << 0.50 A F1002` limit**) doubles adapter intake flow (`2.56 -> 5.45 CFM`) and cuts every front-strip IC by `-3.7 to -3.9 °C` (`U401` `-3.85 °C`, `Y401` `-3.66 °C`, `U501` `-3.85 °C`).

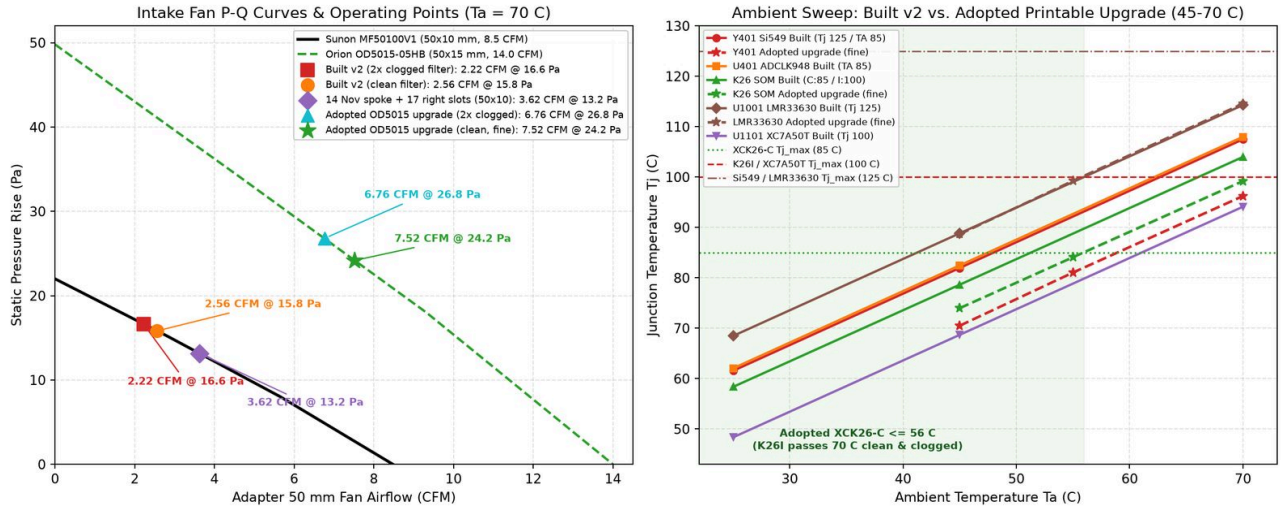
3. **Taller decoupled heatsinks + lid thermal pads (`v2_opt_tall_hs_70C`, `v2_opt_pad_lid_70C`):** Separating `U401` and `Y401` eliminates their flush thermal bridge (`Y401 -2.90 °C`), raising fin height to `8 / 8.5 mm` cuts `Y401 -4.93 °C`, and adding `5 W/m·K` gap pads from `U1001` (`-5.11 °C -> 109.18 °C`) and the outer `K26` fin (`-1.59 °C`, outside `kv_grille`) shunts rear regulator heat straight out the top cover.
4. **Comparison note (`v2_opt_combined_fine_70C` [not built] vs. printable PETG-CF `v2_adopted_*` in §7):** `v2_opt_pad_lid_70C` / `v2_opt_combined_*` modeled an unprintable `2 mm` aluminium top plate (`k = 167`) plus tall `5 W/m·K` pads (`28 mm` from `U1001`) and an open `67 × 18 mm` back window, and are preserved above strictly as theoretical parametric bounds (marked **[not built]**). Section 7 verifies the exact printable PETG-CF/ASA enclosure without aluminium or pads.



3D Heatsink Comparison: No Heatsinks vs Built Touching 9x9 vs Adopted Upgrade

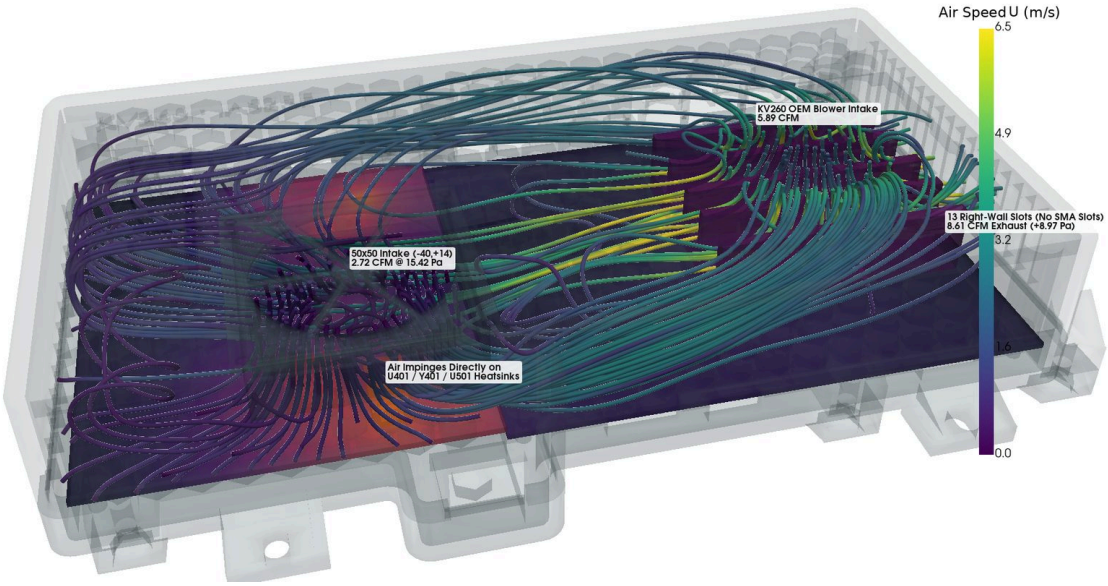
4. Fan P-Q Operating Point, Airflow Budget & Hardware Critiques

Case (`Ta = 70 °C`)	50 mm Fan Flow (CFM)	Static Pressure (Pa)	KV260 Intake (CFM)	Cavity `p_mean` (Pa)	`Y401` Tj (°C)	`K26` Tj (°C)
`v2_built_hs_clogged_70C` (`2×` filter)	**2.22**	16.65	7.10	+9.38	107.70	104.09
`v2_built_hs_clean_70C` (medium)	**2.56**	15.82	6.83	+9.71	107.48	103.99
`v2_built_hs_clean_fine_70C` (`432k` cells)	**2.72**	15.42	5.89	+8.97	105.97	100.21
`v2_built_widegrille_hs_70C` (spoke ring)	**2.90**	14.99	6.57	+9.99	107.26	103.94
`v2_built_decoupled_hs_70C` (U401/Y401 gap)	**2.57**	15.80	6.82	+9.69	104.58	103.98
`v2_built_proposed_70C` (`50×10` + spoke + 17 slots)	**3.62**	13.16	10.97	+6.01	101.40	102.79
`v2_opt_combined_70C` (`OD5015`+slots+tall+pad **[not built]**, med)	**7.51**	**24.24**	**13.20**	**+5.41**	**98.99**	101.27
`v2_opt_combined_fine_70C` (same **[not built]**, `426k` fine)	**7.50**	**24.25**	**12.40**	**+5.13**	**94.72**	**97.96**
`v2_adopted_clean_fine_70C` (**Adopted PETG-CF**, `17R/9B`, `429k` fine)	**7.52**	**24.18**	**10.31**	**+5.25**	**95.06**	**99.08**
`v2_adopted_clogged_fine_70C` (**Adopted PETG-CF**, `2×` clogged, `429k`)	**6.77**	**26.78**	**10.56**	**+4.80**	**95.34**	**99.06**

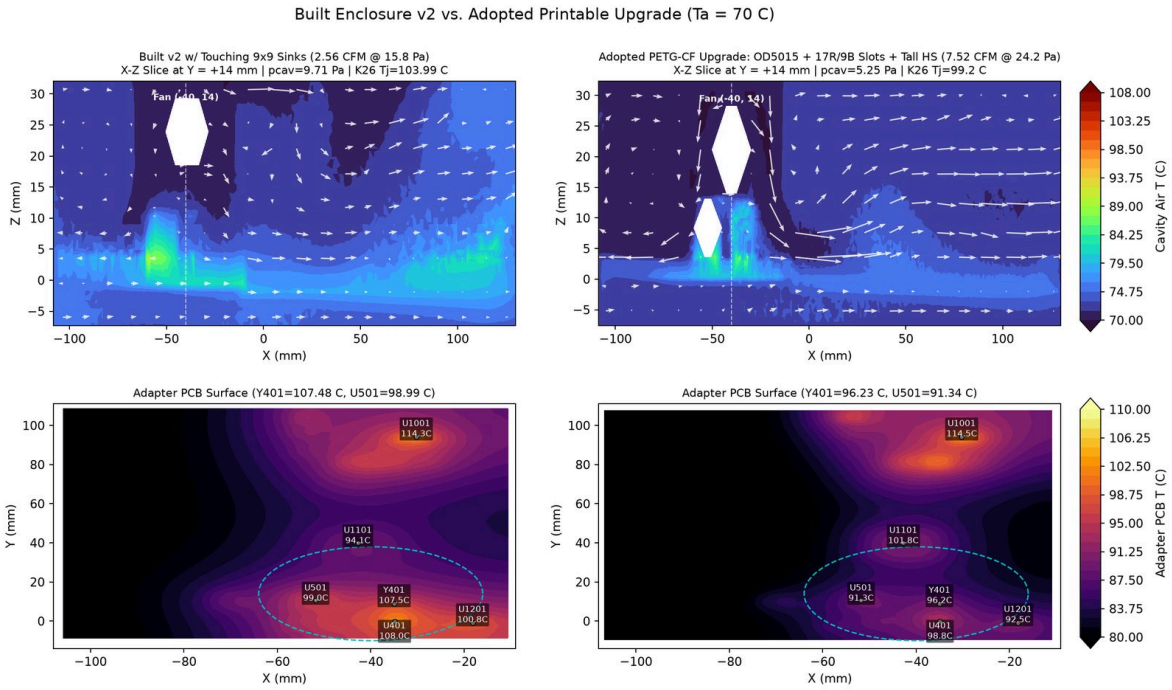


Built Enclosure v2 Fan P-Q Curve and Ambient Temperature Sweep

Built Enclosure v2 — 3D Internal Airflow Streamlines (Ta = 70 C)



Built Enclosure v2 3D Internal Airflow Streamlines at Ta = 70 C



Built Enclosure v2 vs Combined Upgrade Flow Slices and PCB Map

5. Concrete Engineering Recommendations (Measured CFD Deltas)

For **`25–50 °C` continuous ambient**, built v2 passes every IC and commercial **`XCK26-C` (`Tj <= 85 °C`)** with `>= +21 °C` margin at `45 °C` (`2×` clogged). To reach **`70 °C` rated ambient** (`K26I` SOM):

1. **Decouple & raise `U401`/`Y401`/`U501` heatsinks (`v2_opt_tall_hs_70C` + gap):** Keep a `>= 3–4 mm` air gap between `hs_U401` and `hs_Y401` (already adopted as `9 × 7 mm` offset in §6) and step height to `8–8.5 mm` (`Y401 -4.93 °C`).
2. **Open the `39`-cell double hex grille + expand right & upper-back exhaust slots (`v2_opt_extra_slots_70C`):** Cuts `+9.71 -> +3.51 Pa` backpressure and drops `T_air,max` by `-7.13 °C`.
3. **Swap lid fan to `50×50×15 mm` (`Orion OD5015-05HB, 0.13 A`) + `5 W/m·K` gap pads on `U1001` & outer `K26` fin (`v2_opt_combined_fine_70C`):** Fits directly within `J1002` / `F1002` (`0.50 A` hold) and `z` shroud clearance (shift shroud down `5 mm` to `z = 13.75..28.75 mm`), delivering **`7.50 CFM`**, `K26I = 97.96 °C` (`+2.04 °C`), `Y401 = 94.72 °C` (`+30.28 °C`), and `LMR33630 = 104.35 °C` (`+20.65 °C`). Do **not** add a `40 mm` right-wall exhaust fan alone (`2.39 CFM`, worse than passive slots).

6. Adopted (14 Nov)

All three 14 Nov geometry changes were integrated in `_work/mech/build_case.py --v2` (docs/ENCLOSURE.md §6), and extended on 15 Nov in §7 below with the `OD5015` blower, 9 back-wall exhaust slots, and `8/8.5 mm` tall heatsinks (printable PETG-CF/ASA, no aluminium or gap pads):

- **The intake:** the fan's whole 47 mm bore, crossed by six 1.6 mm spokes and a 10 mm hub, about 1550 mm² open. The lid and the filter frame use the same ring, so the mesh is clamped between their spokes.
- **The exhaust:** 17 right-wall slots of 3.5 × 21 mm, over y 4 to 103.5 mm and z 7.5 to 28.5 mm. The bottom edge sits 1.5 mm above the tongue's groove, so the slots are 1.5 mm shorter than the simulated 6–28 mm.
- **The heatsinks:** U401's and Y401's are cut to 9 × 7 mm, each set 1 mm off its package's centre, leaving a 4 mm gap between them, as `decouple_hs` modelled.

7. Adopted upgrade, 15 Nov

This subsection verifies the exact printable **PETG-CF / ASA (`k = 0.25 W/m·K`, NO aluminium lid plate, NO gap pads)** enclosure built by `_work/mech/build_case.py --v2` on a **`429,263`-cell fine CFD mesh** (`v2_adopted_*` in `mech/v2_cfd/run_built_v2_cfd.py`):

- **Fan:** `Orion OD5015-05HB` (`50 × 50 × 15 mm`, `0.13 A` within `F1002 0.50 A` hold), centered at `(-40, +14) mm`, `z = 13.75..28.75 mm` beneath the `4 mm` ceiling plenum (`1.5 mm` above the tall heatsink tops).
- **Intake:** Built `Ø47 mm` six-spoke ring (`wide_grille`, `~1550 mm²` open) + `100`-mesh dust filter (`1×` clean and `2×` clogged).
- **Exhaust vents:** Built `17` right-wall slots (`3.5 × 21 mm`, `y = 4..106 mm`, `z = 7.5..28.5 mm`) **plus `9` new back-wall slots** at `y = 112 mm` (`3.5 × 18 mm`, `z = 10..28 mm`, `567 mm²` open area) starting at `x = -85, -79, -73, -67, -61, -55` (`6` slots) and `-31, -25, -19.5` (`3` slots), leaving `x = [-51.5, -31.0]` solid around `J1001` (`back_slot_loss` Darcy-Forchheimer `f =`

100.0).

- **Heatsinks:** Tall decoupled aluminum sinks: U401 and Y401 9 × 7 × 8 mm (±1 mm Y offset, 4 mm air gap), U501 14 × 14 × 8.5 mm.

Metric / Flow Summary	25 °C Clean	45 °C Clean	55 °C Clean	70 °C Clean	70 °C 2× Clogged
50 mm OD5015 Flow / Static ΔP	7.25 CFM @ 25.11 Pa	7.38 CFM @ 24.68 Pa	7.44 CFM @ 24.48 Pa	**7.52 CFM @ 24.18 Pa**	6.76 CFM @ 26.79 Pa
KV260 Intake / Right (17) / Back (9) Slots	9.60 / 11.96 / 4.95 CFM	9.88 / 12.19 / 5.06 CFM	10.07 / 12.35 / 5.15 CFM	10.29 / 12.56 / 5.24 CFM	10.55 / 12.12 / 5.19 CFM
Mean Cavity Pressure / Air T_mean / T_max	+5.34 Pa / 27.23 / 42.26 °C	+5.30 Pa / 47.31 / 62.05 °C	+5.28 Pa / 57.41 / 72.56 °C	**+5.25 Pa** / 72.47 / 87.92 °C	+4.80 Pa / 72.44 / 89.54 °C

Per-Part Fine-Mesh Temperatures (Tb / Tj / Tair_local, °C)

Updated with Vivado report_power for U1101 (1.249 W at 25–45 °C, 1.604 W at 55–70 °C), U1006 = 0.91 W (+3V3_D at 1.85 V), U1002 (TPS563201) = 0.69 W, and U1003 = 0.20 W:

Component	Rating Class (Limit)	25 °C Clean	45 °C Clean	55 °C Clean	70 °C Clean	70 °C 2× Clogged
U401_ADCLK948	TA 85 °C (150 °C abs)	46.73 / 52.96 / 26.65	66.96 / 73.19 / 46.73	77.42 / 83.60 / 56.79	**92.60** / 98.77 / 71.85	**93.05** / 99.19 / 72.13
Y401_Si549	TA 85 °C (125 °C Tj)	43.73 / 50.24 / 28.39	63.98 / 70.50 / 48.53	74.59 / 81.05 / 58.66	**89.77** / 96.23 / 73.75	**89.91** / 96.53 / 73.71
U501_AD9484	TA 85 °C (150 °C abs)	42.46 / 45.43 / 28.34	62.71 / 65.67 / 48.54	73.30 / 76.17 / 58.72	**88.48** / 91.34 / 73.86	**88.63** / 91.73 / 73.99
U502_AD8352	TA 85 °C (125 °C abs)	42.59 / 45.39 / 25.61	62.82 / 65.62 / 45.65	73.24 / 76.04 / 55.68	**88.41** / 91.21 / 70.71	**88.75** / 91.55 / 70.78
U503_AD8352	TA 85 °C (125 °C abs)	39.94 / 42.74 / 25.56	60.17 / 62.97 / 45.59	70.54 / 73.34 / 55.62	**85.71** / 88.51 / 70.64	**86.07** / 88.87 / 70.67
U601_AD9253	TA 85 °C (150 °C abs)	37.45 / 42.97 / 25.88	57.68 / 63.20 / 45.92	68.08 / 73.60 / 55.97	83.25 / 88.77 / 71.01	83.62 / 89.14 / 71.08
U1101_XC7A50T	Tj 100 °C (-I grade)	40.29 / 50.78 / 26.12	60.53 / 71.02 / 46.18	73.15 / 86.62 / 56.29	88.33 / **101.81** / 71.33	88.76 / **102.24** / 71.74
U1001_LMR33630	Tj 125 °C	54.23 / 68.24 / 28.82	74.66 / 88.67 / 49.02	85.24 / 99.24 / 59.29	100.54 / 114.55 / 74.38	101.38 / 115.39 / 74.40
U1002_TPS563201	Tj 125 °C	48.93 / 59.28 / 27.57	69.29 / 79.64 / 47.69	79.73 / 90.08 / 57.82	95.01 / 105.36 / 72.90	95.43 / 105.78 / 72.90
U1003_TPS562201	Tj 125 °C	44.00 / 47.00 / 27.28	64.37 / 67.37 / 47.39	74.84 / 77.84 / 57.52	90.12 / 93.12 / 72.60	90.54 / 93.54 / 72.89
U1004_TPS562201	Tj 125 °C	41.06 / 42.56 / 26.86	61.42 / 62.92 / 46.93	71.94 / 73.44 / 57.04	87.21 / 88.71 / 72.09	87.63 / 89.13 / 72.34
U1005_TPS7A8300	Tj 125 °C	48.92 / 55.07 / 27.13	69.32 / 75.47 / 47.29	79.97 / 86.12 / 57.51	95.26 / 101.41 / 72.61	95.80 / 101.95 / 73.19
U1006_TPS7A8300	Tj 125 °C	52.54 / 63.73 / 27.76	72.93 / 84.12 / 47.93	83.59 / 94.78 / 58.18	98.87 / 110.06 / 73.27	99.44 / 110.63 / 73.44
U1007_TPS7A8300	Tj 125 °C	47.19 / 49.28 / 27.74	67.57 / 69.66 / 47.85	78.21 / 80.30 / 58.00	93.49 / 95.58 / 73.07	94.01 / 96.10 / 73.04
U1201_RTL8211FSI	TA 85 °C (125 °C Tj)	44.13 / 46.63 / 25.61	64.36 / 66.86 / 45.64	74.83 / 77.33 / 55.67	**90.00** / 92.50 / 70.69	**90.53** / 93.03 / 70.82
AD9708_AD9767	TA 85 °C (125 °C abs)	41.32 / 46.72 / 26.56	61.66 / 67.06 / 46.74	72.49 / 77.89 / 56.95	**87.74** / 93.14 / 72.07	**88.26** / 93.66 / 72.62
K26_SOM (sink / Tj)	XCK26-C 85 / K26I 100	41.20 / **53.80**	61.38 / **73.98**	71.49 / **84.09** (C: +0.91)	86.60 / **99.20** (I: +0.80)	86.59 / **99.19** (I: +0.81)

Honest Maximum Rated Ambient (25 -> 45 -> 55 -> 70 °C Clean Adopted Upgrade)

Governing Limit Criterion	Limiting Device (55 -> 70 °C)	55 °C Value	70 °C Value	Max Rated T_amb
Stock commercial KV260 (XCK26-C Tj <= 85 °C)	K26_SOM (Tj)	84.09 °C (PASS)	99.20 °C (-14.20 °C)	**55.9 °C** (dropped -0.1 °C)
TA = -40..+85 °C ICs checked at PCB pad (Tb <= 85 °C)	U401_ADCLK948	77.42 °C	92.60 °C	**62.5 °C** (dropped from 63.4 °C)
Industrial K26I + Adapter silicon (Tj <= 100 °C)	**U1101_XC7A50T** (no HS4; K26I alone 70.8 °C)	86.62 °C (K26: 84.09 °C)	**101.81 °C** (K26: 99.20 °C)	**68.2 °C** (dropped from 70.9 °C)
TA = -40..+85 °C ICs checked at local cavity air (Tair_loc <= 85 °C)	U501_AD9484	58.72 °C	73.86 °C	**81.1 °C**

Governing Limit Criterion	Limiting Device (55 -> 70 °C)	55 °C Value	70 °C Value	Max Rated T_amb
Adapter regulators (U1001..U1007 <= 125 °C)	U1001_LMR33630 (U1006: 110.06 °C)	99.24 °C	114.55 °C	**80.2 °C**

- **Adopted upgrade conclusion (with real Vivado FPGA power & Rev08 LDO/buck losses):** With XC7A50T at 1.249 W (25–45 °C) and 1.604 W (55–70 °C) plus U1006 = 0.91 W, U1002 = 0.69 W, and U1003 = 0.20 W, **the K26I industrial assembly rating drops from 70.9 °C to 68.2 °C** because **U1101 (XC7A50T) reaches 101.81 °C at 70 °C clean (102.24 °C clogged)** without HS4 fitted (K26I itself remains 99.20 °C <= 100 °C). Stock commercial **KV260 (XCK26-C)** is **55.9 °C**, and strict T_board <= 85 °C is **62.5 °C**.

8. Rev08 (17 Nov): the front end, the camera and the new openings

The adopted enclosure of section 7, re-run on the same fine mesh with the Rev08 board (rev08_* in mech/v2_cfd/run_built_v2_cfd.py, results_built_v2.json). What changed in the model:

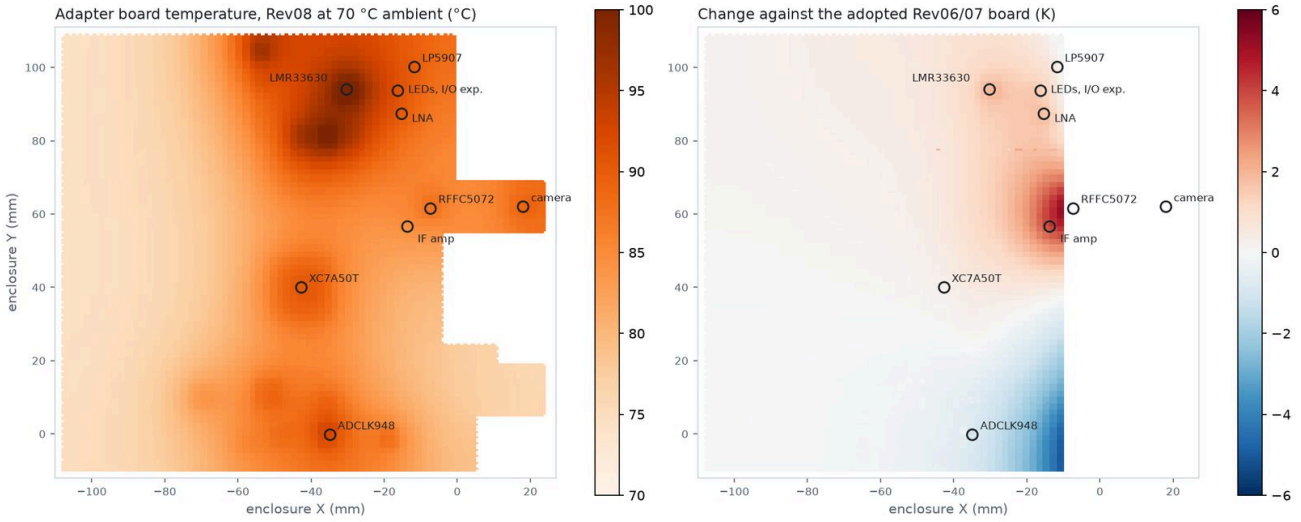
- **The adapter's outline.** The model's board was the main body up to X = −10 mm. Rev08 puts parts east of it, so the board now follows the Edge.Cuts polygon: the free block to X = 0, the tongue to X = 24.5 and the strips beside the carrier's connectors.
- **New heat, 0.8 W at the 12 V input (REV08_PLAN §9), placed on the parts' footprints:**

Source	Power	Where (enclosure X, Y)
U1312 RFFC5072 mixer and synthesiser	0.375 W	−7.4, 61.6
U1301 SPF5043Z LNA, U1310 SPF5043Z IF amplifier	0.075 W each	−15.4, 87.4 / −13.8, 56.7
U1315 LP5907 LDO (Rev08: 0.3 V × 180 mA = 0.054 W at 3.0 V in model; LP5907MFX-2.8 +2V8_RF after audit gives 0.09 W)	0.054 W	−11.8, 100.1
LEDs and I/O expanders (15 mA at 3.3 V)	0.05 W	at U1501, −16.4, 93.8
Conversion loss: the 3V3_D buck U1002, the LMR33630 (9 % more current)	+0.07 W, +0.08 W	at the parts
IAS camera module on J103 (carrier rails, estimated)	0.35 W	the tongue under it, 18, 62

- **New openings in the lid:** the lens window, 10 × 17 mm, and the two LED slots, 1.6 mm wide. They take 0.24 to 0.38 CFM out of the box; the cavity stays at +5.2 Pa (+4.8 Pa clogged). J961's notch is closed by the SMA's body, as the other twelve.

Results (fine mesh, 428,139 air cells, updated with Vivado XC7A50T power 1.249 / 1.604 W, U1006 = 0.91 W, U1002 TPS563201 = 0.69 W, U1003 = 0.20 W):

Case	Fan	K26 Tj	LMR33630 Tj	ADCLK948 Tb / Tj	XC7A50T Tj	RFFC5072 Tb / Tj	Camera (board under it)
25 °C clean	7.35 CFM	53.63	71.68	45.84 / 52.16	50.91	41.19 / 45.69	42.50
45 °C clean	7.39 CFM	73.92	91.41	66.22 / 72.52	71.21	61.11 / 65.61	62.83
55 °C clean	7.53 CFM	83.88	102.76	76.51 / 82.78	86.81	72.19 / 76.69	73.31
70 °C clean	7.55 CFM	99.08	117.43	91.82 / 98.08	**102.08**	87.10 / 91.60	88.60
70 °C, filter clogged twice	6.77 CFM	99.29	117.94	92.24 / 98.48	**102.39**	87.00 / 91.50	88.50
70 °C clean, HS4 fitted (Rev08 final re-audit)	7.47 CFM	99.21	117.71	91.87 / 98.13	**93.38**	86.87 / 91.37	88.42
70 °C, filter clogged twice, HS4 fitted	6.72 CFM	99.35	118.11	92.36 / 98.60	**94.24**	87.01 / 91.51	88.30
Section 7, 70 °C clean, for comparison	7.52 CFM	99.20	114.55	92.60 / 98.77	**101.81**	n/a	n/a



Rev08 adapter board at 70 °C and its change against Rev06/07

Rated ambient (interpolated between the 55 and 70 °C runs):

Limit	Governing part	Rated ambient (new)	Previous (0.73 W FPGA)
Stock KV260, commercial K26 (Tj ≤ 85 °C)	`K26`	**56.1 °C**	56.1 °C
TA-rated adapter parts on their board temperature (Tb ≤ 85 °C)	`U401` ADCLK948 (`Tb = 76.51 -> 91.82 °C`)	**63.3 °C** (dropped `-0.8 °C`)	64.1 °C
TA-rated parts on the local cavity air (≤ 85 °C)	`U1501` (`Tair = 60.10 -> 75.10 °C`)	79.9 °C	80.1 °C
Adapter regulators	`U1001` LMR33630 (125 °C; `U1006`: `111.09 °C`)	77.7 °C	81.1 °C
Industrial K26I + Adapter (`Tj ≤ 100 °C`)	**`U1101` `XC7A50T`** (`Tj = 86.81 -> 102.08 °C`, no `HS4`; `K26I` alone **`70.9 °C`**)	**68.0 °C** (dropped `-3.1 °C`)	71.1 °C

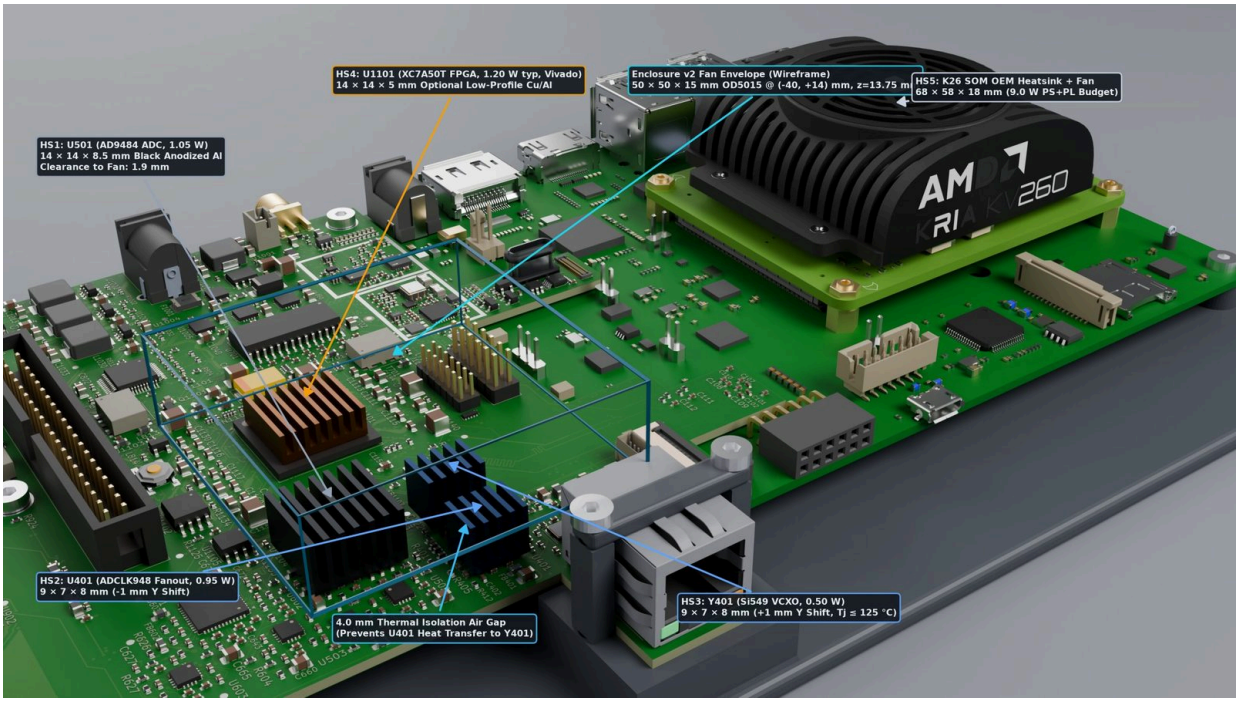
What it shows.

- **The `K26I` assembly rating drops below 70 °C.** With the real Vivado `XC7A50T` power (`1.604 W` at `70 °C` max process) plus `U1006 = 0.91 W` and `U1002 = 0.69 W`, `U1101` reaches `102.08 °C` clean (`102.39 °C` clogged) without `HS4`, dropping the `K26I`-paired ambient rating from `71.1 °C` to **`68.0 °C`** (`K26I` itself still passes at `99.08 °C`, `70.9 °C` limit). Stock commercial `KV260` stays at **`56.1 °C`**, and adapter-limited `Tb <= 85 °C` drops from `64.1 °C` to **`63.3 °C`**.
- **`HS4` on the `XC7A50T` (Rev08 final re-audit, 19 November; `run_built_v2_cfd.py` option `hs4`, cases `rev08_hs4_*`).**
- **What it is:** the 14 x 14 x 5 mm stick-on aluminium sink of the heatsink map, on the same epoxy as `U501`'s.
- **Effect at 70 °C:** it takes `U1101` from 102.08 to **93.38 °C** (clogged: 102.39 to **94.24 °C**), 6-7 °C under its 100 °C limit. Nothing else moves by more than 0.3 °C.
- **Effect on the ratings:** with it, the `K26I` assembly is limited by the `K26` itself (70.9 °C), no longer by the adapter's FPGA. The enclosure's overall rating stays **63.3 °C**, set by `U401`'s board temperature, which `HS4` does not change.
- **Decision:** at that rating `U1101` is at about 95 °C without the sink, so `HS4` is not needed to meet it.
- **Recommendation:** fit `HS4` all the same in a vehicle (5 °C more margin at 63 °C, and the only way to run past 68 °C with a `K26I`).
- **The front end warms its own corner.** The board around the RFFC5072 rises by up to 5.16 K. The RFFC5072 is at 91.60 °C junction at 70 °C, far from its limit; its board temperature reaches its 85 °C rating at 67.9 °C ambient.
- **The front edge cools.** With the board now running east of X = −10, the Ethernet PHY's and the clock's corner spreads into it: the board there falls by up to 4.97 K.
- **The LMR33630** rises from `114.55 °C` (Section 7) to `117.43 °C` at `70 °C` (`117.94 °C` clogged), `7.6 °C` under its `125 °C` limit (`U1006` sits at `111.09 °C`, `13.9 °C` under its `125 °C` limit).
- **The camera.** The board under the module sits about 17 °C above ambient. The module's own rating is the sensor's, typically 70 °C operating, so the camera, not the board, is the first to run out of margin in a hot vehicle: at 45 °C ambient it sees about 62 °C.

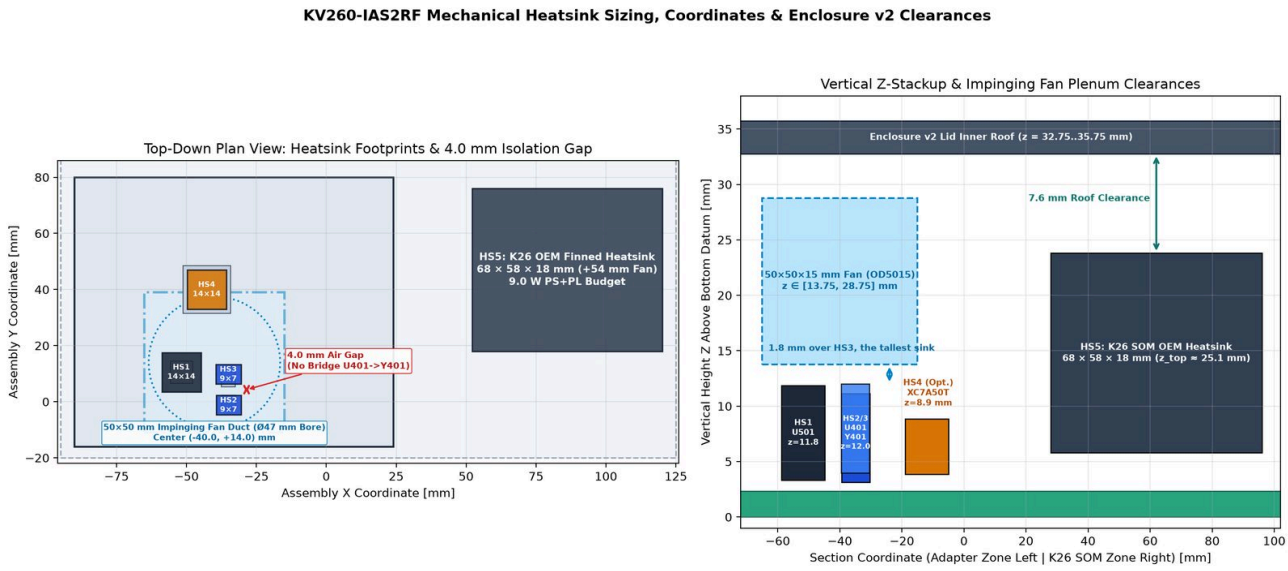
Heatsink Placement, Mechanical Dimensions & Keep-Outs (HS1–HS5)

Verified on the 3-D CAD assembly (`_work/mech/render_heatsinks.py`, `_work/mech/plot_heatsink_map.py`):

Heatsink	Target Component	Dimensions (L × W × H)	Assembly centre (X, Y, case frame)	Vertical Envelope & Clearance
HS1	U501 (AD9484 400 MSPS ADC)	**14 × 14 × 8.5 mm** (black anodized Al, 0.18 mm TIM)	(-51.8, +10.55) mm	Fin top 11.8 mm (1.9 mm below the 50 × 50 × 15 mm fan at z = 13.75 mm)
HS2	U401 (ADCLK948 LVPECL fan-out)	**9 × 7 × 8 mm** (blue anodized Al, -1.0 mm Y shift)	(-34.9, -1.20) mm	Fin top 11.2 mm (y_max = +2.3 mm)
HS3	Y401 (Si549 Programmable XO)	**9 × 7 × 8 mm** (blue anodized Al, +1.0 mm Y shift)	(-35.0, +9.80) mm	Fin top 12.0 mm, 1.8 mm under the fan (y_min = +6.3 mm -> **4.0 mm thermal gap** to HS2)
HS4	U1101 (XC7A50T Artix-7, **fit it in a vehicle**)	**14 × 14 × 5 mm** (low-profile Cu/Al)	(-42.75, +40.0) mm	Fin top ~9.0 mm (102.1 -> 93.4 °C at 70 °C)
HS5	K26 SOM (XCK26 OEM cooler)	**68 × 58 × 18 mm + 54 mm fan**	(+86.1, +47.0) mm	Fin top ~25.1 mm (7.6 mm to Enclosure v2 roof)



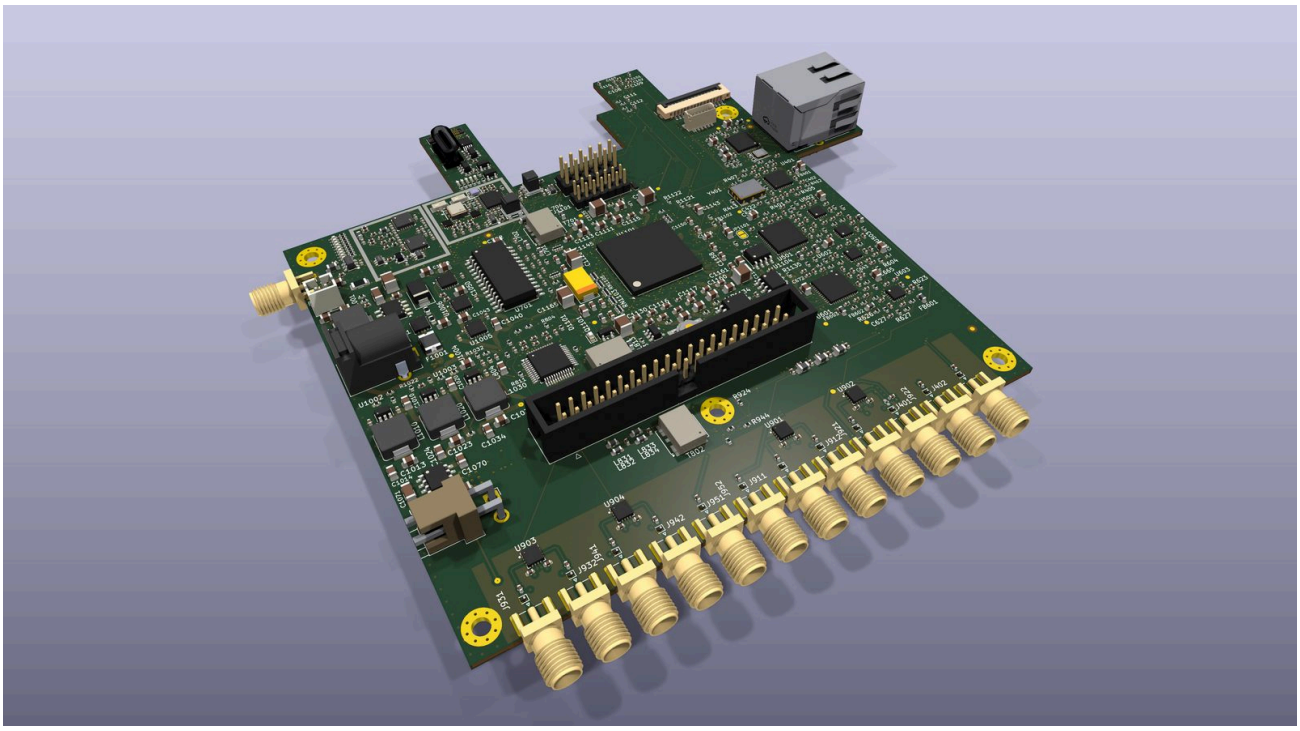
Annotated 4K heatsink placement



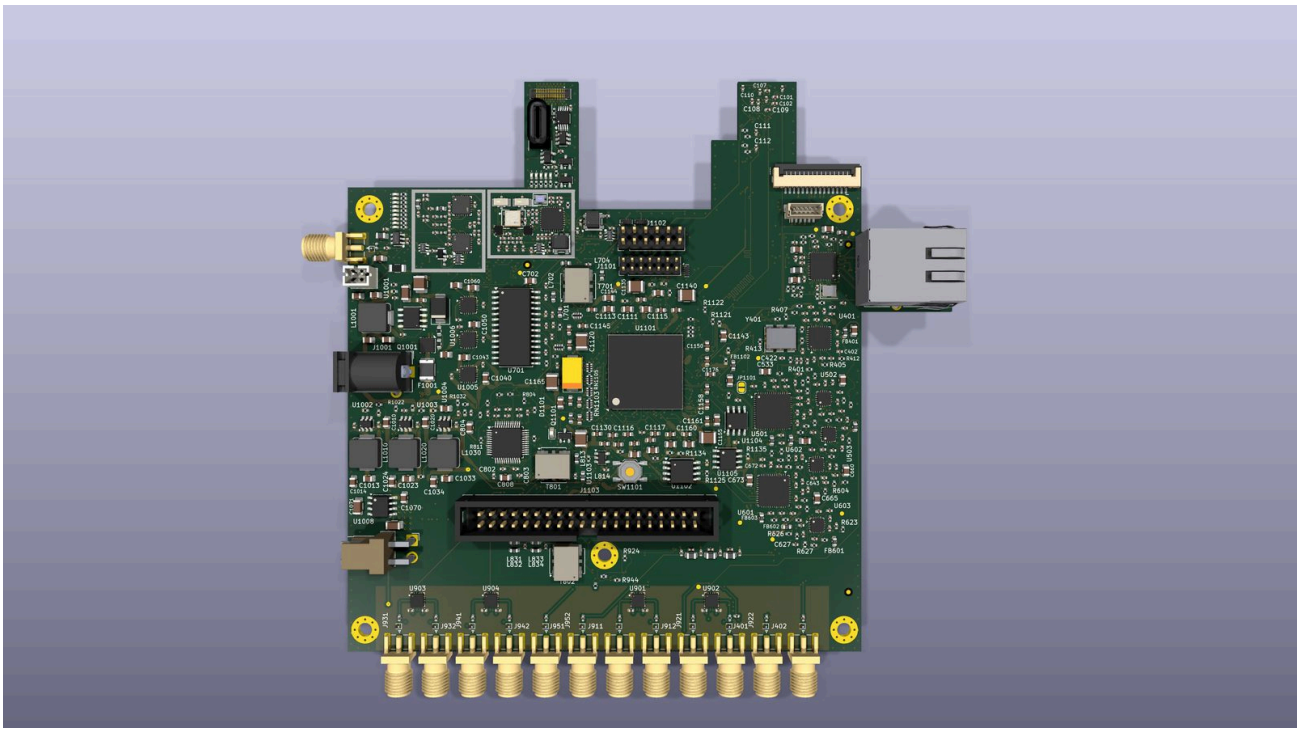
Mechanical heatsink keep-out & clearance map

Source: 4K Hardware & Enclosure Gallery

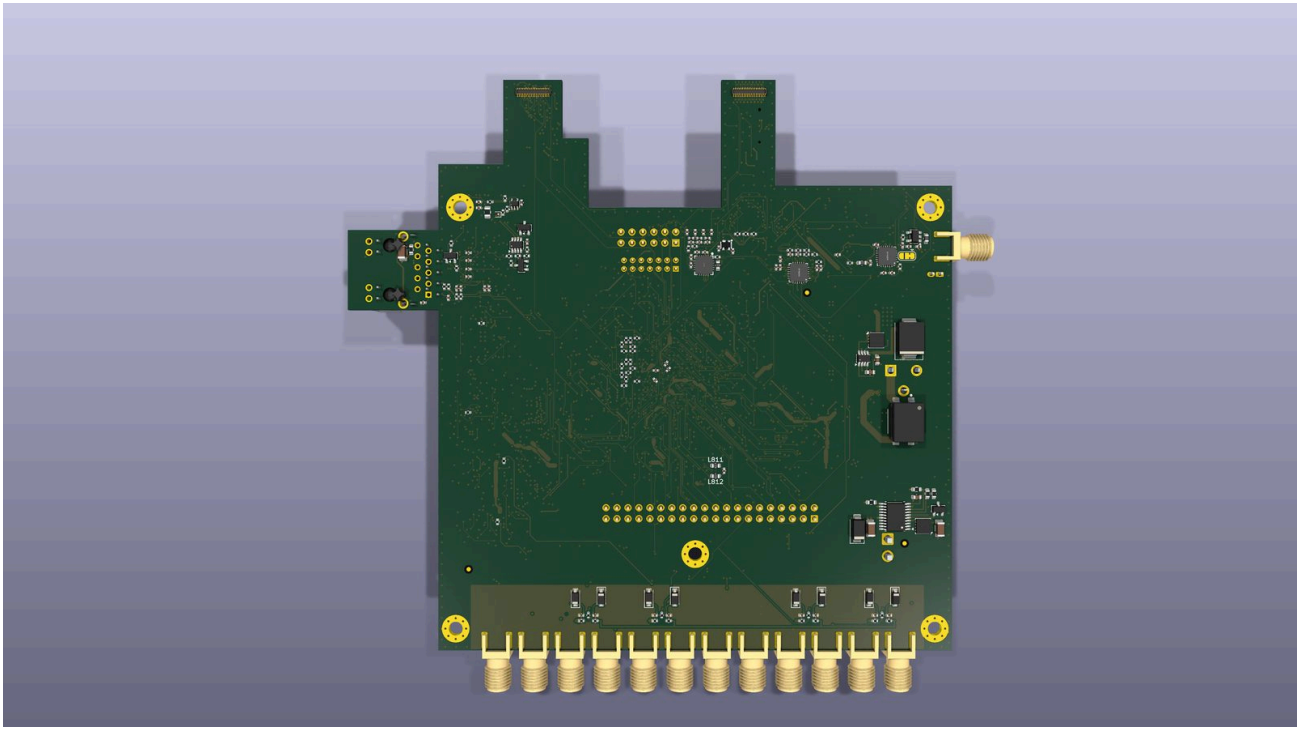
4K Hardware, Heatsink & Enclosure v2 Visual Plates



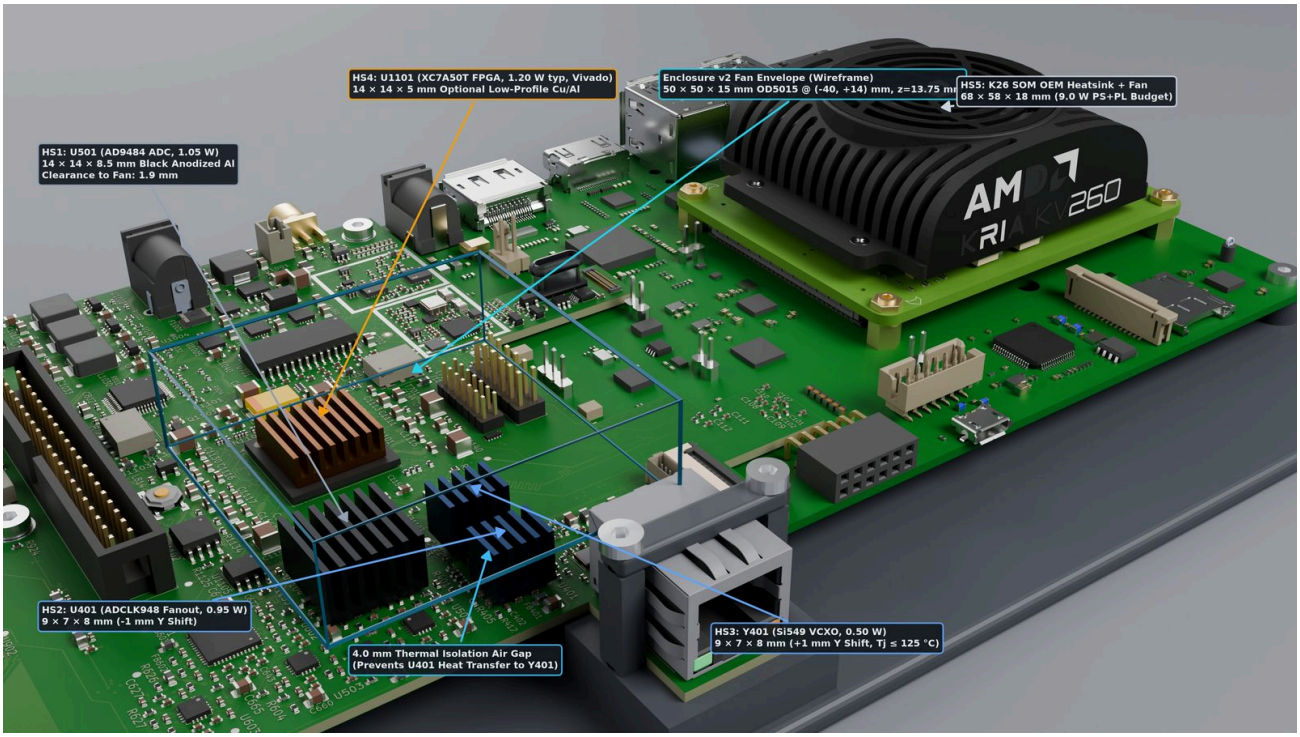
Adapter PCB: 4K Isometric Raytrace (docs/img/highres/renders/board_iso_4k.png)



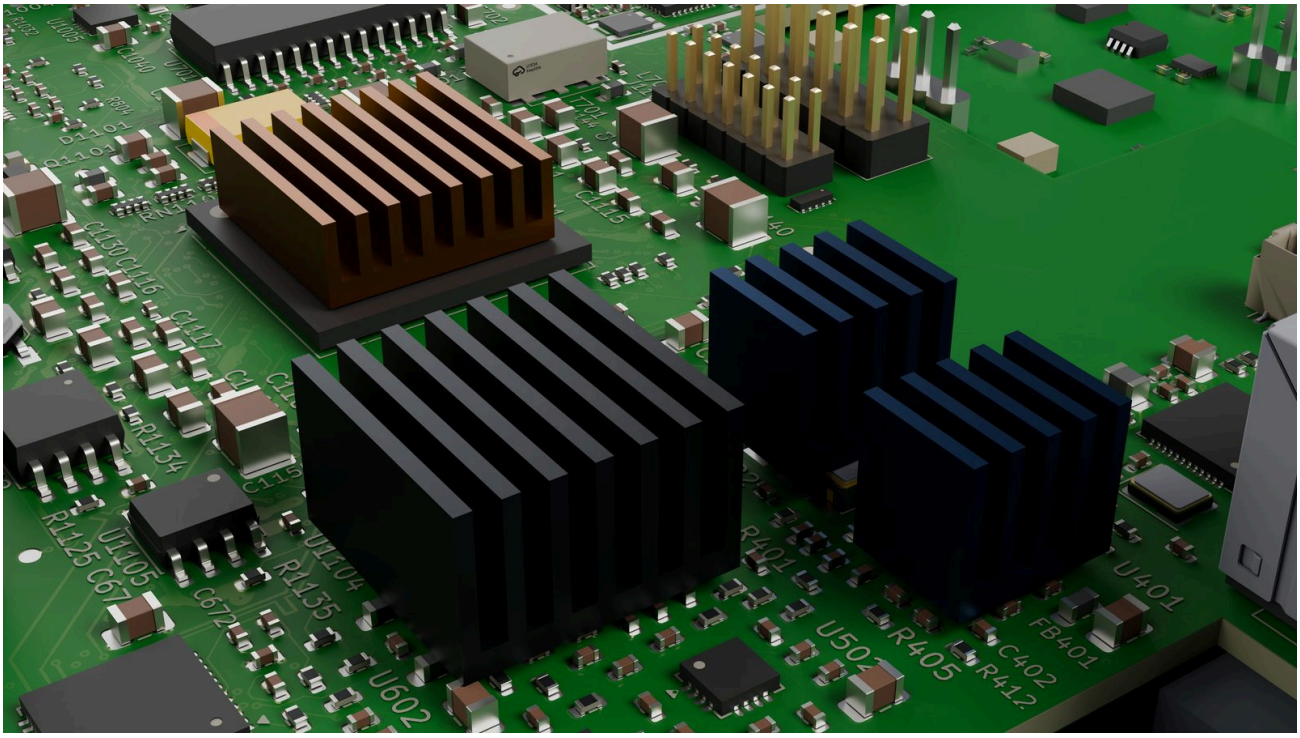
Adapter PCB: 4K Top Copper & Assembly (docs/img/highres/renders/board_top_4k.png)



Adapter PCB: 4K Bottom Copper & Assembly (docs/img/highres/renders/board_bottom_4k.png)



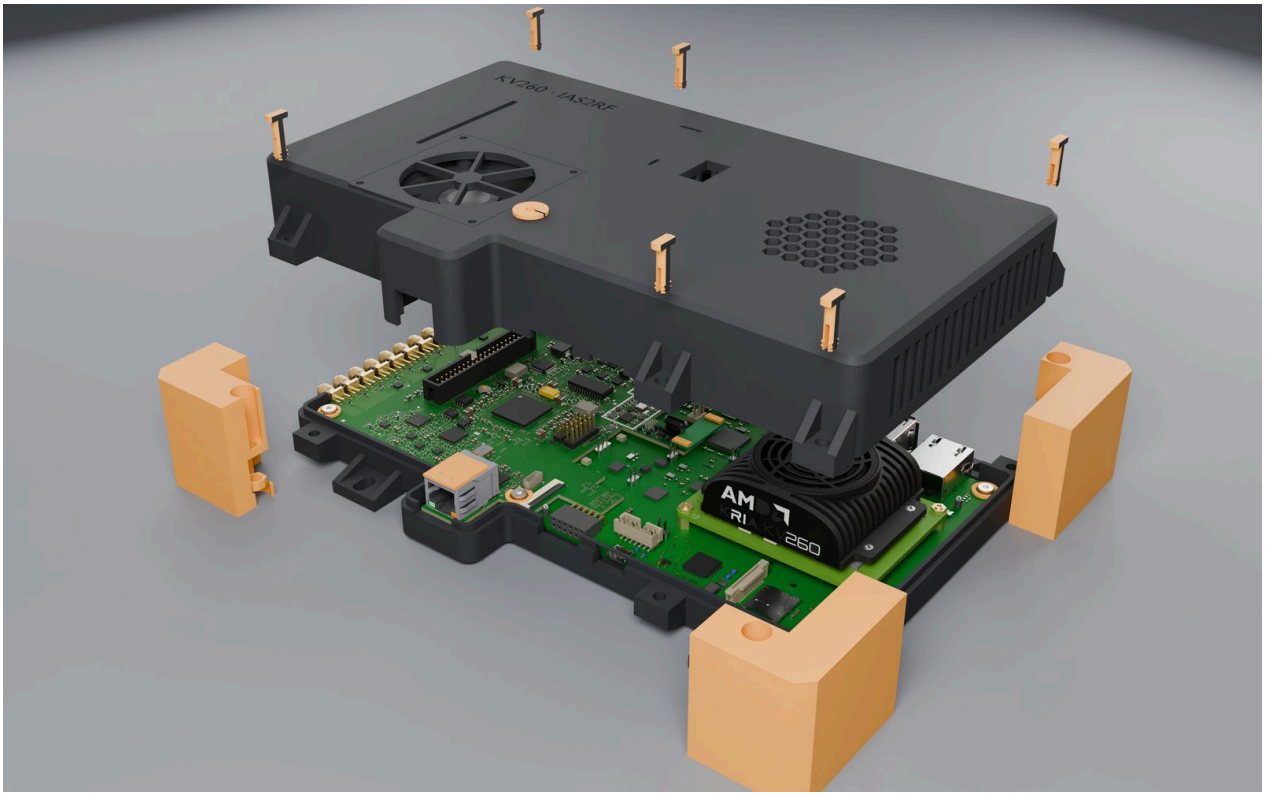
Heatsink Placement Overview (HS1–HS5 + 50 mm Fan Wireframe) (docs/img/highres/renders/board_heatsinks_4k.jpg)



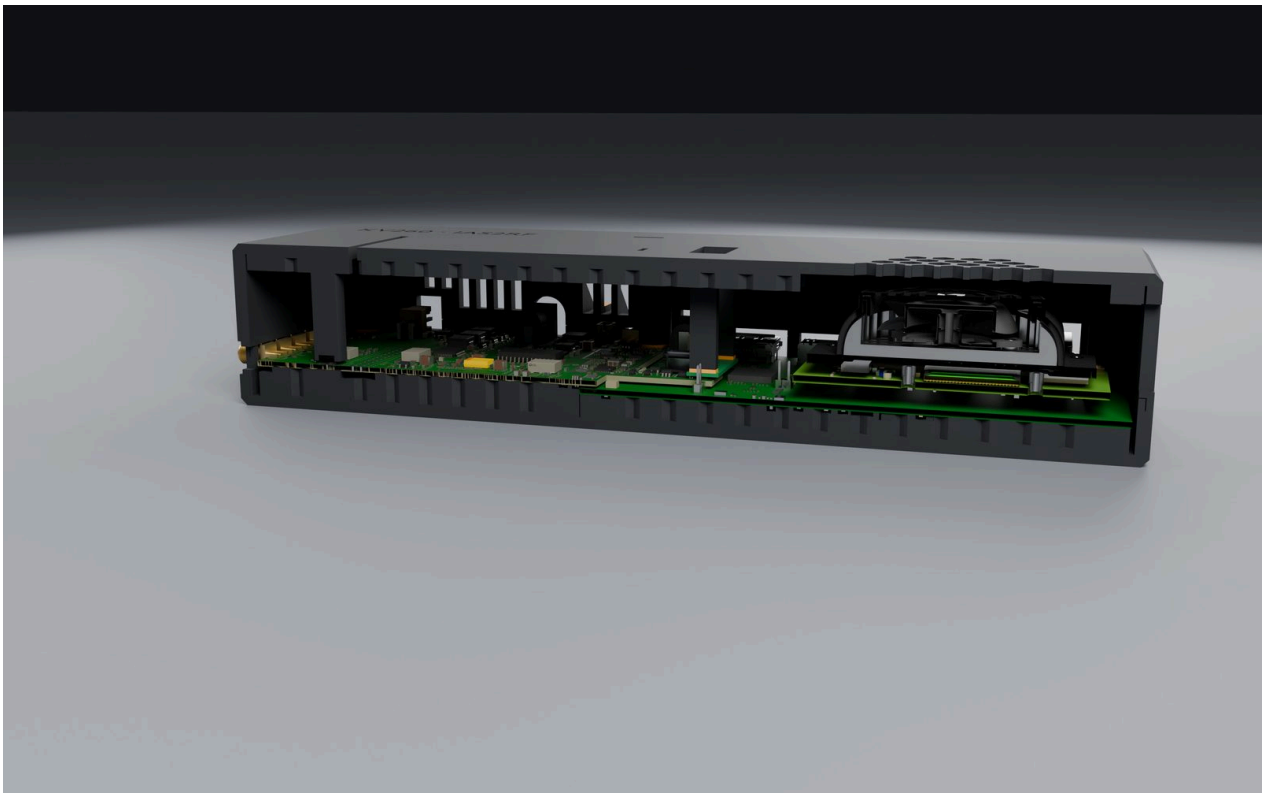
Heatsink Macro Close-Up (4.0 mm Thermal Gap U401/Y401) (docs/img/highres/renders/board_heatsinks_closeup_4k.jpg)



Enclosure v2: Closed Assembly with Filtered Intake & TPU Bumpers (docs/img/highres/renders/case_v2_closed_4k.jpg)



Enclosure v2: Open Tray with Kria K26 + RF Adapter Seated (docs/img/highres/renders/case_v2_open_4k.jpg)



Enclosure v2: Longitudinal Cross-Section (Fan Duct, SMAs & K26 Cooler) (docs/img/highres/renders/case_v2_section_4k.jpg)

Part VI: Fabrication & Costing

3 technical document(s)

Source: docs/FABRICATION.md

Fabrication: ordering the board from JLCPCB

26 September 2026 · outputs by `_work/fab/make_fab.py` · stack JLC08161H-2116C since 12 November 2026

> **8 layers since 12 Nov 2026.** Order **8 layers, stack JLC08161H-2116C**, as `fab/<date>/ORDER.txt` says; the widths for that stack are in LAYOUT §3 and `_work/field_solver8.py`. The 6-layer 2116A figures further down are the record of the earlier board.

One command writes everything JLCPCB asks for into `fab/`. That folder is git-ignored: the files are always regenerated, never edited.

```
py _work/fab/make_fab.py
```

Since 10 Nov the output is not a draft: DRC reports no errors and no unrouted connections, so the script names the folder without `DRAFT-`. The LVDS review of LAYOUT §6.2–6.3 and the calculator check above were closed on 10 Nov; the RF/high-speed review of 11 Nov (**SIGNAL_INTEGRITY.md**) was checked the same way. The script copies the project's custom rules (`KV260-IAS2RF.kicad_dru`) with the board: without them the RF lines' 0.15 mm necks at 0.5 mm-pitch pins read as clearance errors.

1. What the script does

Step	How	Why
Check the board	`kicad-cli pcb drc --refill-zones --schematic-parity` on a copy in `fab/_work/`	Any error or unrouted connection makes the output a DRAFT. The zones are filled on the copy only; the board in git stays unfilled
Gerbers	L1–L8, paste, silkscreen, mask, outline. Protel extensions, soldermask subtracted from silkscreen, zones checked	JLCPCB's KiCad guide, point by point
Drill	Excellon, mm, decimal, absolute origin, alternate mode for oval holes, plus a PDF drill map	Same guide
Zip	Gerbers + drill in one zip, spaces in the layer names replaced by `_`	The zip is what is uploaded
BOM	`Comment, Designator, Footprint, LCSC Part #, Quantity`, one line per value and footprint: 236 lines, 785 parts (19 Nov single power entry + RJ45 shield RC; 224 / 770 pre-KVPWR, 214 / 739 on 17 Nov)	JLCPCB's BOM columns
CPL	`Designator, Mid X, Mid Y, Layer, Rotation`, from KiCad's position file: 785 placements (fiducials, holes and the solder jumper JP1101 left out: they are copper only)	JLCPCB's CPL columns
ORDER.txt	The order form's values, and the DRC result	So the order is entered the same way every time

2. The order form

Field	Value	Why
Layers	**8** (6 until 12 Nov)	
Thickness	1.6 mm	
Impedance control	**Yes, JLC08161H-2116C** (8 layers; JLC06161H-2116A until 12 Nov)	The stack the widths were solved for (`_work/field_solver8.py`). Any other stack changes every impedance
Copper	1 oz outer, 0.5 oz inner	The stack's own
Via covering	**Epoxy filled & capped (POFV)**	772 vias sit in pads on the Rev08 board (765 on 17 Nov; the GPS PPS block of 18 Nov added 11; the final re-audit of 19 Nov removed four dead ones, LAYOUT §6.10) (543 on 11 Nov: 0402 passives, butted decoupling vias, every IC's exposed pad, five in L1030's output pad). JLCPCB fills and caps them free, and by default, on 6–20-layer boards. Most of the BGA's fan-out vias sit between its balls; 29 sit in ball pads (LAYOUT §6.1)
Min via	0.20 mm hole, 0.45 mm pad	Within JLCPCB's 8-layer capability
Min track / space	**0.09** / 0.10 mm	Inner LVDS pairs 0.10 / 0.15 mm, 0.09 / 0.12 mm under the FPGA (110 segments at 0.09 mm); L1 pairs 0.117 / 0.150 mm

Field	Value	Why
Surface finish	**ENIG**	Flat pads for the 1.0 mm BGA and the LFCSPs; HASL is not flat enough

3. What is left for the day of the order

The board is routed (0 errors, 0 unrouted since 10 Nov). Run the script again after any change: the folder loses its `DRAFT-` prefix only when DRC reports zero errors and zero unrouted connections.

Check the LCSC codes, and refresh them. The symbols carry no part numbers, so the codes live in `_work/fab/lcsc_parts.csv`, one per BOM line, and `make_fab.py` copies them into the BOM. They were chosen on 2 October 2026 by `_work/fab/lcsc_select.py` from JLCPCB's own parts search, by rule:

- the value, the package and, for a chip, the exact model must match;
- capacitors: C0G below 1 nF, X7R or X5R above, never Y5V; the voltage rating at least what the line's highest rail needs (16 V on the 0402 decoupling that touches 5 V, 25 V on the 12 V input);
- resistors 1 %;
- among the parts that qualify: JLCPCB "basic" first (no loading fee), then stock.

Stock changes daily: run `py _work/fab/lcsc_select.py` again before ordering and read the diff of the CSV, then `python _work/fab/quote.py` for today's prices (**JLCPCB_QUOTE.md**). On 10 Nov two lines were re-selected because their part ran out: the 22.6 kΩ (now C100316) and the PROG switch (now TL3342F450QG). **Re-run on 17 November for Rev08: 212 of 214 lines have a code** (187 distinct); after the RF and power audit (18 November), **222 of 224**; and after the single power entry (`KVPWR`, `R1043 = 6.04k`) and RJ45 shield RC (`C1223`, `R1218`) (19 November), **234 of 236 lines (`209` distinct codes)**. Note that `TPS26631PWPR` (`C2866319`) showed `0` LCSC stock on 19 November and requires global sourcing or consignment alongside the other zero-stock ICs below. Its drop-in alternative is the same part on a 250-piece reel, `TPS26631PWPT` (`C2832195`), also at `0` that day. With the PSU board (**PSU_SPEC**) feeding the KV260, the whole KV260 branch (`U1010`, `Q1010`, `Q1011`, `R1040-R1043`, `C1093-C1095`, `D1004`, `J1004`) can be left unfitted instead. The rules gained the front end's parts by name (the Murata LQW15/LQW18 wirewounds the filter Monte Carlo assumed, Q 40–45, ±2 %), any small capacitor as C0G, and the LEDs by colour; green is AlGaInP (≥ 560 nm, about 2 V), because the rail and status LEDs run from 3.3 V through a resistor. The `74LVC1G07` rule now takes only TI's part, not a second source of the same name. Four are not the drawn value, because that value is not made (the CSV's Note column says so):

Line	Drawn	Fitted	Effect
C710, C814, C834	106 pF (AERIS C141)	110 pF C0G	+3.8 % on one element of the DAC reconstruction filter. Or 100 pF plus 5.6 pF by hand
L701–L704, L811–L834	107.3 nH (AERIS L22)	110 nH ±2 %, Murata LQW18	+2.5 %, same filter
C1110	T520V337M2R5ATE025 (UG483)	T520V337M006ATE025	Same series and case, 6.3 V instead of 2.5 V
L1423	100 nH ±2 %	LQW15ANR10J, ±5 %	The 2 % part is not stocked; the same tolerance the Monte Carlo gave the 390 nH

Not stocked, or not catalogue parts: the Si549 (Y401) has no code, because Skyworks builds its ordering code per configuration: order it from Skyworks or a distributor and consign it. The TC1-1-13M+ (T1301) is Mini-Circuits' only: LCSC's part of that name is a clone with another pin-out, so it is consigned too. On 17 November nine lines were short for two boards (JLCPCB_QUOTE §1), the SMA among them (5 in stock for 26). Several codes exist but showed **zero stock** on 2 October: ADCLK948, AD9484, AD9708, M3SWA2-34DR+. Others are very short (XC7A50T 73, AD8352 9, AD9253 2, ADT2-1T+ 7). JLCPCB's "global sourcing" or consignment covers them.

Check every rotation in JLCPCB's placement preview. KiCad's zero orientation and JLCPCB's differ for some packages (SOT-23, some QFNs and SOICs). The CPL is KiCad's; correct the rotation there if a part shows turned.

Confirm the impedances in JLCPCB's own calculator (`jlcpcb.com/pcb-impedance-calculator`): 8 layers, 1.6 mm, outer copper 1 oz, inner 0.5 oz, stack **JLC08161H-2116C** (L1 · L2 GND · L3 · L4 PWR · L5 GND · L6 · L7 GND · L8). The field solver (`_work/field_solver8.py`, SIGNAL_INTEGRITY §8) gives:

Row	Type	Layer	References	Width / spacing	Field solver	Used on the board by
1	Single-ended	L1 / L8	L2 / L7	183 µm	50.4 Ω	`IF_RX_*`, `IF_TX_*` (RF50), the SMA launches
2	Single-ended	L3 / L6	L2+L4 / L5+L7	151 µm	50 Ω	Single 50 Ω inner lines
3	Differential	L3 / L6	as row 2	100 / 150 µm	100.2 Ω	The coupled LVDS pairs
4	Differential	L3 / L6	as row 2	90 / 120 µm	98.5 Ω	The same pairs under the FPGA

Row	Type	Layer	References	Width / spacing	Field solver	Used on the board by
5	Differential	L1	L2	117 / 150 µm	100.4 Ω	The L1 pairs

The 6-layer check of 10 November (stack JLC06161H-2116A, every width within 1–6 % of JLCPCB's calculator) is superseded; **enter these five rows in the calculator for the 8-layer stack before paying**, and order stack 2116C explicitly: a cheaper stack with thinner outer prepreg would move the RF lines off 50 Ω.

4. How it was checked

Check	Result
Script run on the placed board	17 files in the zip (8 copper layers, 2 mask, 2 paste, 2 silkscreen, outline, drill, job file), BOM 236 lines / 785 parts, CPL 785 placements, DRC 0 violations, 0 unconnected pads, 0 footprint errors (19 November, single power entry and RJ45 shield RC on the Rev08 board; 224 / 770 pre-KVPWR, 214 / 739 on 17 Nov)
CPL against BOM	The same 785 references in both (19 Nov)
Settings against JLCPCB's KiCad guide	Protel extensions, subtract soldermask, zone check; Excellon mm, decimal, absolute, alternate oval mode, all as the guide lists

Source: docs/JLCPCB_QUOTE.md

JLCPCB order: quote

10 November 2026, bare boards re-quoted on 8 layers on 12 November, parts, assembly and bare boards for the Ethernet option (140 × 132 mm) on 13 November, parts and assembly for Rev08 on 17 November, re-priced on 18 November and on 19 November for the single power entry · board KV260-IAS2RF · not ordered yet

What ordering the board from JLCPCB, made and assembled, would cost today. This is a budget, not an order: nothing was uploaded and no cart was created. How to enter the order is in **FABRICATION.md**; the files come from `python _work/fab/make_fab.py`.

Prices are in US dollars, before VAT. Stock and prices change daily: run `python _work/fab/quote.py` again before ordering. It refreshes `_work/fab/quote.csv` and the parts table in §4.

1. Summary

	2 assembled boards	5 assembled boards	Source
Bare boards, 8 layers, 140 × 132 mm (5 made either way)	287.96	287.96	JLCPCB's quote page, §2 (13 Nov; same outline and stack since)
Assembly fees	445.49	482.44	JLCPCB's price page, §3 (17 Nov counts + 12 audit + 10 single-entry + 2 RJ45 shield RC feeders, +2 hand joints, +53 SMT joints, +2 X-ray parts)
Parts (209 LCSC codes, 19 Nov, single power entry + RJ45 shield RC)	1,638.38	3,878.89	JLCPCB's parts search, §4
Si549 oscillator and TC1-1-13M+ balun, bought apart and consigned	~45 `[E]`	~110 `[E]`	No usable LCSC code, §5
Shipping, UPS Express Saver, duties paid (DDP)	26.08	26.08	Quote page, for the bare boards' 0.50 kg; more for assembled ones
Total	**≈ 2,443**	**≈ 4,785**	
Per board	≈ 1,221	≈ 957	

Rev08 (17 November), re-priced with `lcsc_select.py` on live stock and `quote.py`: 214 BOM lines, 739 parts, 212 lines with a code and 187 distinct codes (+72 since Rev06): the VHF/UHF front end, the 14 LEDs, the USB bridge and the IAS0 receptacle. Parts rise by about $64 a board, most of it the RFFC5072 ($14.64), the two PE42442 and two SKY13418 switches, the SPF5043Z amplifiers, the PE4312 and the thirteenth SMA. **Feeder loading is now the largest assembly fee, $286** (187 × $1.53), against $174 for Rev06: the front end's filters use many distinct C0G and wirewound values. The rows below are the history of this quote.

18 November, before the tag: 219 lines, 751 parts, 217 lines with a code, 192 distinct codes. New: the HRO TYPE-C-31-E-17 in place of the HX vertical USB-C (LAYOUT 6.8), the GPS PPS block (the XUNPU 15-way FPC receptacle, the JST-SH header, an SN74LVC1G17, a 0.2 A PTC and seven passives). Five new codes add $7.65 of feeder loading. The parts total is lower than on 17 November, by $52 for two boards, because the XC7A50T-2FTG256I's price fell overnight ($56.54 less for the two boards' units); the new parts themselves cost about $1.50 a board. The 15-way FFC to the KV260 is not assembled: it is on the shopping list.

19 November (single power entry `KVPWR` + RJ45 shield RC): 236 lines, 785 parts, 234 lines with a code, 209 distinct codes. Fifteen parts are added: thirteen on `KVPWR` (three reuse existing codes: `DMT10H015LFG-7` `C5245407` extended qty +1, `2N7002` `C8545` basic qty +1, `10u 25V 1206` `C13585` basic qty +1; ten add new codes: `ZEGMCM9070-501T` `C53154905` extended `$0.54` stock `1,400`, `TPS26631PWPR` `C2866319` extended `$5.52` **stock `0`** global sourcing/consignment, `SS34` `C8678` basic `$0.035`, `B2PS-VH` `C158007` extended `$0.152`, `316k` 0603 `C25814` extended, `24.9k` 0603 `C137761` extended, `30.9k` 0603 `C2930090` extended, `6.04k` 0603 `C25977` extended stock `85,053` `$0.0017` setting the `3.0 A` limit, `22n` 0603 `C21122` basic, `1u 100V` 1206 X7R `C13832` extended -> **4 basic / 9 extended** across the 13 `KVPWR` parts, 2 new basic / 8 new extended) plus two on `J1201`'s shield RC (`C1223` `1n 2kV` 1206 X7R `C23631` extended stock `1,130,950` `$0.0179`, and `R1218` `1M` 0603 1% `C22935` basic stock `5,150,785` `$0.0018`). Live quote rises over the 18 Nov audit total by **+$29.45** on parts (`$1,608.93 -> $1,638.38`; `+$53.68` for 5 boards) and **+$21.88** on assembly (12 new feeders `+$18.36`, `J1004` +2 hand joints `+$0.07`, ~53 SMT joints `+$0.17`, `U1010`/`Q1010` +2 X-ray `+$3.28`), shifting two boards by **+$51** (`≈ $2,392 -> ≈ $2,443`) and five boards by **+$77** (`≈ $4,708 -> ≈ $4,785`). The off-board `J1004`-to-`J12` jumper (`VHR-2N` + `2 × SVH-21T-P1.1`, 18 AWG, `5.5 × 2.5 mm` plug) and `5 A` fuse are on the **shopping list**.

18 November, after the RF and power audit (AUDIT_Rev08.md): 224 lines, 770 parts, 222 lines with a code, 199 distinct codes. New or changed: the TCAN3403DDFRQ1 (C35926232) for the TCAN330, the TPS563201DDCR (C116592) for one TPS562201, the LP5907MFX-2.8 (C186700) for the -3.0, the mSMD200-24V PTC (C143954) for the 1.5 A one, the LQW15AN24NG00D (C167472) of the new 300 MHz high-pass (its six other parts reuse codes already on the board), 3.24 k and 330 ohm values. Parts rise by $8.56 for two boards, assembly by about $11 of feeder loading (7 new codes).

On 6 layers the bare boards were $236.88, so the move to 8 layers adds **$46.04 to the order**, 2 % of the total for two boards. The parts list grew by two 0402 resistors (R105, R106), a few cents.

The Ethernet option (13 November, CONTROL_SPEC §7) adds about $46 to two boards: $25 of parts (the PHY and the RJ45 are most of it) and $21 of assembly, mostly the 12 new feeders. Its four DNP capacitors are not in the BOM. **The bare boards, re-quoted for the tab's 140 × 132 mm bounding box, cost $5.04 more** ($287.96 against $282.92): the board line $15.30 against $11.90, the rest a few cents up since 12 Nov (§2).

Rev06 (14 November, branch `rev06`), re-priced the same way: parts $1,523.80 for two boards and $3,644.36 for five (115 LCSC codes; +$20 and +$41), feeder loading 114 × $1.53 = $174.42 (+$12). The difference is the Rev05 input protection, now with codes (LM74502-Q1, two DMT10H015LFG, SMCJ33CA, SMBJ18CA), the fan header with its PTC, and the SGMII bias network; C1218–C1221 are now fitted. Two boards come to **≈ $2,156**, five to **≈ $4,361**.

Rev07 (15 November): the HF input's anti-alias low-pass (SIGNAL_INTEGRITY §9.9) adds ten parts and nine LCSC codes, all extended and in stock (`_work/fab/lcsc_parts.csv`): six C0G 0402 capacitors and three 0805 wirewound inductors (LQW2BASR22J00L, SDWL2012CR27GSTF, LQW2BASR33G00L, the scarcest at 949 in stock). Estimated, not re-quoted: 9 × $1.53 of feeder loading and about $1 of parts per board, so **≈ $2,172** for two boards and **≈ $4,385** for five. Run `quote.py` before ordering. The same eight parts are short (plus TPD4E05U06DQAR, 71 in stock for 80): see below.

Parts are two thirds of the cost, and eight lines are 80 % of the parts (about $659 of $826 per board, 17 Nov):

Part	Each	×/board	Per board
M3SWA2-34DR+ (RF switch)	45.76	4	183.03
AD9253BCPZ-125 (ADC)	97.38	1	97.38
AD9484BCPZ-500 (ADC)	97.29	1	97.29
XC7A50T-2FTG256I (FPGA)	93.47	1	93.47
AD8352ACPZ (ADC driver)	20.87	4	83.47
SMA edge connectors	4.77	13	62.03
ADT2-1T+ (balun)	7.23	3	21.70
ADCLK948BCPZ (clock)	20.79	1	20.79

Prices from LCSC, at the tier for two boards' quantity.

Nine parts are short of stock for even two boards (17 November): ADCLK948, AD9484, AD9253, AD9708 and M3SWA2-34DR+ have none, AD8352 has 7 of 8, ADT2-1T+ 1 of 6, TMP1075DR 1 of 2, and **the SMA, SMA-J-P-H-ST-EM1, 5 of 26** (905 on 2 October). The Rev08 parts are all in stock for five boards; the scarcest are the RFFC5072 (61), the TA1090EC SAW filter (149) and the PE42442 (245). JLCPCB's "global sourcing" buys them in and its price can differ from LCSC's list price above. The other choice is to buy them from a distributor and consign them. The ADI parts and the Mini-Circuits switches are sold at Digi-Key and Mouser, often for less than the LCSC list price.

2. Bare boards: $287.96 for 5

Entered on jlcpcb.com/quote on 12 Nov 2026 with the values of FABRICATION §2 (8 layers); the 6-layer column is the same page on 10 Nov. Nothing was uploaded: the page prices from the dimensions.

Field	Value	6 layers (2116A)	8 layers (2116C)	8 layers, 140 × 132 (13 Nov)
Layers, size, quantity	119 × 120 mm, 5 (140 × 132 on 13 Nov)	Board **9.30**	Board **11.90**	Board **15.30**
Thickness, finish	1.6 mm (2116C is 1.52 mm actual), ENIG 1 µ"	Surface finish **18.20**	**18.20**	**18.70**
Material	FR4 TG155	**3.66**	0.00	0.00
Copper	1 oz outer, 0.5 oz inner	n/a	n/a	n/a
Stack	JLC06161H-2116A / **JLC08161H-2116C**	Stack-up fee **102.79**	**83.89**	**84.24**

Field	Value	6 layers (2116A)	8 layers (2116C)	8 layers, 140 × 132 (13 Nov)
Impedance control	±10 %	**33.08**	**33.08**	**33.08**
Via covering	Epoxy filled & capped (POFV)	0.00	0.00	0.00
Min via	0.2 mm hole (the board's 0.20 / 0.45 mm vias)	**18.31**	**18.31**	**18.83**
4-wire Kelvin test	Forced on by the 0.2 mm vias	**17.49**	**17.49**	**17.76**
Confirm production file	Forced on by the specified stack	**1.05**	**1.05**	**1.05**
Engineering fee		**33.00**	**99.00**	**99.00**
Build time	7–8 days	0.00	0.00	0.00
Total		**236.88**	**282.92** (desktop app: 277.92)	**287.96** (desktop app: 282.96)

The difference is the engineering fee ($99 on 8 layers against $33) and the board itself; the 2116C stack-up fee is lower than 2116A's. The page warns that 2116C is 1.5216 mm thick, not 1.6 mm (within the ±10 % tolerance); the board has nothing that depends on its thickness.

The specified stack costs $83.89 on its own ($102.79 for 2116A on 6 layers), and it rules out JLCPCB's Economic assembly. The page says the stack "doesn't support economic PCB assembly". Both are the price of the impedances: POWER_AND_STACKUP §2.6 explains why the board uses this stack and not the default 3313.

The 0.2 mm vias cost $35.80 (via size and Kelvin test). The fan-out of the 1.0 mm BGA needs them.

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3. Assembly fees: Standard PCBA

The 2116C stack, like 2116A, allows only **Standard** PCBA. Its fees, from JLCPCB's price page (last updated 22 Oct 2026). The assembly quote itself needs the Gerbers uploaded, so it was not run:

Fee	Rate	2 boards	5 boards
Setup, **both sides**	51.12	51.12	51.12
Stencil, both sides	16.42	16.42	16.42
SMT joints (2,685 per board, the SMD pads of the 739 fitted parts)	0.0016 / joint	8.59	21.48
Hand-soldered joints (87 per board: J1001, J1002, J1101, J1102, J1103, J1201)	0.0164 / joint	2.85	7.13
Hand-soldering labour	3.58 / order	3.58	3.58
Feeder loading: every part on Standard, basic or extended	1.53 × 187 parts	286.11	286.11
X-ray, 22 parts per board with hidden joints (FPGA, QFNs, LFCSPs; Rev08 adds the two PE42442, two SKY13418, the PE4312, the RFFC5072 and the two TCA6416A)	0.82 / 0.49 per part	36.08	53.90
Packing	0.50 + area	0.50	0.50
Total		**405.25**	**440.24**

Counted on 17 November from the board file and the BOM (19 Nov single power entry + RJ45 shield RC add 12 feeders `+ $18.36`, 2 hand joints on `J1004`, ~53 SMT joints and 2 X-ray parts `U1010`/`Q1010`, reflected in §1; Rev06: 1,930 joints, 85 by hand, 106 feeders, 14 X-ray parts; $265.73 and $290.51).

The setup and stencil are double-sided because of two parts: J101 and J102, the KV260 connectors, sit on the bottom face. Their 0.4 mm pitch rules out hand-fitting them.

The **feeder loading** ($162) is the largest assembly fee. On Standard PCBA every part is loaded, basic or not; fewer distinct values would lower it.

Not counted: a possible fixture fee for the hand-soldered parts ($16.42 for 1–29 boards, if JLCPCB applies it), and the Si549's consignment handling.

The FAQ page gives other figures (setup $8, stencil $1.50, $3 per extended part). The price page is newer and has the Standard column. The live quote, once the files are uploaded, is the final word.

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4. Parts, line by line

Each line is one LCSC code. **Buy** is what JLCPCB would purchase: the boards' need plus its attrition, at least its minimum. Links go to JLCPCB's part page (code) and LCSC's (part). Stock in **bold** is short of the two-board need.

<!-- parts:begin --> *Searched 2026-11-19 by `_work/fab/quote.py`; prices in USD, JLCPCB's tier for the quantity bought.*

LCSC	Part	Maker	Value	Lib	Per board	Stock	Buy 2 / unit / cost	Buy 5 / unit / cost
C33062043	M3SWA2-34DR+	Mini-Circuits	M3SWA2-34DR+	extended	4	**0**	8 / 45.73 / 365.81	20 / 44.25 / 884.95
C514282	AD9253BCPZ-125	Analog Devices	AD9253BCPZ-125	extended	1	**0**	2 / 97.31 / 194.62	5 / 97.31 / 486.54
C653480	AD9484BCPZ-500	Analog Devices	AD9484BCPZ-500	extended	1	**0**	2 / 97.22 / 194.43	5 / 97.22 / 486.09
C578707	AD8352ACPZ-R7	Analog Devices	AD8352ACPZ	extended	4	**4**	8 / 20.85 / 166.82	20 / 19.97 / 399.42
C2976033	XC7A50T-2FTG256I	AMD/XILINX	XC7A50T-2FTG256I	extended	1	27	2 / 65.17 / 130.33	5 / 65.17 / 325.83
C5199907	SMA-J-P-H-ST-EM1	Samtec	CLK_REF_IN / CLK_OUT / SDR_RX_A / AERIS_IF_A / AERIS_IF / SDR_RX_WB / SDR_TX_A / AERIS_TX_A / AERIS_TX / SDR_TX_WB / SDR_RX_C / SDR_TX_C / VU_ANT	extended	13	**16**	26 / 4.769 / 123.98	65 / 4.366 / 283.78
C5223988	ADT2-1T+	Mini-Circuits	ADT2-1T+	extended	3	**1**	6 / 7.227 / 43.36	15 / 6.263 / 93.95
C578960	ADCLK948BCPZ	Analog Devices	ADCLK948BCPZ	extended	1	**0**	2 / 20.77 / 41.54	5 / 20.77 / 103.86
C653734	AD9708ARZ	Analog Devices	AD9708AR	extended	1	**0**	2 / 16.84 / 33.68	5 / 16.84 / 84.20
C3034742	RFFC5072TR13	Qorvo	RFFC5072	extended	1	36	2 / 14.63 / 29.25	5 / 14.63 / 73.13
C653820	AD9767ASTZRL	Analog Devices	AD9767ASTZ	extended	1	169	2 / 14.55 / 29.10	5 / 14.55 / 72.76
C41359590	MT25QL128ABA1ESE-0SIT	Micron Tech	MT25QL128ABA1ESE	extended	1	74	2 / 12.96 / 25.93	5 / 12.96 / 64.82
C470913	PE42442A-Z	pSemi	PE42442	extended	2	245	4 / 4.957 / 19.83	10 / 4.264 / 42.64
C5245407	DMT10H015LFG-7	Diodes Incorporated	DMT10H015LFG	extended	3	65	6 / 3.208 / 19.25	15 / 2.798 / 41.97
C544500	TPS7A8300RGRR	Texas Instruments	TPS7A8300RGR	extended	3	71	6 / 3.207 / 19.24	15 / 2.768 / 41.52
C470902	SPF5043Z	Qorvo	SPF5043Z	extended	2	5902	4 / 3.393 / 13.57	10 / 2.899 / 28.99
C2866319	TPS26631PWPR	Texas Instruments	TPS26631PWPR	extended	1	**0**	2 / 5.518 / 11.04	5 / 5.518 / 27.59
C2886897	TL3342F450QG	E-Switch	PROG	extended	1	27	13 / 0.7482 / 9.73	13 / 0.7482 / 9.73
C5219206	LM74502QDDFRQ1	Texas Instruments	LM74502-Q1	extended	1	**0**	6 / 1.619 / 9.71	6 / 1.619 / 9.71
C470892	PE4259-63	pSemi	PE4259	extended	4	13691	8 / 1.187 / 9.50	20 / 1.064 / 21.28
C2878381	TMP1075DR	Texas Instruments	TMP1075DR	extended	1	**1**	23 / 0.3962 / 9.11	23 / 0.3962 / 9.11
C4990147	HFCN-1000+	Mini-Circuits	HFCN-1000+	extended	1	302	2 / 3.078 / 6.16	5 / 3.078 / 15.39
C45783	CL21A226MAQNNNE	Samsung Electro-Mechanics	22u 10V	basic	13	3626525	30 / 0.1975 / 5.93	69 / 0.1975 / 13.63
C2904132	RTL8211FSI-CG	Realtek Semicon	RTL8211FSI-CG	extended	1	4359	2 / 2.87 / 5.74	5 / 2.87 / 14.35
C50933	HR911130C	HANRUN(Zhongshan HanRun Elec)	HR911130C	extended	1	6171	2 / 2.86 / 5.72	5 / 2.86 / 14.30
C500480	PE4312C-Z	pSemi	PE4312	extended	1	1497	2 / 2.839 / 5.68	5 / 2.839 / 14.19
C5476329	150040VS73240	Wurth Elektronik	CFG green / LINK green / LO green / +12V green / +5V0 green / +3V3_D green / +1V8_D green / +1V0 green	extended	8	379	16 / 0.316 / 5.06	40 / 0.28 / 11.20
C544380	LM2663M/NOPB	Texas Instruments	LM2663M	extended	1	5795	2 / 2.392 / 4.78	5 / 2.392 / 11.96
C20415295	TA1090EC	TST	TA1090EC	extended	1	149	2 / 2.166 / 4.33	5 / 2.166 / 10.83
C879868	LFCN-1000+	Mini-Circuits	LFCN-1000+	extended	1	456	2 / 2.071 / 4.14	5 / 2.071 / 10.35
C150871	SKY13418-485LF	Skyworks Solutions	SKY13418-485LF	extended	2	4200	4 / 1.025 / 4.10	10 / 0.8398 / 8.40
C2041815	SRP7028A-8R2M	BOURNS	SRP7028A-8R2M	extended	1	201	2 / 1.822 / 3.64	5 / 1.822 / 9.11
C879855	TC4-1W+	Mini-Circuits	TC4-1W+	extended	1	2142	2 / 1.706 / 3.41	5 / 1.706 / 8.53
C182336	TCA6416ARTWR	Texas Instruments	TCA6416ARTWR	extended	2	32351	4 / 0.8202 / 3.28	10 / 0.6728 / 6.73
C45961	PESD5V0F1BL,315	Nexperia	PESD5V0F1BL	extended	14	127276	36 / 0.0842 / 3.03	78 / 0.0662 / 5.16
C7424785	TYPE-C-31-E-17	Korean Hroparts Elec	TYPE-C-31-E-17	extended	1	1032	2 / 1.427 / 2.85	5 / 1.427 / 7.14

LCSC	Part	Maker	Value	Lib	Per board	Stock	Buy 2 / unit / cost	Buy 5 / unit / cost
C492354	878321420	MOLEX	JTAG 2x7 2mm	extended	1	2901	2 / 1.401 / 2.80	5 / 1.401 / 7.01
C35926232	TCAN3403DDFRQ1	Texas Instruments	TCAN3403DDFRQ1	extended	1	858	2 / 1.324 / 2.65	5 / 1.324 / 6.62
C77101	GRM32ER61C476KE15L	Murata Electronics	47u	extended	5	79115	12 / 0.2161 / 2.59	27 / 0.2161 / 5.83
C136150	T520V337M006ATE025	KEMET	330u	extended	1	1419	2 / 1.278 / 2.56	5 / 1.278 / 6.39
C913186	SRP7028A-3R3M	BOURNS	SRP7028A-3R3M	extended	2	1022	4 / 0.5926 / 2.37	10 / 0.4715 / 4.71
C186700	LP5907MFX-2.8/NOPB	Texas Instruments	LP5907MFX-2.8	extended	1	612	5 / 0.4617 / 2.31	5 / 0.4617 / 2.31
C3096093	PJ-102AH	CUI	12V IN	extended	1	1682	2 / 1.075 / 2.15	5 / 1.075 / 5.38
C146656	B-3100S40P-A110	Ckmtw(Shenzhen Cankemeng)	AERIS ADAR	extended	1	1150	2 / 0.8415 / 1.68	5 / 0.8415 / 4.21
C2158038	AP22652W6-7	Diodes Incorporated	AP22652W6-7	extended	1	8442	5 / 0.3317 / 1.66	5 / 0.3317 / 1.66
C15850	CL21A106KAYNNNE	Samsung Electro-Mechanics	10u / 10u 10V	basic	21	8580560	52 / 0.0312 / 1.62	115 / 0.0312 / 3.59
C7432791	HGC1210R5476M250NSVK	Chinocera	47u 25V	extended	1	72648	5 / 0.3096 / 1.55	5 / 0.3096 / 1.55
C424540	BM20B(0.8)-34DP-0.4V(51)	HRS(Hirose)	BM20B(0.8)-34DP	extended	2	12985	6 / 0.2217 / 1.33	12 / 0.2217 / 2.66
C3035748	CH340X	WCH(Jiangsu Qin Heng)	CH340X	extended	1	33244	2 / 0.663 / 1.33	5 / 0.663 / 3.32
C96123	CL31A476MPHNNNE	Samsung Electro-Mechanics	47u	basic	2	440275	8 / 0.1629 / 1.30	14 / 0.1629 / 2.28
C98092	LQW18ANR27G00D	Murata Electronics	270n	extended	12	8690	28 / 0.0464 / 1.30	64 / 0.0464 / 2.97
C841384	LMR33630ADDAR	Texas Instruments	LMR33630ADDA	extended	1	25067	2 / 0.6319 / 1.26	5 / 0.6319 / 3.16
C167487	LQW15AN82NG00D	Murata Electronics	82n	extended	1	5317	20 / 0.0627 / 1.25	20 / 0.0627 / 1.25
C1779	CL21A475KAQNNNE	Samsung Electro-Mechanics	4.7u	basic	13	1880127	36 / 0.0343 / 1.23	75 / 0.0343 / 2.57
C49066	CL32A107MQVNNNE	Samsung Electro-Mechanics	100u	extended	1	144383	5 / 0.2469 / 1.23	7 / 0.2469 / 1.73
C135223	1XXD26000MAA	KDS Daishinku	26MHz 1XXD26000MAA	extended	1	15655	2 / 0.6106 / 1.22	5 / 0.6106 / 3.05
C1329579	SRP7028A-2R2M	BOURNS	SRP7028A-2R2M	extended	1	919	2 / 0.5599 / 1.12	5 / 0.5599 / 2.80
C53154905	ZEGMCM9070-501T	ZE	ZEGMCM9070-501T	extended	1	1400	2 / 0.5353 / 1.07	5 / 0.5353 / 2.68
C86129	LQW15AN22NG00D	Murata Electronics	22n	extended	3	29931	20 / 0.0518 / 1.04	23 / 0.0518 / 1.19
C2049745	DFE201210U-2R2M=P2	Murata Electronics	2.2u	extended	1	13808	5 / 0.2001 / 1.00	5 / 0.2001 / 1.00
C13585	CL31A106KBHNNNE	Samsung Electro-Mechanics	10u 25V	basic	2	4161599	8 / 0.121 / 0.97	14 / 0.121 / 1.69
C13832	CL31B105KCHNNNE	Samsung Electro-Mechanics	1u 100V	extended	1	247743	15 / 0.0627 / 0.94	15 / 0.0627 / 0.94
C80670	LP5907MFX-3.3/NOPB	Texas Instruments	LP5907MFX-3.3	extended	1	25871	5 / 0.165 / 0.83	7 / 0.165 / 1.16
C424541	BM20B(0.8)-34DS-0.4V(51)	HRS(Hirose)	BM20B(0.8)-34DS-0.4V(51)	extended	1	18610	4 / 0.185 / 0.74	7 / 0.185 / 1.29
C1525	CL05B104KO5NNNC	Samsung Electro-Mechanics	100n	basic	143	34579451	301 / 0.0024 / 0.72	730 / 0.0024 / 1.75
C333860	LQW2BAS1R0J00L	Murata Electronics	1u	extended	1	2956	5 / 0.1413 / 0.71	5 / 0.1413 / 0.71
C160392	BM06B-SRSS-TB(LF)(SN)	JST	BM06B-SRSS-TB	extended	1	31052	2 / 0.3518 / 0.70	5 / 0.3518 / 1.76
C337958	LQW2BASR22J00L	Murata Electronics	220n	extended	1	7145	5 / 0.1376 / 0.69	7 / 0.1376 / 0.96
C2228109	CQ0402ARNPO9BNR40	YAGEO	0.4p	extended	1	2625	20 / 0.031 / 0.62	20 / 0.031 / 0.62
C516070	JK-SMD0805-020-30V	Jinrui Electronic Materials Co.	PTC 0.2A hold	extended	1	359354	20 / 0.0312 / 0.62	20 / 0.0312 / 0.62
C703717	LQW2BASR33G00L	Murata Electronics	330n	extended	1	2739	5 / 0.1218 / 0.61	7 / 0.1218 / 0.85
C2041663	LQW15AN27NG8ZD	Murata Electronics	27n	extended	1	20701	5 / 0.1156 / 0.58	7 / 0.1156 / 0.81
C86130	LQW15ANR10J00D	Murata Electronics	100n	extended	1	7526	6 / 0.0965 / 0.58	9 / 0.0965 / 0.87
C22390021	TPD4E05U06DQAR	DOWO	TPD4E05U06DQAR	extended	3	80819	20 / 0.0289 / 0.58	21 / 0.0289 / 0.61
C1623	CL10B474KA8NNNC	Samsung Electro-Mechanics	0.47u / 470n	basic	26	1327113	62 / 0.0092 / 0.57	140 / 0.0092 / 1.29
C9006	X322525MOB4SI	YXC Crystal Oscillators	25MHz	basic	1	401525	6 / 0.0952 / 0.57	9 / 0.0952 / 0.86
C1855147	CQ0402ARNPO0BNR30	YAGEO	0.3p	extended	2	6888	20 / 0.028 / 0.56	20 / 0.028 / 0.56
C7829	SN74LVC1G07DBVR	Texas Instruments	74LVC1G07	extended	1	31104	6 / 0.0932 / 0.56	9 / 0.0932 / 0.84
C343993	PESD1CAN	BORN	PESD1CAN	extended	1	136981	6 / 0.0893 / 0.54	9 / 0.0893 / 0.80
C370392	SDWL2012CR27GSTF	Sunlord	270n	extended	1	949	5 / 0.1081 / 0.54	7 / 0.1081 / 0.76
C326067	CQ0402ARNPO9BNR20	YAGEO	0.2p	extended	1	3626	20 / 0.0267 / 0.53	20 / 0.0267 / 0.53
C143954	mSMD200-24V	TECHFUSE	PTC 2A hold	extended	1	2100	5 / 0.0994 / 0.50	7 / 0.0994 / 0.70
C577389	CQ0402BRNPO9BNR60	YAGEO	0.6p	extended	1	28169	20 / 0.0241 / 0.48	20 / 0.0241 / 0.48
C158007	B2PS-VH(LF)(SN)	JST	B2PS-VH	extended	1	44818	3 / 0.152 / 0.46	6 / 0.152 / 0.91
C43379	SMD1206P050TF/13.2	RUILON(Shenzhen Ruilongyuan Elec)	PTC 0.5A hold	extended	1	12885	5 / 0.0901 / 0.45	7 / 0.0901 / 0.63
C90061	TPS562201DDCR	Texas Instruments	TPS562201	extended	2	467651	8 / 0.0565 / 0.45	14 / 0.0565 / 0.79
C434447	SZYY0402B	Yongyu Photoelectric	HB blue	extended	1	479226	20 / 0.0215 / 0.43	20 / 0.0215 / 0.43
C341787	LQW15AN75NG00D	Murata Electronics	75n	extended	1	10694	6 / 0.0716 / 0.43	9 / 0.0716 / 0.64
C167472	LQW15AN24NG00D	Murata Electronics	24n	extended	1	18760	6 / 0.069 / 0.41	9 / 0.069 / 0.62
C108965	LQW15AN68NG00D	Murata Electronics	68n	extended	1	20176	6 / 0.0659 / 0.40	9 / 0.0659 / 0.59
C116592	TPS563201DDCR	Texas Instruments	TPS563201	extended	1	117588	6 / 0.0662 / 0.40	9 / 0.0662 / 0.60
C21516	BLM15HD102SN1D	Murata Electronics	BLM15HD102SN1	extended	2	67567	20 / 0.0195 / 0.39	20 / 0.0195 / 0.39
C310048	SMCJ33CA/TR13	Brightking	SMCJ33CA	extended	1	92658	3 / 0.1266 / 0.38	6 / 0.1266 / 0.76
C19269358	FPC-1.0FX-15PWCR-H20	XUNPU	FPC-1.0FX-15PWCR-H20	extended	1	3573	2 / 0.1919 / 0.38	5 / 0.1919 / 0.96
C19829631	SN74LVC1G17DCKR	TECH PUBLIC	SN74LVC1G17DCKR	extended	1	19187	10 / 0.0375 / 0.38	10 / 0.0375 / 0.38
C8678	SS34	MDD(Microdiode Semiconductor)	SS34	basic	1	2523304	10 / 0.0351 / 0.35	13 / 0.0351 / 0.46
C6364703	AHW1608F-1R0KTF	APV	1u	extended	2	27488	8 / 0.0418 / 0.33	14 / 0.0418 / 0.59
C78413	SMBJ18CA/TR13	Brightking	SMBJ18CA	extended	1	479678	6 / 0.0541 / 0.32	9 / 0.0541 / 0.49
C113110	LQW15AN16NG00D	Murata Electronics	16n	extended	2	12374	8 / 0.0406 / 0.32	14 / 0.0406 / 0.57
C86139	LQW18ANR22G00D	Murata Electronics	220n	extended	1	36811	6 / 0.0498 / 0.30	9 / 0.0498 / 0.45
C98095	LQW18ANR39G00D	Murata Electronics	390n	extended	1	2513	6 / 0.0495 / 0.30	9 / 0.0495 / 0.45

LCSC	Part	Maker	Value	Lib	Per board	Stock	Buy 2 / unit / cost	Buy 5 / unit / cost
C19077423	MMSZ5232B	hongjiacheng	5.6V	preferred	8	37733	20 / 0.0145 / 0.29	44 / 0.0145 / 0.64
C114502	M24C02-FMN6TP	STMicroelectronics	M24C02-FMN6TP	extended	1	13645	2 / 0.1423 / 0.28	5 / 0.1423 / 0.71
C167482	LQW15AN56NG00D	Murata Electronics	56n	extended	1	12655	6 / 0.0451 / 0.27	9 / 0.0451 / 0.41
C2827654	USBLC6-2SC6	TECH PUBLIC	USBLC6-2SC6	extended	1	203833	6 / 0.0449 / 0.27	9 / 0.0449 / 0.40
C23631	CC1206KKX7RDBB102	YAGEO	1n 2kV	extended	1	1130950	15 / 0.0179 / 0.27	15 / 0.0179 / 0.27
C25503856	XL-1005UYC	XINGLIGHT	CLK yellow	extended	1	172074	20 / 0.0132 / 0.26	20 / 0.0132 / 0.26
C108301	PBY160808T-601Y-N	Chilisin Elec	600R@100MHz	extended	6	736581	22 / 0.0114 / 0.25	40 / 0.0114 / 0.46
C167485	LQW15AN62NG00D	Murata Electronics	62n	extended	1	10983	6 / 0.041 / 0.25	9 / 0.041 / 0.37
C47339	CL05A474KP5NNNC	Samsung Electro-Mechanics	0.47u	preferred	4	532805	20 / 0.012 / 0.24	32 / 0.012 / 0.38
C12624	KT-0603G	Hubei KENTO Elec	green	extended	1	200324	20 / 0.0119 / 0.24	21 / 0.0119 / 0.25
C88219	0603B104K101NT	FH (Guangdong Fenghua Advanced Tech)	100n 100V	extended	1	1275939	20 / 0.0116 / 0.23	20 / 0.0116 / 0.23
C304314	HCB1608KF-221T20	TAI-TECH	220R@100MHz	extended	5	862918	20 / 0.0116 / 0.23	35 / 0.0116 / 0.41
C25503345	XL-1005SURC	XINGLIGHT	ADCR red / ADCS red / TX red / ERR red	extended	4	866655	26 / 0.0084 / 0.22	38 / 0.0084 / 0.32
C81464	MMBT3904LT1G	onsemi	MMBT3904	extended	4	1327801	13 / 0.0164 / 0.21	25 / 0.0164 / 0.41
C52923	CL05A105KA5NQNC	Samsung Electro-Mechanics	1u	basic	11	9471974	34 / 0.0055 / 0.19	67 / 0.0055 / 0.37
C32713279	HX PZ2.54-2x6P ZZ	hanxia	Pmod	extended	1	22794	2 / 0.093 / 0.19	5 / 0.093 / 0.46
C8545	2N7002	Jiangsu Changjing Electronics Technology Co., Ltd.	2N7002	basic	2	6047108	12 / 0.0158 / 0.19	18 / 0.0158 / 0.28
C21120	CL10B224KA8NNNC	Samsung Electro-Mechanics	220n 25V	basic	2	939812	20 / 0.0089 / 0.18	20 / 0.0089 / 0.18
C23733	CL05A475MP5NRNC	Samsung Electro-Mechanics	4.7u	basic	1	981223	20 / 0.0077 / 0.15	20 / 0.0077 / 0.15
C327229	CC0402BRNPO9BN1R3	YAGEO	1.3p	extended	1	40583	20 / 0.0074 / 0.15	20 / 0.0074 / 0.15
C25087	0402WGF2000TCE	UNI-ROYAL(Uniroyal Elec)	200	basic	21	1532334	52 / 0.0029 / 0.15	115 / 0.0029 / 0.33
C1523	0402B102K500NT	FH (Guangdong Fenghua Advanced Tech)	1n	basic	12	4102044	39 / 0.0036 / 0.14	75 / 0.0036 / 0.27
C526982	CC0402FRNPO9BN820	YAGEO	82p	extended	1	49105	20 / 0.0069 / 0.14	20 / 0.0069 / 0.14
C541342	CC0402BRNPO9BN6R2	YAGEO	6.2p	extended	1	21193	20 / 0.0068 / 0.14	20 / 0.0068 / 0.14
C576706	CC0402JRNPO9BN161	YAGEO	160p	extended	3	30334	20 / 0.0066 / 0.13	25 / 0.0066 / 0.17
C15195	CL05B103KB5NNNC	Samsung Electro-Mechanics	10n	basic	10	5492561	35 / 0.0037 / 0.13	65 / 0.0037 / 0.24
C576704	CC0402JRNPO9BN111	YAGEO	110p	extended	1	52496	20 / 0.0066 / 0.13	20 / 0.0066 / 0.13
C106200	CC0402JRNPO9BN101	YAGEO	100p	extended	31	6568451	82 / 0.0015 / 0.12	175 / 0.0015 / 0.26
C541433	CC0402FRNPO9BN130	YAGEO	13p	extended	1	12006	20 / 0.006 / 0.12	20 / 0.006 / 0.12
C25744	0402WGF1002TCE	UNI-ROYAL(Uniroyal Elec)	10k / 10k 1%	basic	33	35935096	81 / 0.0015 / 0.12	180 / 0.0015 / 0.27
C25499	4D02WGJ0220TCE	UNI-ROYAL(Uniroyal Elec)	4x22	extended	7	610280	24 / 0.0048 / 0.12	45 / 0.0048 / 0.22
C131337	B2B-PH-K-S(LF)(SN)	JST	FAN 5V	extended	1	267768	3 / 0.0356 / 0.11	6 / 0.0356 / 0.21
C21122	CL10B223KB8NNNC	Samsung Electro-Mechanics	22n	basic	1	973155	20 / 0.0056 / 0.11	20 / 0.0056 / 0.11
C327205	CC0402BRNPO9BN8R2	YAGEO	8.2p	extended	5	395624	20 / 0.0044 / 0.09	35 / 0.0044 / 0.15
C106998	CC0402JRNPO9BN151	YAGEO	150p	extended	1	535940	20 / 0.0043 / 0.09	20 / 0.0043 / 0.09
C106223	CC0402JRNPO9BN390	YAGEO	39p	extended	1	115606	20 / 0.0047 / 0.09	20 / 0.0047 / 0.09
C327209	CC0402BRNPO9BN1R8	YAGEO	1.8p	extended	1	478293	20 / 0.0043 / 0.09	20 / 0.0043 / 0.09
C527000	CC0402JRNPO9BN110	YAGEO	11p	extended	2	20404	20 / 0.0044 / 0.09	20 / 0.0044 / 0.09
C327292	CC0402BRNPO9BN1R2	YAGEO	1.2p	extended	1	115003	20 / 0.0046 / 0.09	20 / 0.0046 / 0.09
C226372	AC0402FR-0724R9L	YAGEO	24.9	extended	7	192225	24 / 0.0039 / 0.09	45 / 0.0039 / 0.18
C100316	CR0402FF2262G	LIZ Elec	22.6k	extended	1	19140	20 / 0.0043 / 0.09	20 / 0.0043 / 0.09
C106999	CC0402JRNPO9BN181	YAGEO	180p	extended	1	260215	20 / 0.0038 / 0.08	20 / 0.0038 / 0.08
C107006	CC0402JRNPO9BN331	YAGEO	330p	extended	2	291980	20 / 0.0042 / 0.08	20 / 0.0042 / 0.08

LCSC	Part	Maker	Value	Lib	Per board	Stock	Buy 2 / unit / cost	Buy 5 / unit / cost
C505468	CC0402BRNPO9BN5R6	YAGEO	5.6p	extended	2	199428	20 / 0.0042 / 0.08	20 / 0.0042 / 0.08
C541365	CC0402JRNPO9BN910	YAGEO	91p	extended	2	15658	20 / 0.0041 / 0.08	20 / 0.0041 / 0.08
C326937	CC0402BRNPO9BN2R7	YAGEO	2.7p	extended	1	91356	20 / 0.0037 / 0.07	20 / 0.0037 / 0.07
C1532	0402B223K500NT	FH (Guangdong Fenghua Advanced Tech)	22n	basic	2	609358	20 / 0.0034 / 0.07	20 / 0.0034 / 0.07
C281756	CC0402BRNPO9BN2R0	YAGEO	2p	extended	1	557810	20 / 0.0033 / 0.07	20 / 0.0033 / 0.07
C25076	0402WGF1000TCE	UNI-ROYAL(Uniroyal Elec)	100	basic	23	10081226	61 / 0.0012 / 0.07	130 / 0.0012 / 0.16
C25900	0402WGF4701TCE	UNI-ROYAL(Uniroyal Elec)	4.7k	basic	16	12626768	42 / 0.0017 / 0.07	90 / 0.0017 / 0.15
C25867	0402WGF1501TCE	UNI-ROYAL(Uniroyal Elec)	1.5k	basic	4	1108765	23 / 0.0029 / 0.07	35 / 0.0029 / 0.10
C25890	0402WGF3301TCE	UNI-ROYAL(Uniroyal Elec)	3.3k	basic	1	1526533	20 / 0.0036 / 0.07	20 / 0.0036 / 0.07
C130117	CC0402CRNPO9BN5R0	YAGEO	5p	extended	2	69734	20 / 0.0028 / 0.06	20 / 0.0028 / 0.06
C505479	CC0402CRNPO9BN7R5	YAGEO	7.5p	extended	1	23430	20 / 0.0031 / 0.06	20 / 0.0031 / 0.06
C106202	CC0402JRNPO9BN180	YAGEO	18p	extended	2	1611084	20 / 0.003 / 0.06	20 / 0.003 / 0.06
C25803	0603WAF1003T5E	UNI-ROYAL(Uniroyal Elec)	100k	basic	1	13398501	20 / 0.0029 / 0.06	20 / 0.0029 / 0.06
C281763	CC0402JRNPO9BN620	YAGEO	62p	extended	3	44145	20 / 0.0027 / 0.05	25 / 0.0027 / 0.07
C226375	AC0402FR-07255RL	YAGEO	255	extended	2	7263	20 / 0.0024 / 0.05	20 / 0.0024 / 0.05
C11702	0402WGF1001TCE	UNI-ROYAL(Uniroyal Elec)	1k	basic	16	29788366	42 / 0.0013 / 0.05	90 / 0.0013 / 0.12
C137761	RC0603FR-0724K9L	YAGEO	24.9k	extended	1	1639918	20 / 0.0023 / 0.05	20 / 0.0023 / 0.05
C106203	CC0402JRNPO9BN220	YAGEO	22p	extended	7	2205322	24 / 0.0018 / 0.04	45 / 0.0018 / 0.08
C107002	CC0402JRNPO9BN270	YAGEO	27p	extended	2	1038024	20 / 0.0018 / 0.04	22 / 0.0018 / 0.04
C107005	CC0402JRNPO9BN330	YAGEO	33p	extended	8	5461237	26 / 0.0017 / 0.04	50 / 0.0017 / 0.08
C189470	CC0402CRNPO9BN6R8	YAGEO	6.8p	extended	3	318503	20 / 0.0018 / 0.04	25 / 0.0018 / 0.04
C2933256	FRC0603F7321TS	FOJAN	7.32k	extended	1	429585	20 / 0.0019 / 0.04	20 / 0.0019 / 0.04
C25792	0402WGF4702TCE	UNI-ROYAL(Uniroyal Elec)	47k	basic	1	5394425	20 / 0.0019 / 0.04	20 / 0.0019 / 0.04
C25794	0402WGF5102TCE	UNI-ROYAL(Uniroyal Elec)	51k	basic	1	1337921	20 / 0.0019 / 0.04	20 / 0.0019 / 0.04
C25814	0603WAF3163T5E	UNI-ROYAL(Uniroyal Elec)	316k	extended	1	100550	20 / 0.0018 / 0.04	20 / 0.0018 / 0.04
C2930090	FRC0603F3092TS	FOJAN	30.9k	extended	1	279966	20 / 0.0019 / 0.04	20 / 0.0019 / 0.04
C22935	0603WAF1004T5E	UNI-ROYAL(Uniroyal Elec)	1M	basic	1	5150785	20 / 0.0018 / 0.04	20 / 0.0018 / 0.04
C107000	CC0402JRNPO9BN200	YAGEO	20p	extended	4	784495	20 / 0.0016 / 0.03	30 / 0.0016 / 0.05
C60137	CC0402JRNPO9BN470	YAGEO	47p	extended	1	2463875	20 / 0.0013 / 0.03	20 / 0.0013 / 0.03
C106199	CC0402JRNPO9BN100	YAGEO	10p	extended	2	1553969	20 / 0.0016 / 0.03	22 / 0.0016 / 0.04
C281755	CC0402JRNPO9BN240	YAGEO	24p	extended	3	273638	20 / 0.0014 / 0.03	25 / 0.0014 / 0.03
C114394	CC0402JRNPO9BN360	YAGEO	36p	extended	2	183567	20 / 0.0014 / 0.03	20 / 0.0014 / 0.03
C25120	0402WGF499JTCE	UNI-ROYAL(Uniroyal Elec)	49.9	basic	7	1213441	24 / 0.0012 / 0.03	45 / 0.0012 / 0.05
C25079	0402WGF1200TCE	UNI-ROYAL(Uniroyal Elec)	120	basic	3	3219045	21 / 0.0012 / 0.03	30 / 0.0012 / 0.04
C620468	0402WGF115JTCE	UNI-ROYAL(Uniroyal Elec)	11.5	extended	8	9670	26 / 0.0011 / 0.03	50 / 0.0011 / 0.06
C138027	RC0402FR-0724K9L	YAGEO	24.9k	extended	1	848658	20 / 0.0014 / 0.03	20 / 0.0014 / 0.03
C25905	0402WGF5101TCE	UNI-ROYAL(Uniroyal Elec)	5.1k	basic	2	4283516	20 / 0.0014 / 0.03	25 / 0.0014 / 0.03
C25977	0603WAF6041T5E	UNI-ROYAL(Uniroyal Elec)	6.04k	extended	1	85053	20 / 0.0017 / 0.03	20 / 0.0017 / 0.03
C2933071	FRC0402F1300TS	FOJAN	130	extended	2	42680	20 / 0.0009 / 0.02	20 / 0.0009 / 0.02
C3013184	FRC0402F64R9TS	FOJAN	64.9	extended	3	49037	20 / 0.0012 / 0.02	25 / 0.0012 / 0.03
C2909380	FRC0402F68R0TS	FOJAN	68	extended	1	1100108	20 / 0.0011 / 0.02	20 / 0.0011 / 0.02
C2930008	FRC0402F4301TS	FOJAN	4.3k	extended	4	251191	20 / 0.0012 / 0.02	30 / 0.0012 / 0.04
C7467414	FRC0402F1150TS	FOJAN	115	extended	1	12182	20 / 0.001 / 0.02	20 / 0.001 / 0.02
C270625	0402WGF240JTCE	UNI-ROYAL(Uniroyal Elec)	24	extended	2	190739	20 / 0.0012 / 0.02	20 / 0.0012 / 0.02
C25765	0402WGF2002TCE	UNI-ROYAL(Uniroyal Elec)	20k	basic	1	2644479	20 / 0.001 / 0.02	20 / 0.001 / 0.02
C25105	0402WGF330JTCE	UNI-ROYAL(Uniroyal Elec)	33	basic	4	4511554	23 / 0.001 / 0.02	35 / 0.001 / 0.04
C2998115	FRC0402F1911TS	FOJAN	1.91k 1%	extended	1	52813	20 / 0.0011 / 0.02	20 / 0.0011 / 0.02
C5159686	FRC0402F3831TS	FOJAN	3.83k	extended	2	34121	20 / 0.001 / 0.02	20 / 0.001 / 0.02
C25741	0402WGF1003TCE	UNI-ROYAL(Uniroyal Elec)	100k	basic	7	8467912	26 / 0.0009 / 0.02	47 / 0.0009 / 0.04
C122548	0402WGF3322TCE	UNI-ROYAL(Uniroyal Elec)	33.2k	extended	1	607611	20 / 0.001 / 0.02	20 / 0.001 / 0.02
C11457	0402WGF3241TCE	UNI-ROYAL(Uniroyal Elec)	3.24k	extended	1	78959	20 / 0.0012 / 0.02	20 / 0.0012 / 0.02
C25860	0402WGF1101TCE	UNI-ROYAL(Uniroyal Elec)	1.10k 1%	extended	1	574860	20 / 0.0012 / 0.02	20 / 0.0012 / 0.02
C85373	0402WGF1021TCE	UNI-ROYAL(Uniroyal Elec)	1.02k 1%	extended	1	19343	20 / 0.0012 / 0.02	20 / 0.0012 / 0.02
C25092	0402WGF220JTCE	UNI-ROYAL(Uniroyal Elec)	22	basic	1	4368103	20 / 0.001 / 0.02	20 / 0.001 / 0.02
C25882	0402WGF2401TCE	UNI-ROYAL(Uniroyal Elec)	2.4k	preferred	1	674152	20 / 0.0012 / 0.02	20 / 0.0012 / 0.02
C25104	0402WGF3300TCE	UNI-ROYAL(Uniroyal Elec)	330	basic	3	2196676	20 / 0.0011 / 0.02	25 / 0.0011 / 0.03
C2933083	FRC0402F2491TS	FOJAN	2.49k 1%	extended	1	1727266	20 / 0.0012 / 0.02	20 / 0.0012 / 0.02
C25123	0402WGF5100TCE	UNI-ROYAL(Uniroyal Elec)	510	basic	2	2317042	20 / 0.0011 / 0.02	22 / 0.0011 / 0.02
C25908	0402WGF5601TCE	UNI-ROYAL(Uniroyal Elec)	5.6k	preferred	1	251475	20 / 0.001 / 0.02	20 / 0.001 / 0.02
C25768	0402WGF2202TCE	UNI-ROYAL(Uniroyal Elec)	22k	basic	1	1187014	20 / 0.001 / 0.02	20 / 0.001 / 0.02
C25117	0402WGF4700TCE	UNI-ROYAL(Uniroyal Elec)	470	basic	2	2343138	20 / 0.001 / 0.02	20 / 0.001 / 0.02
C2998176	FRC0402F2103TS	FOJAN	210k	extended	1	474495	20 / 0.0011 / 0.02	20 / 0.0011 / 0.02
C17168	0402WGF0000TCE	UNI-ROYAL(Uniroyal Elec)	0	basic	1	14257259	20 / 0.0012 / 0.02	20 / 0.0012 / 0.02
C25879	0402WGF2201TCE	UNI-ROYAL(Uniroyal Elec)	2.2k	basic	3	2836474	20 / 0.0011 / 0.02	25 / 0.0011 / 0.03
C25871	0402WGF1801TCE	UNI-ROYAL(Uniroyal Elec)	1.8k	extended	1	360905	20 / 0.001 / 0.02	20 / 0.001 / 0.02
none			TC1-1-13M+		1		2 / n/a / n/a	5 / n/a / n/a

LCSC	Part	Maker	Value	Lib	Per board	Stock	Buy 2 / unit / cost	Buy 5 / unit / cost
none			Si549 LVPECL 3V3 pinout C		1		2 / n/a / n/a	5 / n/a / n/a
	Total						**1638.38**	**3878.89**

<!-- parts:end -->

Two lines changed against the BOM of 2 October, because their part ran out (`lcsc_select.py` re-run on 10 Nov):

- **22.6 kΩ:** C26960 (16 in stock, sold by the reel) → **C100316**, LIZ CR0402FF2262G. Still ±1 %, but ±200 ppm/°C against ±100.
- **PROG switch:** TL3342F160QG (0 in stock) → **TL3342F450QG**, the same switch with a 4.5 N actuation force against 1.6 N.

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5. Not from JLCPCB

Item	Why	Price
Si549 (Y401), LVPECL, 3.3 V, pinout C, 5 × 7 mm	Skyworks builds the ordering code per configuration; no LCSC code. Order from Skyworks or a distributor and consign it	Not quoted; ~$15–25 each `[E]`
TC1-1-13M+ (T1301), the mixer's input balun	LCSC's only part of that name is HLT's H3-TC1-1-13M+, a clone in a 5-pad body with another pin-out that does not fit the footprint (**RX_VU_SPEC**). Order Mini-Circuits' part from a distributor and consign it	Not quoted; ~$3 each `[E]`
Kria KV260	The host	Already bought

Source: docs/img/highres/README.md

High-Resolution (4K) & Vector Assets Gallery

> These files are not in the repository. They come as KV260-IAS2RF_highres.zip on the rev08.1 release (each older tag's release has its own); unzip it into docs/img/highres/ and the links below resolve. The scripts that make them (_work/export_schematics_and_layout.py, the render and plot scripts) write them here.

The archive provides **4K raster renders (3840 × 2160 PNG)** and **lossless vector drawings (SVG / PDF)** for detailed inspection of the final **8-layer (JLC08161H-2116C) KV260-IAS2RF** hardware, thermal/heatsink mechanical integration, Vivado 2026.1 FPGA silicon floorplans & gateware schematics, Enclosure v2 CAD/CFD/FEA, and 8-layer signal/power integrity simulations.

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1. Schematics (sch/)

- Combined single-page full wired circuit (all 12 sheets stitched onto one vector canvas):
- **FULL_CIRCUIT.pdf** · **FULL_CIRCUIT.svg** · **FULL_CIRCUIT_4k.png**
- Root hierarchy sheet:
- **KV260-IAS2RF.svg** · **ROOT_4k.png**
- Individual schematic sheets (SVG + 4K PNG):
- ADC_RADAR: **KV260-IAS2RF-ADC_RADAR.svg** · **ADC_RADAR_4k.png**
- ADC_SDR: **KV260-IAS2RF-ADC_SDR.svg** · **ADC_SDR_4k.png**
- CLOCK: **KV260-IAS2RF-CLOCK.svg** · **CLOCK_4k.png**
- CONTROL: **KV260-IAS2RF-CONTROL.svg** · **CONTROL_4k.png**
- DAC_RADAR: **KV260-IAS2RF-DAC_RADAR.svg** · **DAC_RADAR_4k.png**
- DAC_SDR: **KV260-IAS2RF-DAC_SDR.svg** · **DAC_SDR_4k.png**
- IAS_LINK: **KV260-IAS2RF-IAS_LINK.svg** · **IAS_LINK_4k.png**
- KVPWR: **KV260-IAS2RF-KVPWR.svg** · **KVPWR_4k.png**
- POWER: **KV260-IAS2RF-POWER.svg** · **POWER_4k.png**
- ROUTING: **KV260-IAS2RF-ROUTING.svg** · **ROUTING_4k.png**
- RX_VU: **KV260-IAS2RF-RX_VU.svg** · **RX_VU_4k.png**
- STATUS: **KV260-IAS2RF-STATUS.svg** · **STATUS_4k.png**

(Full 14-page multi-sheet vector PDF: the root, the composite and the 12 sheets: KV260-IAS2RF_schematic.pdf.)

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2. 8-Layer PCB Layout (layout/)

Every copper layer of the **JLC08161H-2116C** 8-layer stackup, plus composite views matching the 10-page vector layout PDF (docs/KV260-IAS2RF_layout.pdf):

- **L1 (F.Cu):** layer_01_L1_F_Cu.svg · layer_01_L1_F_Cu_4k.png
- **L2 (In1.Cu GND):** layer_02_L2_In1_GND.svg · layer_02_L2_In1_GND_4k.png
- **L3 (In2.Cu SIG):** layer_03_L3_In2_SIG.svg · layer_03_L3_In2_SIG_4k.png
- **L4 (In3.Cu PWR):** layer_04_L4_In3_PWR.svg · layer_04_L4_In3_PWR_4k.png
- **L5 (In4.Cu GND):** layer_05_L5_In4_GND.svg · layer_05_L5_In4_GND_4k.png
- **L6 (In5.Cu SIG):** layer_06_L6_In5_SIG.svg · layer_06_L6_In5_SIG_4k.png
- **L7 (In6.Cu GND):** layer_07_L7_In6_GND.svg · layer_07_L7_In6_GND_4k.png
- **L8 (B.Cu):** layer_08_L8_B_Cu.svg · layer_08_L8_B_Cu_4k.png
- **Combined 8 layers:** layer_09_all_8_layers.svg · layer_09_all_8_layers_4k.png
- **Transparent tracks (GND & PWR copper pours removed):** layer_10_tracks_transparent.svg · layer_10_tracks_transparent_4k.png

PSU board, 4 layers (psu_layout/)

The pages of `KV260-IAS2RF_PSU_layout.pdf`, from `psu/psu.kicad_pcb` with its zones refilled on a copy:

- **L1 (`F.Cu`):** `psu_01_L1_F_Cu.svg` · `psu_01_L1_F_Cu_4k.png`
- **L2 (`In1.Cu` GND):** `psu_02_L2_In1_GND.svg` · `psu_02_L2_In1_GND_4k.png`
- **L3 (`In2.Cu` +12V):** `psu_03_L3_In2_12V.svg` · `psu_03_L3_In2_12V_4k.png`
- **L4 (`B.Cu`):** `psu_04_L4_B_Cu.svg` · `psu_04_L4_B_Cu_4k.png`
- **All four, translucent overlay:** `psu_05_all_4_layers.svg` · `psu_05_all_4_layers_4k.png`

3. Vivado 2026.1 FPGA Silicon Floorplans & Schematics (`fpga/`)

Generated directly from post-route Vivado 2026.1 checkpoints (**`docs/FPGA_GATEWARE.md`**):

- **Artix-7 `XC7A50T-FTG256-2` Silicon Die Floorplan (utilisation in the FPGA figures table):**
- `artix7_silicon_floorplan.pdf` · `artix7_silicon_floorplan.svg` · `artix7_silicon_floorplan_4k.png`
- **Artix-7 `artix_top` Post-Route Circuit Schematic:**
- `artix7_vivado_schematic.pdf` · `artix7_vivado_schematic.svg` · `artix7_vivado_schematic_4k.png`
- **Kria K26 `XCK26-SFVC784-2LV-c` Silicon Die Floorplan (full `ias2rf_k26_bd` block design; utilisation in the FPGA figures table):**
- `kria_k26_silicon_floorplan.pdf` · `kria_k26_silicon_floorplan.svg` · `kria_k26_silicon_floorplan_4k.png`
- **Kria K26 PS + PL `ias2rf_k26_bd` Block Design & PL Circuit Schematic:**
- `kria_k26_vivado_bd_schematic.pdf` · `kria_k26_vivado_bd_schematic.svg` · `kria_k26_vivado_bd_schematic_4k.png`
- **Dual-FPGA AERIS-10 Radar + Wideband SDR Signal-Chain Architecture:**
- `dsp_radar_sdr_pipeline_schematic.pdf` · `dsp_radar_sdr_pipeline_schematic.svg` · `dsp_radar_sdr_pipeline_schematic_4k.png`

4. Hardware, Heatsink & Enclosure 4K Renders (`renders/`)

- **Bare Adapter PCB (`3840 × 2160` KiCad raytrace):**
- `board_iso_4k.png` · `board_top_4k.png` · `board_bottom_4k.png`
- **Heatsink Placement, Envelope & Sizing (`3840 × 2160` Cycles + Vector Map):**
- `board_heatsinks_4k.jpg` (annotated 4K overview with ghosted `50 × 50 × 15 mm` overhead fan)
- `board_heatsinks_clean_4k.jpg` (clean 4K render without overlays)
- `board_heatsinks_closeup_4k.jpg` (4K macro on `HS1`–`HS4` showing `4.0 mm` air gap between `HS2` `U401` and `HS3` `Y401`)
- `heatsink_mechanical_map.svg` (vector CAD keep-out, height budget, and sizing table)
- **Enclosure v2 & KV260 Assembly (`3840 × 2160` Cycles OPTIX + Reference Views):**
- `case_v2_closed_4k.jpg` · `case_v2_open_4k.jpg` · `case_v2_section_4k.jpg`
- The 1600-px Enclosure v1/v2, FEA and mount views (`case_*.jpg`, `case3d_*.jpg`, `mount_*.jpg`) are in **`docs/img/`**.
- The Blender 4K views are published as JPEG (q90); their PNG masters stay out of the repository (`_work/mech/publish_4k.py`).

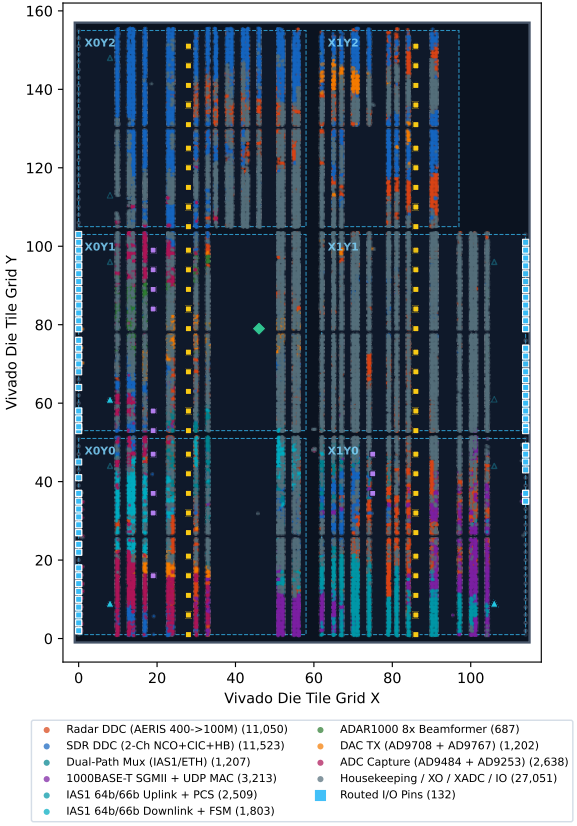
5. Signal & Power Integrity Vector Plots (`sim/`)

- `eyes_1g.svg` · `eye_openings.svg` · `lvds_skew.svg` · `pdn_impedance.svg` · `sma_launch.svg` · `dac_filters.svg`

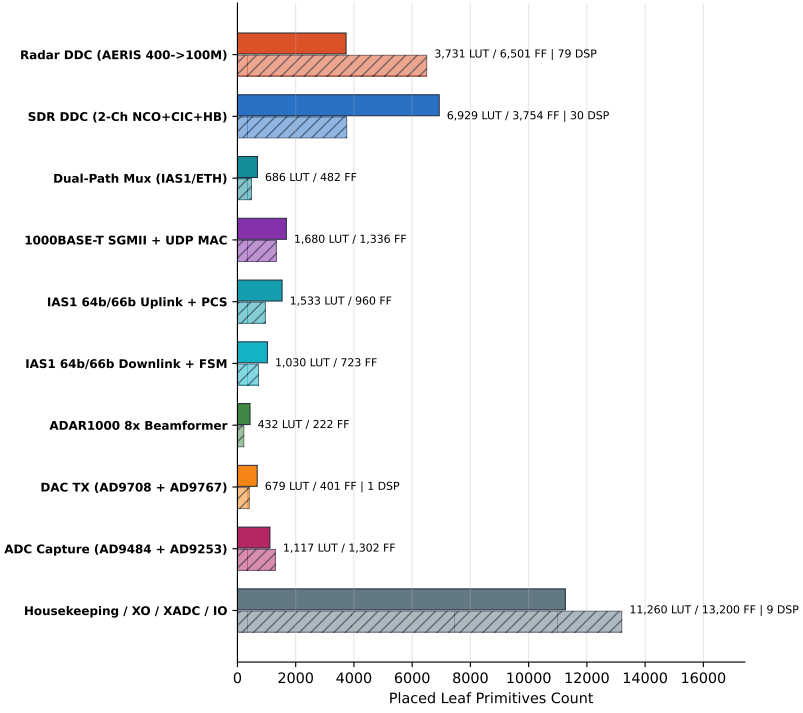
Appendix A: Vivado FPGA Silicon & Schematics

Lossless vector Artix-7 XC7A50T & Kria K26 floorplans and post-route circuit diagrams

Artix-7 XC7A50T-FTG256-2 Silicon Die Occupancy & Post-Route Placement



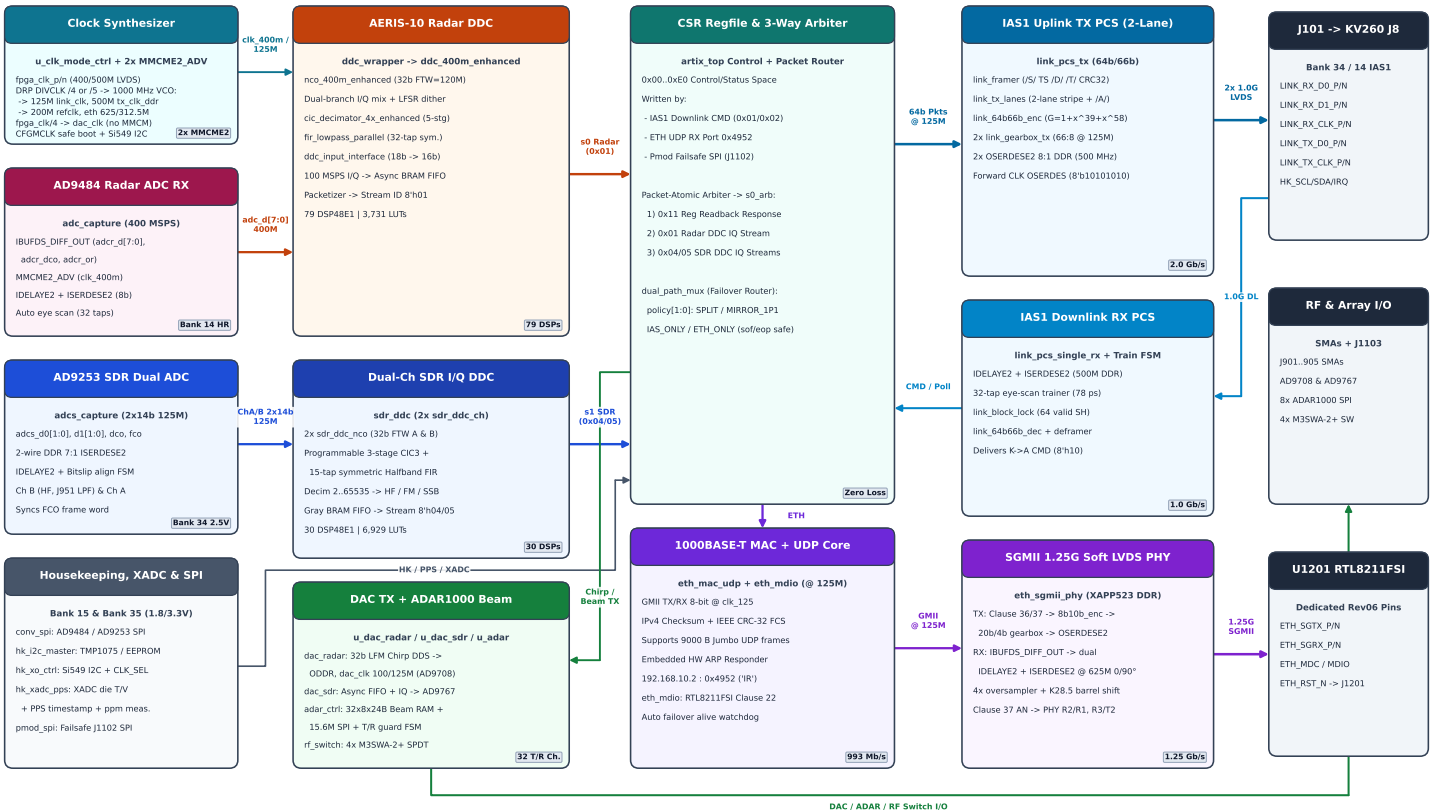
Subsystem Silicon Consumption (Vivado Post-Route)

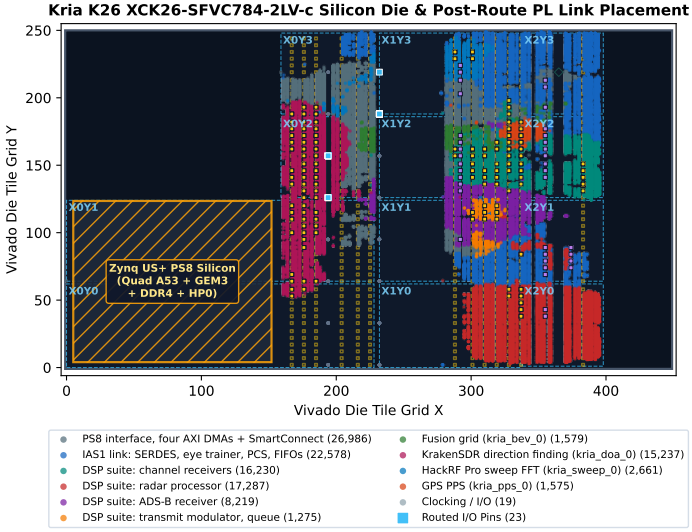


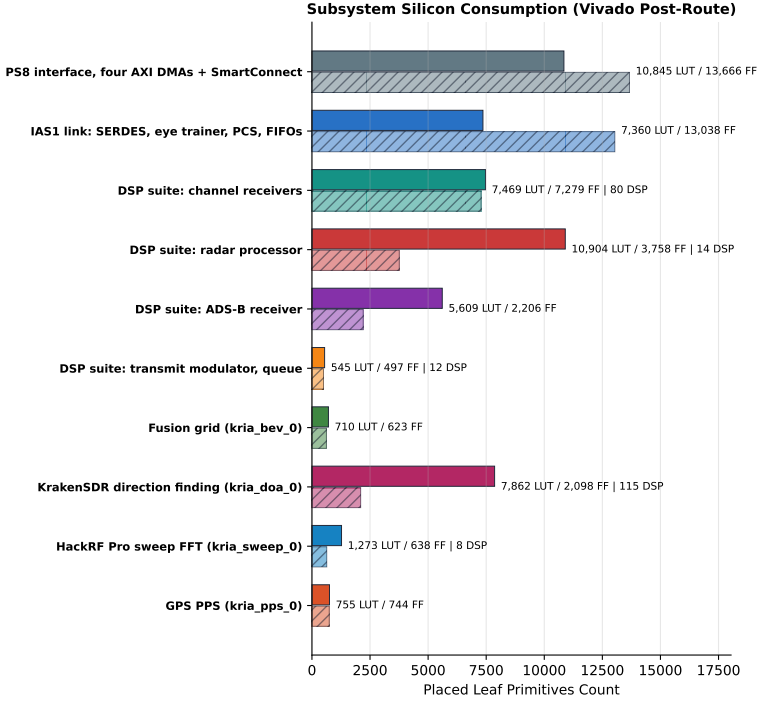

```
Device: XC7A50T-FTG256-2 (Artix-7)
Top: artix_top (ENABLE_ETH=1), post-route, Vivado 2026.1
Slice LUTs: 25,068 / 32,600 (76.9%)
FFs:        28,881 / 65,200 (44.3%)
DSP:        119 / 120 (99.2%)
BRAM36 eq.: 18 / 75 (24.0%: 13 RAMB36 + 10 RAMB18)
Timing:     WNS = +0.076 ns | WHS = +0.049 ns
```

Artix-7 XC7A50T-FTG256-2 (artix_top): Vivado Post-Route Hierarchical Circuit Schematic

Clock Domains: fpga_clk 400/500M | dac_clk 100/125M (no MMCM) | link_clk 125M | tx_clk_ddr 500M | clk_400m 400M | clk_625 625M | cfgmclk | WNS = +0.076 ns, WHS = +0.049 ns



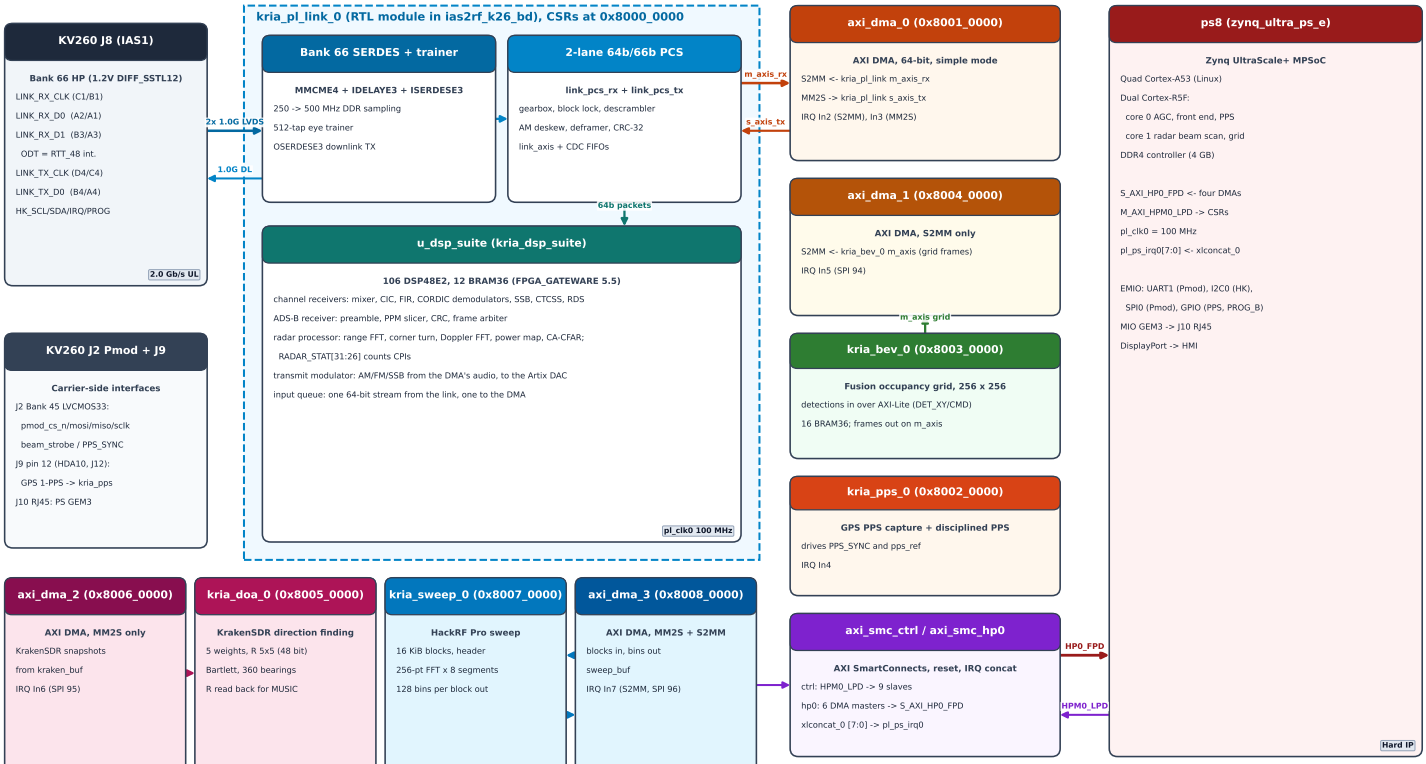





```
Device: XCK26-SFVC784-2LV-c (Kria K26)
Top: ias2rf_k26_bd_wrapper (full block design), post-route
Slice LUTs: 51,870 / 117,120 (44.3%)
FFs:        44,547 / 234,240 (19.0%)
DSP:        229 / 1248 (18.3%)
BRAM36 eq.: 40 / 144 (27.8%: 36 RAMB36 + 8 RAMB18)
Timing:     WNS = +1.125 ns | WHS = +0.010 ns
```

Kria KV260 XCK26-SFVC784-2LV-c: Vivado IPI Block Design (ias2rf_k26_bd) & PL Link Circuit

PS8 + kria_pl_link (link, DSP suite) + kria_pps + kria_bev (fusion grid) + kria_doa + kria_sweep + four AXI DMAs into DDR4 | BD WNS = +1.125 ns, WHS = +0.010 ns



KV260-IAS2RF DSP, Wideband SDR & 10.5 GHz Phased-Array Radar Gateware Pipelines

AERIS-10 400 MSPS Radar DDC | AD9253 125 MSPS Dual-Ch HF/VHF/UHF SDR DDC | LFM Chirp TX DACs | 8x ADAR1000 SPI Beamformer

CHAIN A: AERIS-10 10.5 GHz Radar RX Digital Down-Converter (400 MSPS -> 100 MSPS Complex I/Q -> 0.8 / 1.6 Gb/s)

J905 SMA -> AD9484
- U501 8b 400 MSPS
- 120 MHz IF +/- 50 MHz
- ad9484_radar_model (sim)
- 8-bit LVDS DDR -> ISERDES

nco_400m_enhanced
- 6-Stage Pipelined DDS
- 32b FTW = 0x4CCCCCCD
- fs=400M -> LO=-120.0 MHz
- LFSR dither + cos/sin LUT

I/Q Mixer & CIC4x
- cic_decimator_4x_enhanced
- 8b x 16b DSP48E1 complex
- 5-stage CIC decimate 4x
- 400 MSPS -> 100 MSPS

fir_lowpass_parallel
- 32-Tap Symmetric FIR
- 100 MHz droop comp. LPF
- Folded DSP48E1 MACs
- 18b -> 16b ddc_input_int.

Async FIFO + Post-Dec
- ddc_wrapper
- POST_DECIM = 1 (100M) or
- 4 (25M -> 0.80 Gb/s)
- 64-bit {Q1,I1,Q0,I0}

Stream 8'h01
- To Dual-Path Mux
- 1000/125M -> IAS1 or ETH
- PPS 64b timestamping
- AERIS-10 20 km CFAR

CHAIN B: Wideband Dual-Channel SDR RX (HF/CB 0-62.5 MHz Direct + VHF/FM/Walkie/UHF IF via Mixer -> J901/J902 SMAs)

J901/J902 -> AD9253
- U601 Dual 14b 125 MSPS
- ChA: HF/CB 0.5-55 MHz
- ChB: VHF/UHF external IF
- 2-wire 7:1 ISERDES + FCO

2x sdr_ddc_nco
- Independent 32b Tuning
- 0x44 SDR_DDC_NCO_A
- 0x48 SDR_DDC_NCO_B
- 29.1 mHz tuning step

3-Stage CIC3 Decim
- Programmable Decim R
- AM/CB/Walkie narrow ch.
- FM 200 kHz / Wide 25M
- 16b convergent scale

15-Tap Halfband FIR
- Sysclk Transition Comp.
- Symmetric polyphase MAC
- 80 dB stopband alias rej.
- Bypasses when R < 4

Dual-Clock Gray FIFO
- adcs_clkdiv -> link_clk
- 2 independent I/Q FIFOs
- Programmable words/pkt
- Saturating drop counter

Streams 8'h04/05
- Simultaneous RX
- Coherent ChA + ChB
- Sent via ETH UDP / IAS1
- Demod on K26 ARM/PL

CHAIN C: AERIS-10 8x ADAR1000 Phased-Array & RF Switch Engine

Beam Table BRAM
- 32 Beams x 8 x 24 Bytes
- Reg 0x088 ADAR_TBL_WR
- Stores Ch1..4 RX/TX gain
- & I/Q vector weights

T/R Safe Guard FSM
- adar_ctrl + rf_switch
- guard_pre/post deadtime
- BEAM_STROBE hw trigger
- 4x M3SWA-2+ 1 us settle

J1103 Ribbon 1.8V
- 8x ADAR1000 Array
- 15.625 MHz Mode-0 SPI
- CSB[7:0], TR[7:0], LOAD
- 32 X-band T/R elements

AERIS-10 10.5 GHz / 20 km Array Coordination

auto_tr_chirp Synchronized Pulse Timing

1) Load beam ID -> wait guard_pre -> assert ADAR_TR=1 (TX) & M3SWA-2+ TX path
2) Pulse AD9708 LFM Chirp for pulse_len -> wait guard_post -> switch ADAR_TR=0 (RX)
3) AD9484 captures 400 MSPS echo -> 100 MSPS DDC -> K26 20 km pulse compression

CHAIN D: Radar LFM Chirp TX (AD9708) & Wideband SDR I/Q TX (AD9767)

LFM Chirp DDS
- dac_radar (125 MSPS)
- FTW(n) = f0 + n * df
- Up/down chirp + PRI FSM
- Q15 sine LUT + amp_scale

ODDR Clock & TX
- AD9708 (U701) -> J904
- Center-aligned ODDR clk
- (D1=0,D2=1) -> t_S/t_H met
- 3rd-order LPF + ADT2-1T+

J904 Radar TX
- 10-50 MHz Chirp IF
- Drives AERIS upconverter
- 10.5 GHz X-band PA
- Cal loopback to RX SMAs

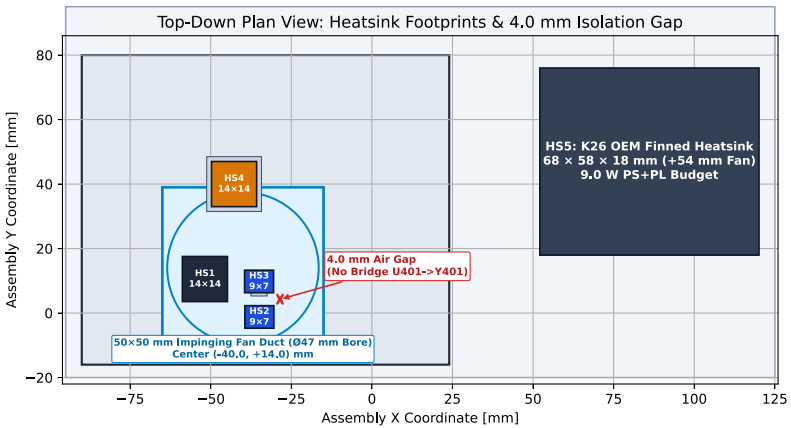
SDR Dual-DAC FIFO & Mux
- dac_sdr (64b -> 2x14b I/Q)
- K26 MM2S Stream -> link_clk
- -> 125 MSPS IQSEL DDR bus
- Saturating underflow monitor

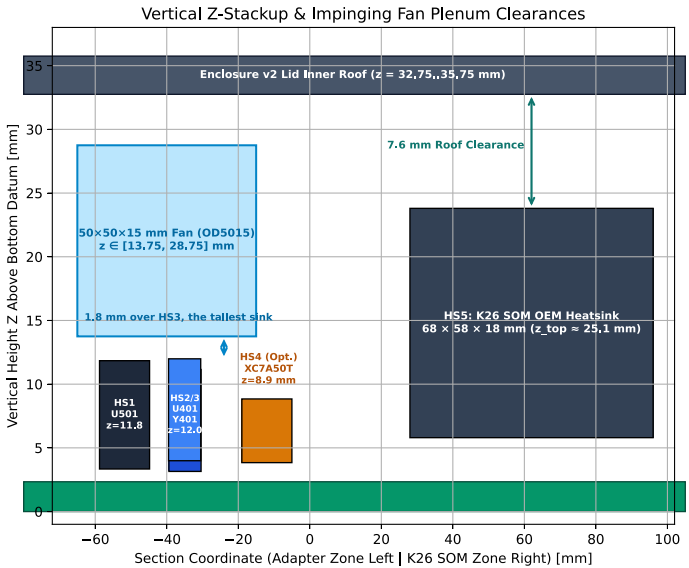
AD9767 (U801) -> J903/T801/T802
- Dual 14b 125 MSPS I/Q TX
- IQWRT + IQCLK interleaved
- 50-Ohm diff LPF + baluns
- HF/CB direct TX & VHF/UHF IF

Appendix B: Heatsink Mechanical Keep-Out Drawing

Lossless vector dimensions, clearances & HS1-HS5 thermal zones

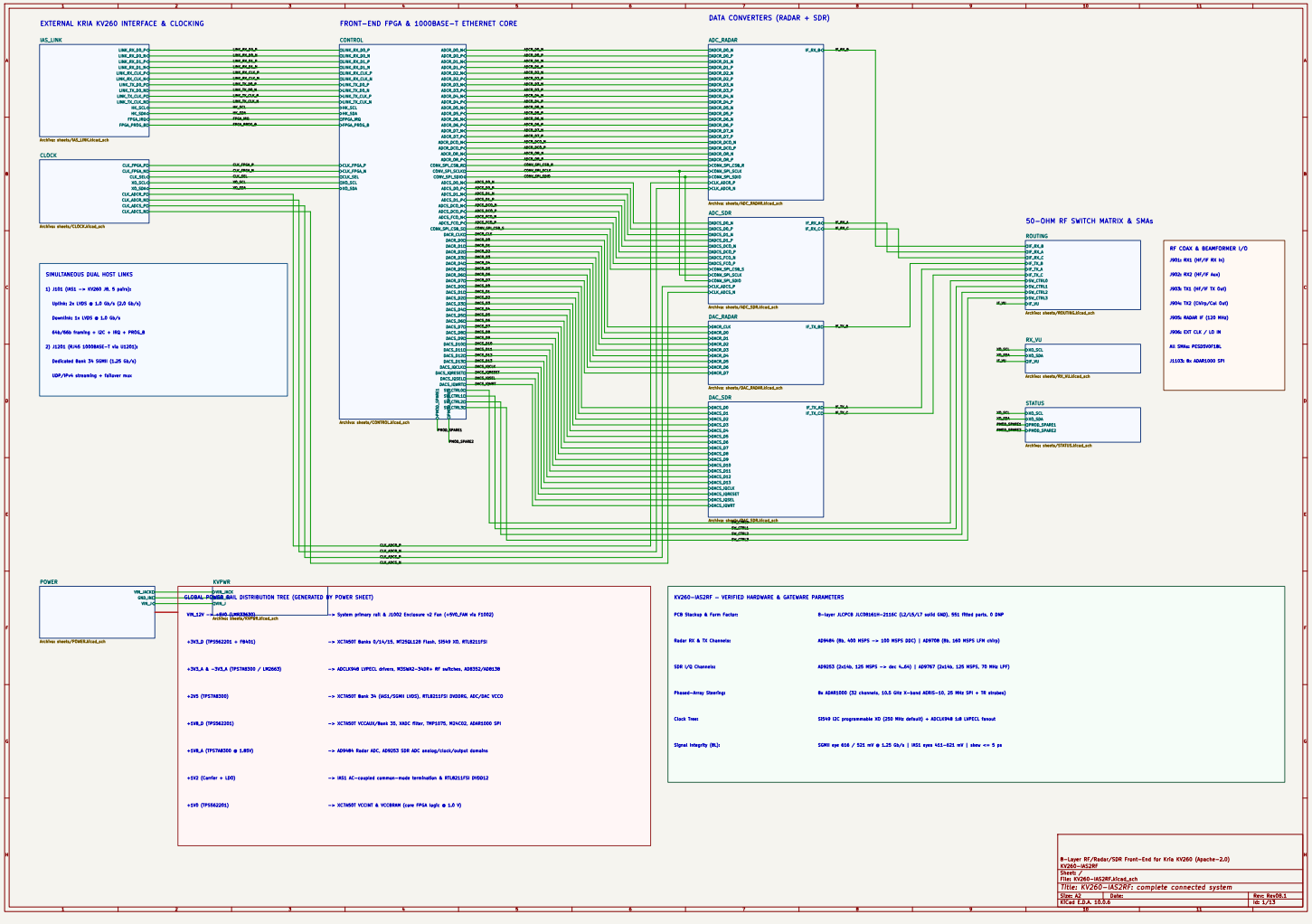
KV260-IAS2RF Mechanical Heatsink Sizing, Coordinates & Enclosure v2 Clearances

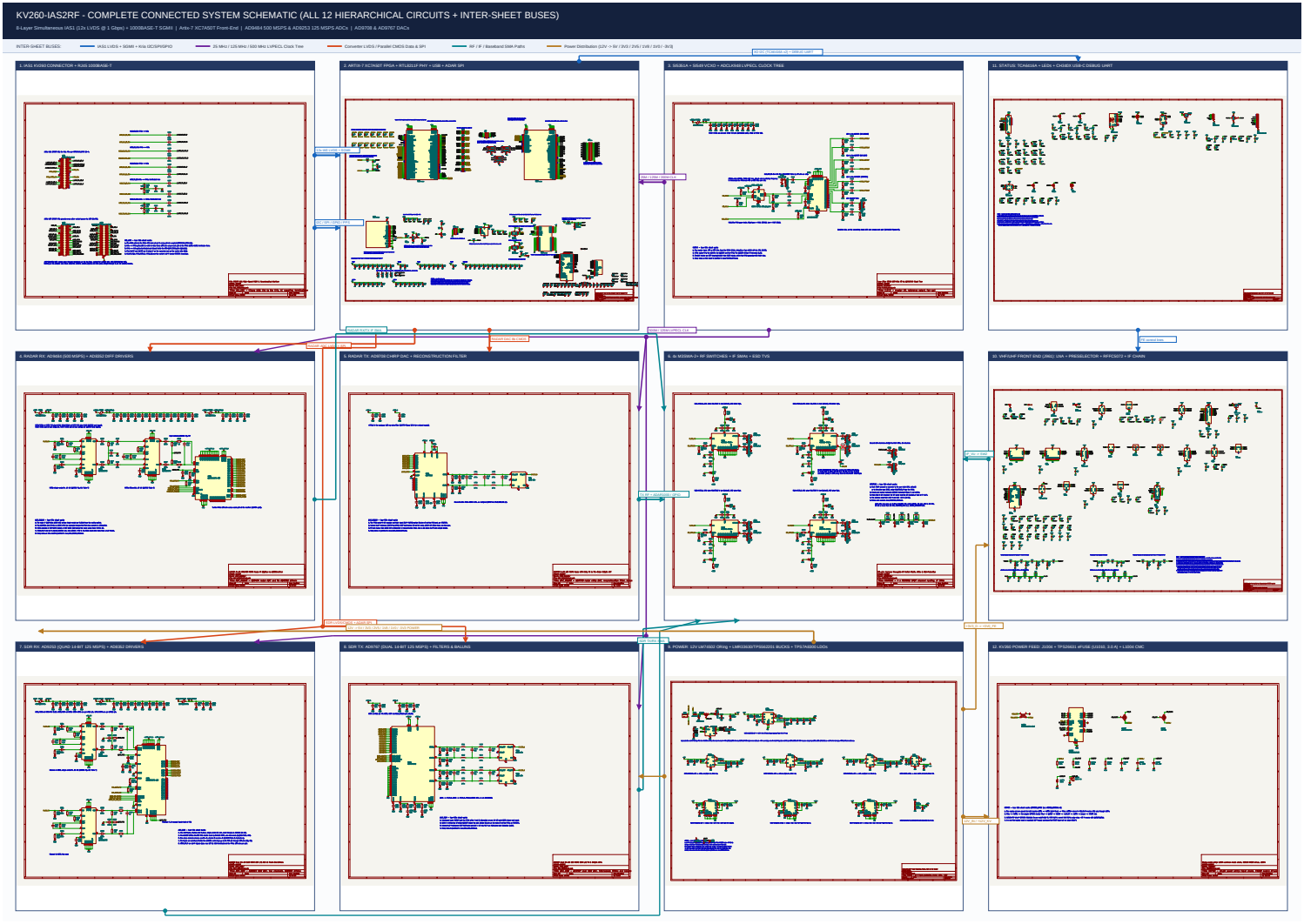


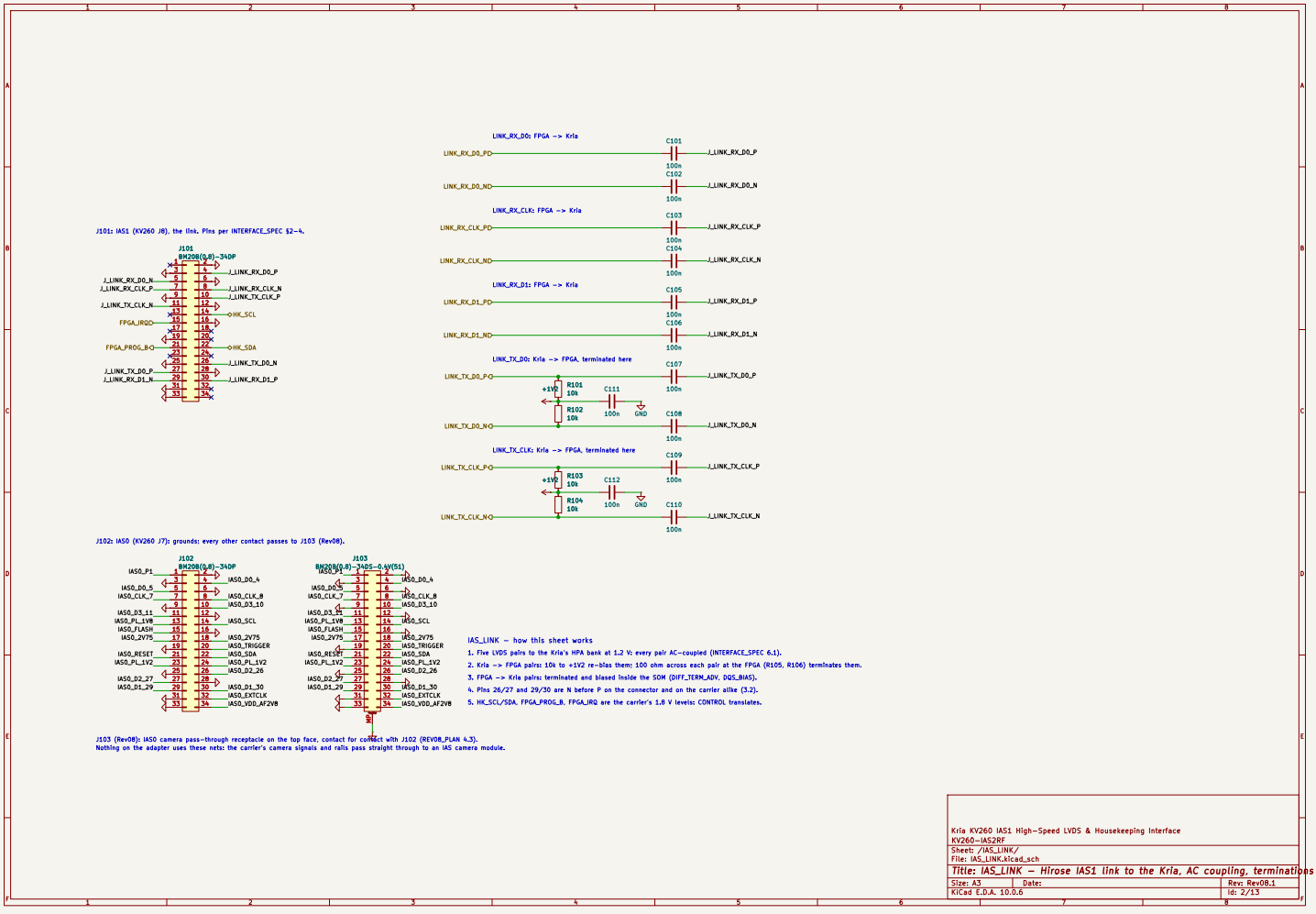


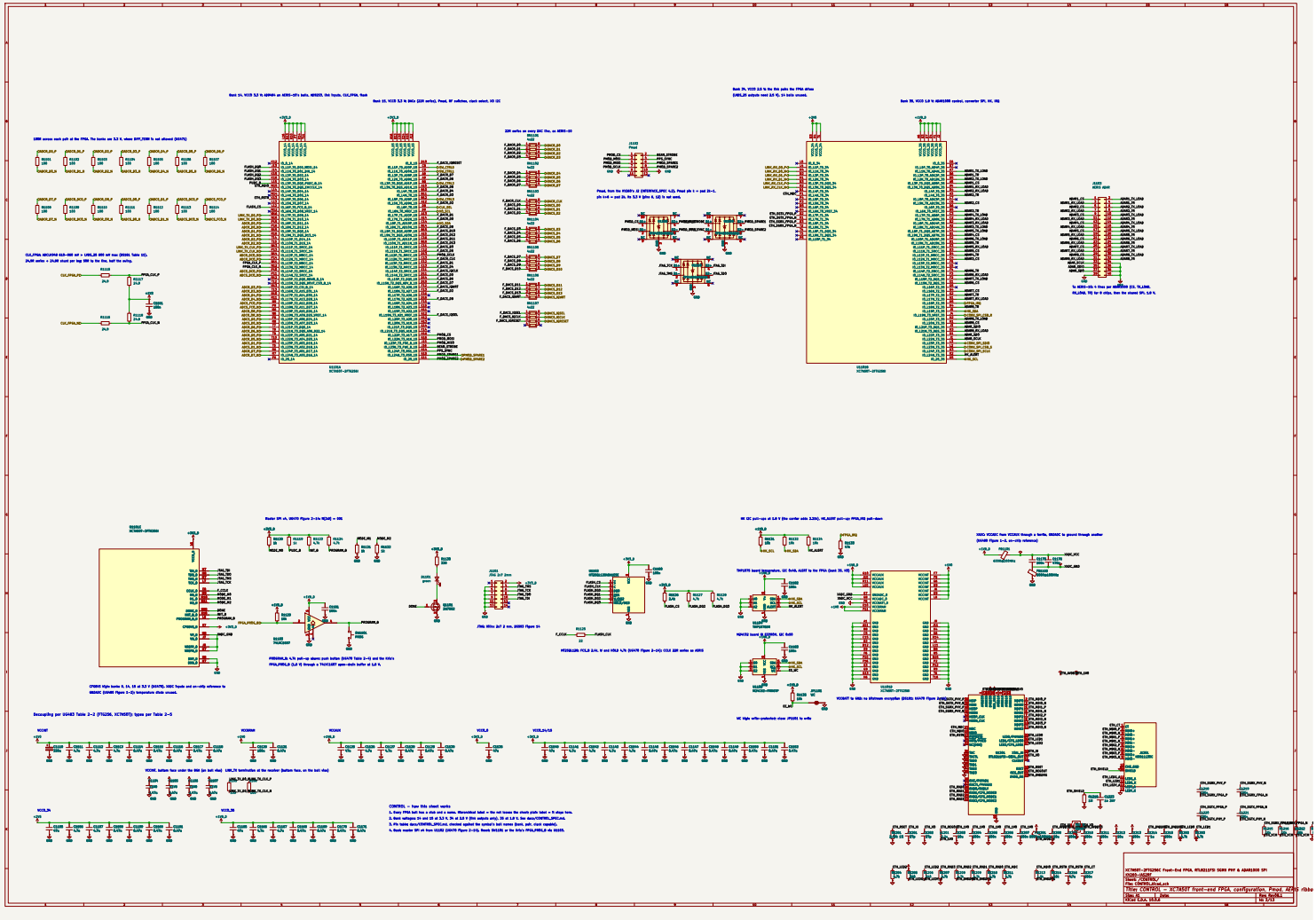
Appendix C: 14-Page Hierarchical KiCad Schematic

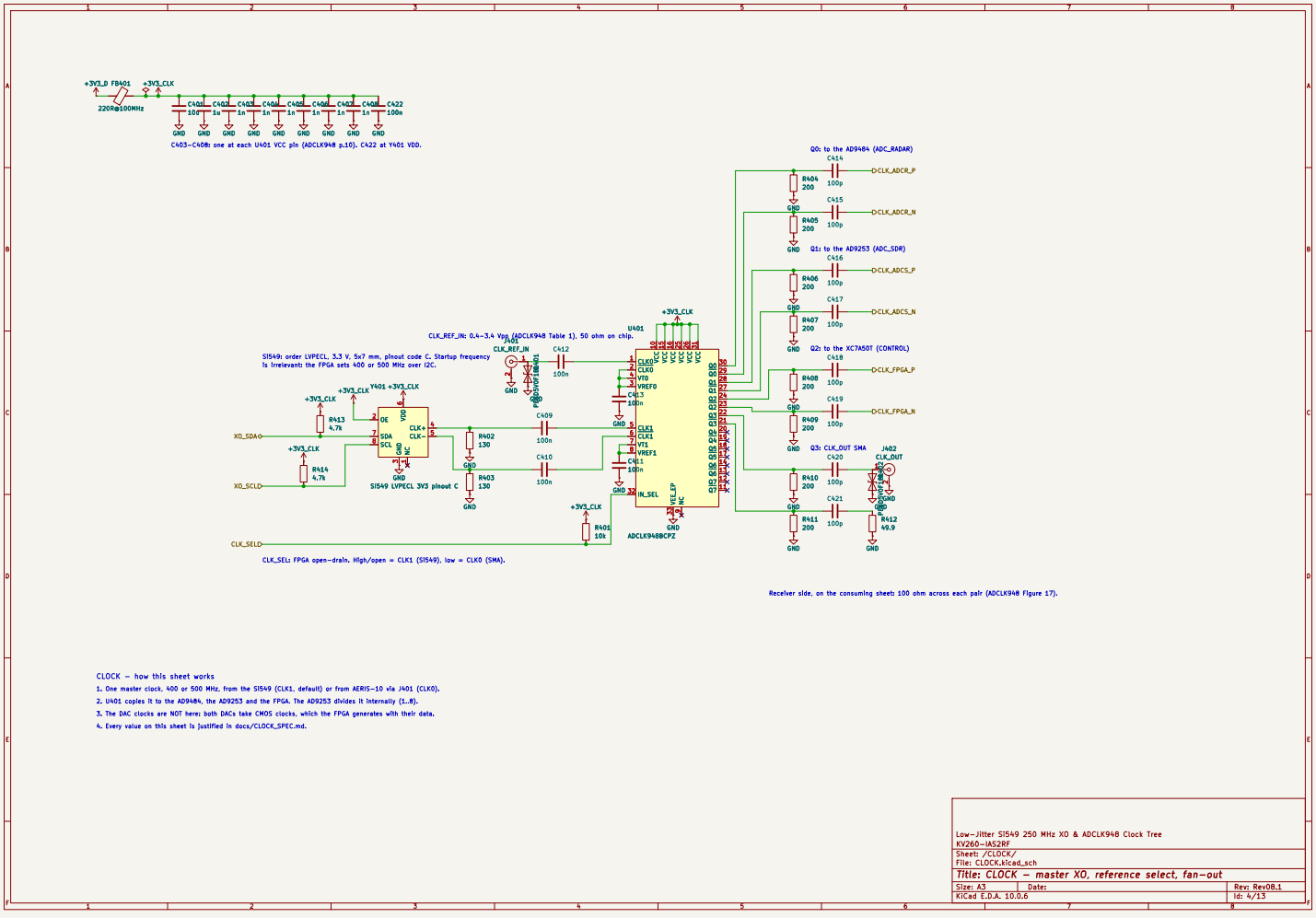
Complete connected overview + all 12 hierarchical schematic sheets (14 vector pages)

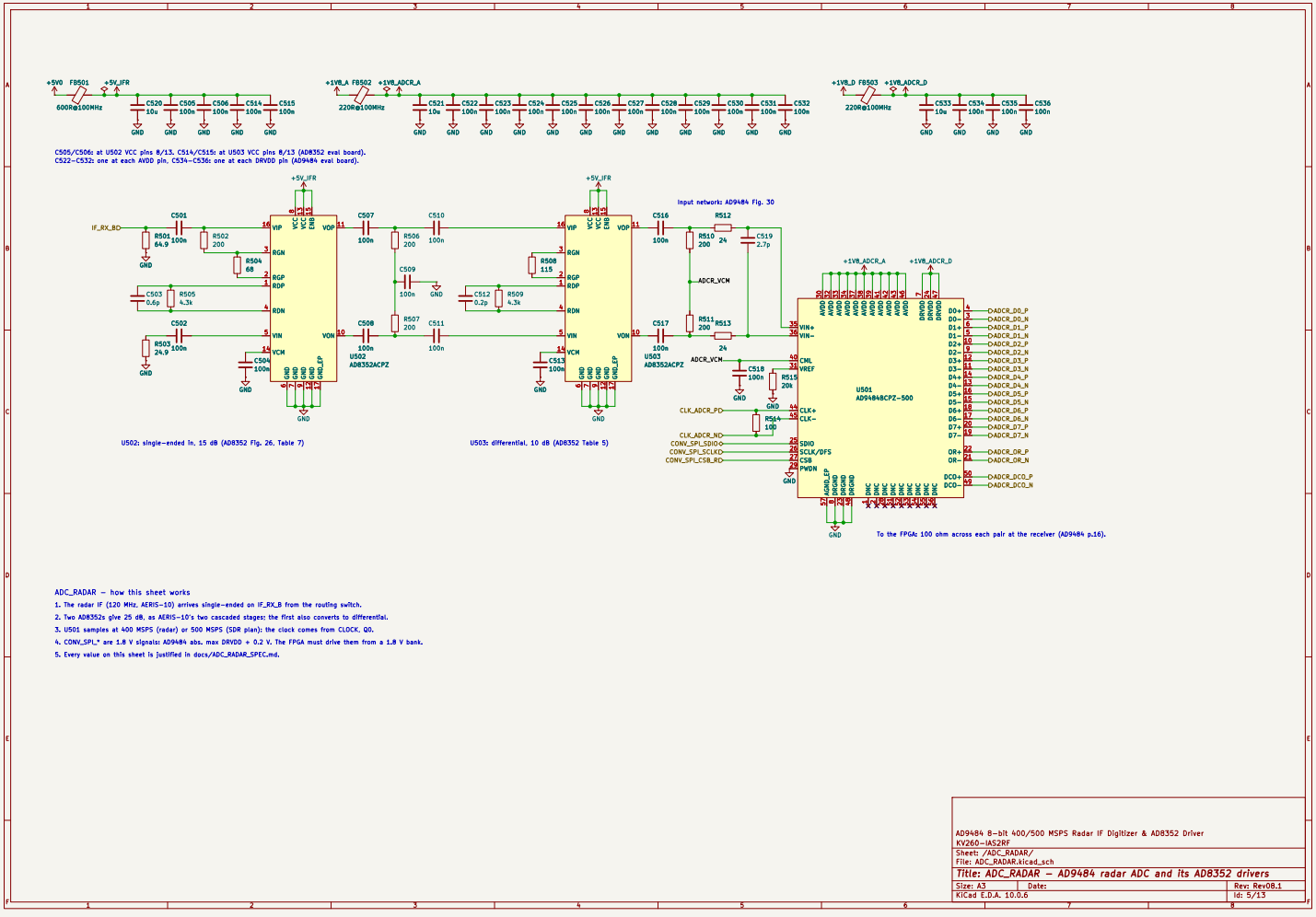

EXTERNAL KRIA KV260 INTERFACE & CLOCKING
FRONT-END FPGA & 1000BASE-T ETHERNET CORE
DATA CONVERTERS (RADAR + SDR)
IAS_LINK
CONTROL
ADC_RADAR
CLOCK
ADC_SDR
50-OHM RF SWITCH MATRIX & SMAs
ROUTING
SIMULTANEOUS DUAL HOST LINKS
1) J101 (IAS1 -> KV260 /M.5 pairs):
Uplink: 2x LVDS @ 1.0 Gb/s (2.0 Gb/s)
Downlink: 1x LVDS @ 1.0 Gb/s
64b/66b framing + I2C + IRQ + PMOD_B
2) J120: (RJ45 1000BASE-T via U120):
Dedicated Bank 34 SGMII (1.25 Gb/s)
UDP/IPv4 streaming + failover mux
DAC_RADAR
DAC_SDR
RF COAX & BEAMFORMER I/O
J901: RX1 (HF/VF RX 1)
J902: RX2 (HF/VF Aux)
J903: TX1 (HF/VF TX Out)
J904: TX2 (Chirp/Cal Out)
J905: RADAR IF (120 MHz)
J906: EXT CLK / LO IN
A5 SMAs: PCSD5V0T1BL
J1103: 8x ADAR1000 SPI
RX_VU
STATUS
POWER
KVPWR
GLOBAL POWER RAIL DISTRIBUTION TREE (GENERATED BY POWER SHEET)
+3V3_D (TPS562201 + FB401)
-> XC7A50T Banks 0/14/15, MT25QL128 Flash, SI549 XO, RTL8211FSI
+3V3_A & -3V3_A (TPS7A8300 / LM2663)
-> ADCLK948 LVPECL drivers, M3SWA2-34DR+ RF switches, AD8352/AD8138
+2V5 (TPS7A8300)
-> XC7A50T Bank 34 (IAS1/SGMII LVDS), RTL8211FSI DVDDRG, ADC/DAC VCCO
+1V8_D (TPS562201)
-> XC7A50T VCCAUX/Bank 35, XADC filter, TMP1075, M24C02, ADAR1000 SPI
+1V8_A (TPS7A8300 @ 1.85V)
-> AD9484 Radar ADC, AD9253 SDR ADC analog/clock/output domains
+1V2 (Carrier + LDO)
-> IAS1 AC-coupled common-mode termination & RTL8211FSI DVDD12
+1V0 (TPS562201)
-> XC7A50T VCCINT & VCCBRAM (core FPGA logic @ 1.0 V)
KV260-IAS2RF — VERIFIED HARDWARE & GATEWARE PARAMETERS
PCB Stackup & Form Factor:
8-layer AXPCB JLCP8161H-2116C (L2/L5/L7 solid GND), 551 fitted parts, 0 DNP
Radar RX & TX Channels:
AD9484 (8b, 400 MSPS -> 100 MSPS DDC) | AD9708 (8b, 165 MSPS LFN chirp)
SDR I/Q Channels:
AD9253 (2x14b, 125 MSPS -> dec 4…64) | AD9767 (2x14b, 125 MSPS, 70 MHz LPF)
Phased-Array Steerings:
8x ADAR1000 (32 channels, 10.5 GHz X-band AESAs-10, 25 MHz SPI + TR strobes)
Clock Trees:
SI549 I2C programmable XO (250 MHz default) + ADCLK948 1:8 LVPECL fanout
Signal Integrity (SI):
SGMII eye 616 / 521 mV @ 1.25 Gb/s | IAS1 eyes 411–621 mV | skew <= 5 ps
8-Layer RF/Radar/SDR Front-End for Kria KV260 (Apache-2.0)
KV260-IAS2RF
Sheets /
Files KV260-IAS2RF.kicad_sch
Title: KV260-IAS2RF: complete connected system
Size: A2
Date:
Rev: Rev05.1
KiCad E.D.A. 10.0.0
Id: 1/13

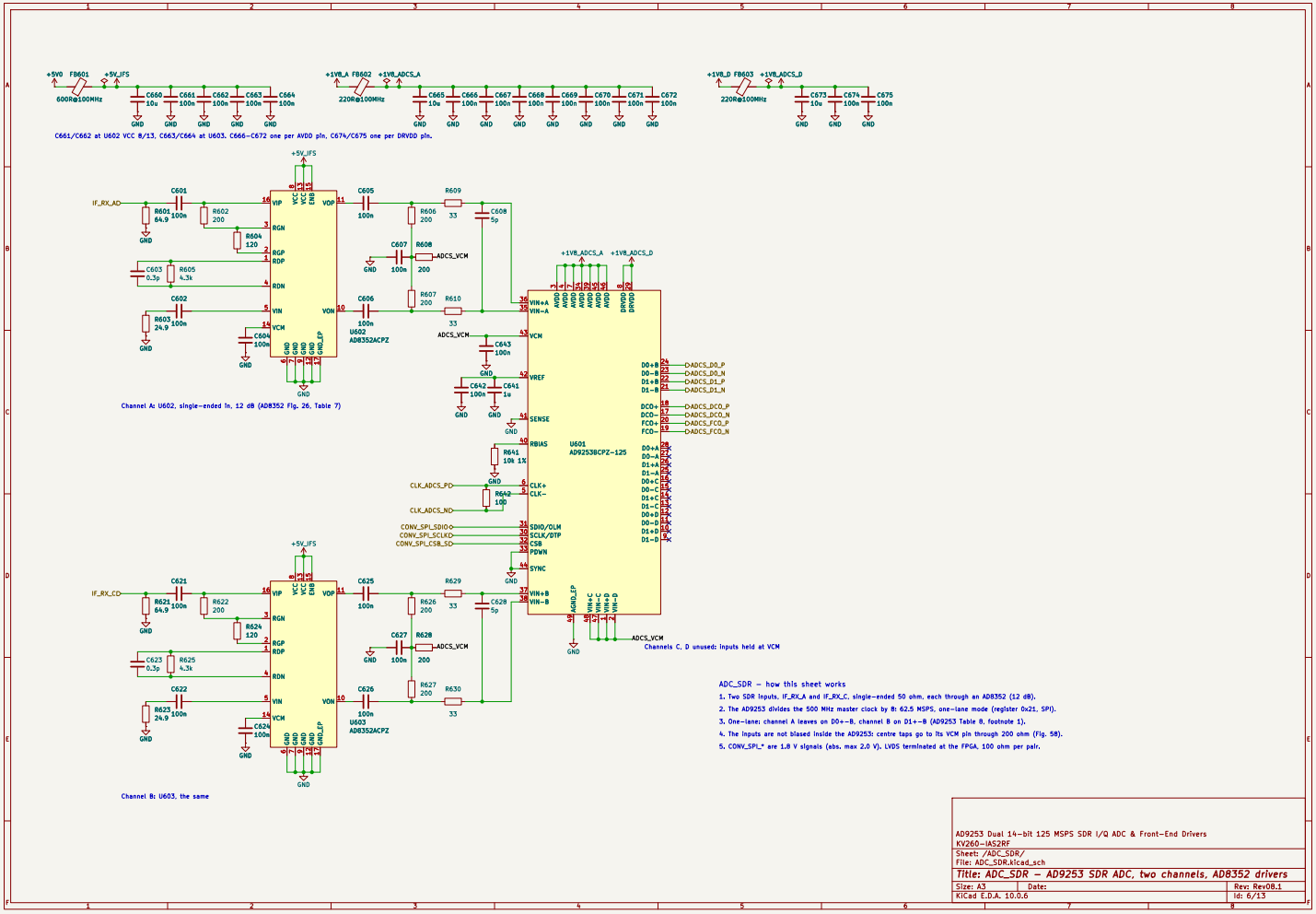

KV260-IAS2RF - COMPLETE CONNECTED SYSTEM SCHEMATIC (ALL 12 HIERARCHICAL CIRCUITS + INTER-SHEET BUSES)
8-Layer Simultaneous IAS1 (12x LVDS @ 1 Gbps) + 1000BASE-T SGMII | Artix-7 XC7A50T Front-End | AD9484 500 MSPS & AD9253 125 MSPS ADCs | AD9708 & AD9767 DACs
INTER-SHEET BUSES:
IAS1 LVDS + SGMII + Kria I2C/SPI/GPIO
25 MHz / 125 MHz / 500 MHz LVPECL Clock Tree
Converter LVDS / Parallel CMOS Data & SPI
RF / IF / Baseband SMA Paths
Power Distribution (12V -> 5V / 3V3 / 2V5 / 1V8 / 1V0 / 3V3)
1. IAS1 KV260 CONNECTOR + RJ45 1000BASE-T
2. ARTIX-7 XC7A50T FPGA + RTL8211F PHY + USB + ADAR SPI
3. SKiLEA + SI549 VCXO + ADCLK948 LVPECL CLOCK TREE
11. STATUS: TCA6416A + LEDs + CH340E USB-C DEBUG UART
4. RADAR RX: AD9484 (500 MSPS) + AD9262 DIFF DRIVERS
5. RADAR TX: AD9708 CHIRP DAC + RECONSTRUCTION FILTER
6. SI-M3399A-J+ RF SWITCHES + IF SMPA + ESD TVS
10. VHF/UHF FRONT-END (J3661) LNA + PRESELECTOR + RFFC5072 + IF CHAIN
7. SDR RX: AD9253 (QUAD 14-BIT 125 MSPS) + AD9262 DRIVERS
8. SDR TX: AD9767 (DUAL 14-BIT 125 MSPS) + FILTERS & BALUNS
9. POWER: 12V (JST-6)/2 ORing + LMR33630/TPS562201 BUCKS + TPS7A8300 LDOs
12. KV260 POWER FEED: 2x304 + TPS25801 ePUSE (11210, 3.0 A) + L1554 CMC

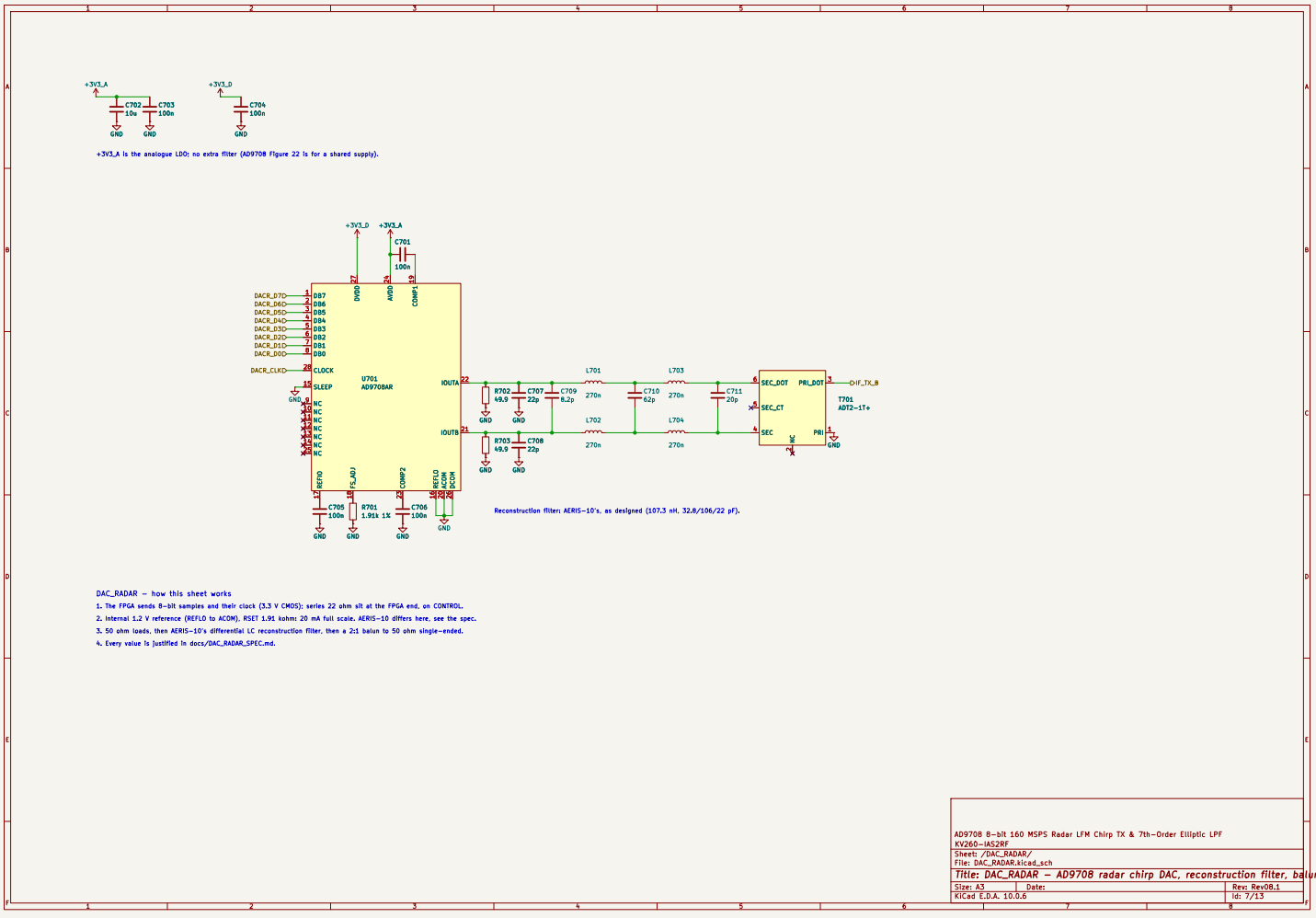

J101: IAS1 (KV260 J8), the link. Pins per INTERFACE_SPEC §2-4.
J101
BH20B(0.8)-34DP
J_LINK_RX_D0_P
J_LINK_RX_D0_N
J_LINK_RX_CLK_P
J_LINK_RX_CLK_N
J_LINK_TX_CLK_N
J_LINK_TX_CLK_P
FPGA_IRQ
HK_SCL
FPGA_PROG_B
HK_SDA
J_LINK_TX_D0_P
J_LINK_TX_D0_N
J_LINK_RX_D1_P
J_LINK_RX_D1_N
LINK_RX_D0: FPGA -> Kria
LINK_RX_D0_PD
LINK_RX_D0_ND
C101
C102
100n
LINK_RX_CLK: FPGA -> Kria
LINK_RX_CLK_PD
LINK_RX_CLK_ND
C103
C104
LINK_RX_D1: FPGA -> Kria
LINK_RX_D1_PD
LINK_RX_D1_ND
C105
C106
LINK_TX_D0: Kria -> FPGA, terminated here
LINK_TX_D0_P
LINK_TX_D0_N
+1V2
R101
10k
R102
C111
GND
C107
C108
LINK_TX_CLK: Kria -> FPGA, terminated here
LINK_TX_CLK_P
LINK_TX_CLK_N
R103
R104
C112
C109
C110
J102: IA50 (KV260 J7): grounds; every other contact passes to J103 (Rev08).
J102
BH20B(0.8)-34DP
J103
BH20B(0.8)-34DS-0.4V(51)
IA50_P1
IA50_D0_4
IA50_D0_5
IA50_CLK_7
IA50_CLK_8
IA50_D3_10
IA50_D3_11
IA50_PL_1V8
IA50_SCL
IA50_FLASH
IA50_2V75
IA50_TRIGGER
IA50_RESET
IA50_SDA
IA50_PL_1V2
IA50_D2_26
IA50_D2_27
IA50_D1_29
IA50_D1_30
IA50_EXTCLK
IA50_VDD_AF2V8
J103 (Rev08): IA50 camera pass-through receptacle on the top face, contact for contact with J102 (REV08_PLAN 4.3).
Nothing on the adapter uses these nets: the carrier's camera signals and rails pass straight through to an IA5 camera module.
IA5_LINK — how this sheet works
1. Five LVDS pairs to the Kria's HPA bank at 1.2 V: every pair AC-coupled (INTERFACE_SPEC 6.1).
2. Kria -> FPGA pairs: 10k to +1V2 re-bias them: 100 ohm across each pair at the FPGA (R105, R106) terminates them.
3. FPGA -> Kria pairs: terminated and biased inside the SOM (DIFF_TERM_ADV, DQS_BIAS).
4. Pins 26/27 and 29/30 are N before P on the connector and on the carrier alike (3.2).
5. HK_SCL/SDA, FPGA_PROG_B, FPGA_IRQ are the carrier's 1.8 V levels: CONTROL translates.
Kria KV260 IA5 1 High-Speed LVDS & Housekeeping Interface
KV260-IAS2RF
Sheet: /IA5_LINK/
File: IA5_LINK.kicad_sch
Title: IA5_LINK — Hirose IA5 1 link to the Kria, AC coupling, terminations
Size: A3
Date:
Rev: Rev08.1
KiCad E.D.A. 10.0.6
Id: 2/13

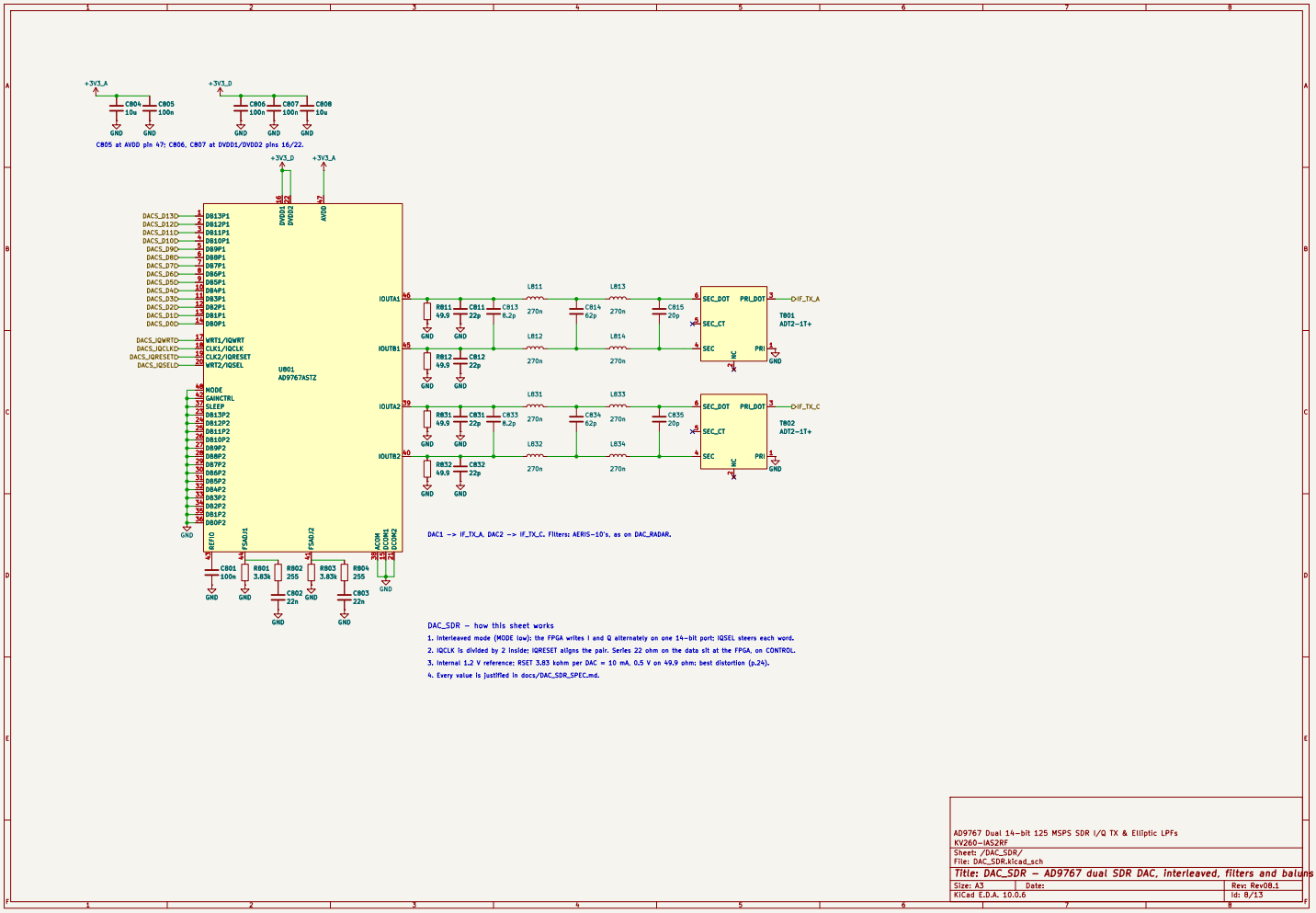


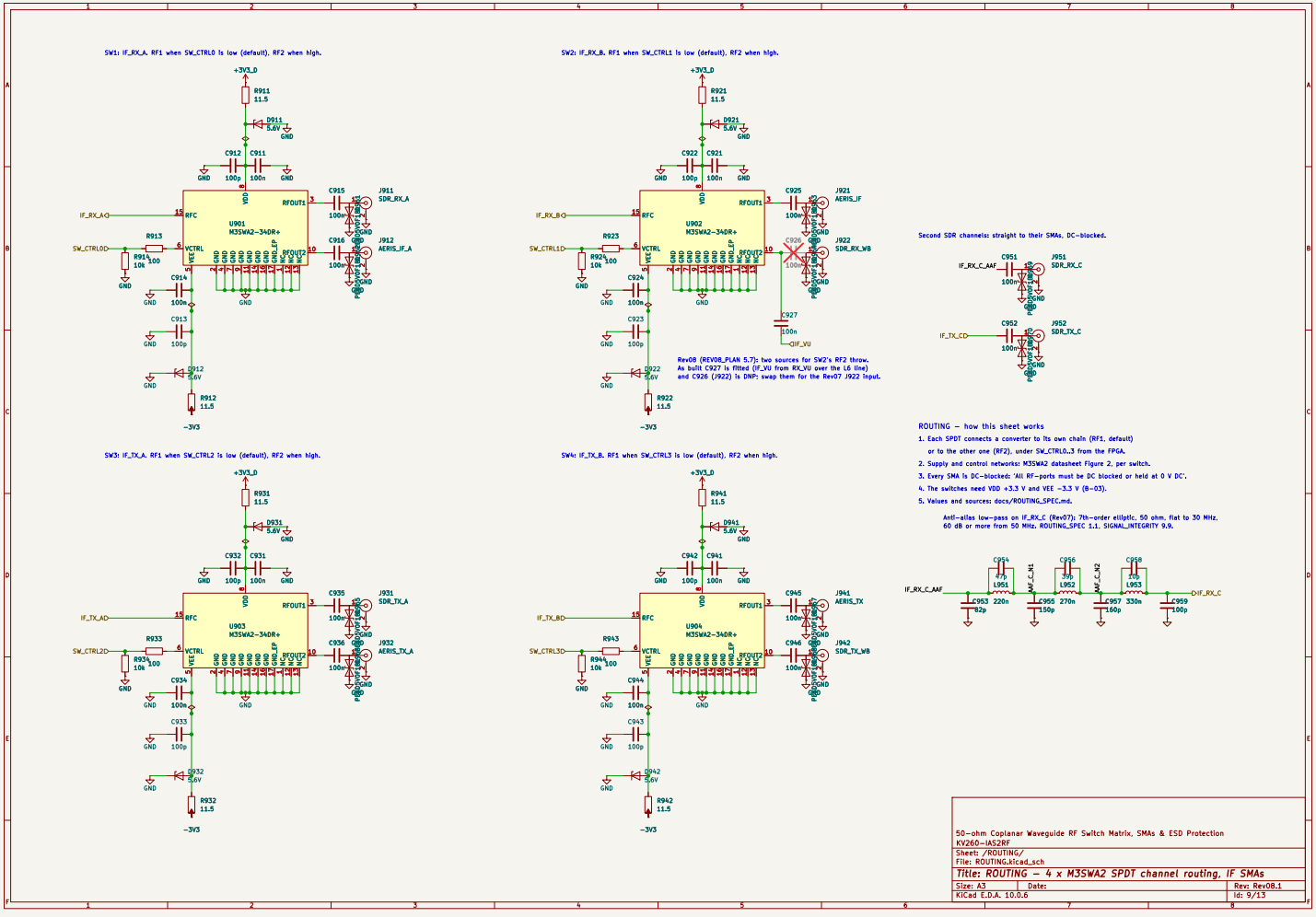

+3V3_D FB401 +3V3_CLK
220R@100MHz
C401 10u
C402 1u
C403 1n
C404 1n
C405 1n
C406 1n
C407 1n
C422 100n
GND
C403–C408: one at each U401 VCC pin (ADCLK948 p.10). C422 at Y401 VDD.
Q0: to the AD9484 (ADC_RADAR)
C414 100p
R404 200
CLK_ADCR_P
C415 100p
R405 200
CLK_ADCR_N
Q1: to the AD9253 (ADC_SDR)
C416 100p
R406 200
CLK_ADCS_P
C417 100p
R407 200
CLK_ADCS_N
Q2: to the XC7A50T (CONTROL)
C418 100p
R408 200
CLK_FPGA_P
C419 100p
R409 200
CLK_FPGA_N
Q3: CLK_OUT SMA
J402
CLK_OUT
C420 100p
R410 200
C421 100p
R411 200
R412 49.9
U401
ADCLK948BCPZ
CLK_REF_JN
CLK_REF_JN: 0.4–3.4 Vpp (ADCLK948 Table 1), 50 ohm on chip.
C412 100n
SI549: order LVPECL, 3.3 V, 5x7 mm, pinout code C. Startup frequency is irrelevant: the FPGA sets 400 or 500 MHz over I2C.
Y401
SI549 LVPECL 3V3 pinout C
R413 4.7k
R414 4.7k
XO_SDA
XO_SCL
R402 130
R403 130
C409 100n
C410 100n
C413 100n
C411 100n
R401 10k
CLK_SEL
CLK_SEL: FPGA open-drain. High/open = CLK1 (SI549), low = CLK0 (SMA).
Receiver side, on the consuming sheet: 100 ohm across each pair (ADCLK948 Figure 17).
CLOCK — how this sheet works
1. One master clock, 400 or 500 MHz, from the SI549 (CLK1, default) or from AERIS-10 via J401 (CLK0).
2. U401 copies it to the AD9484, the AD9253 and the FPGA. The AD9253 divides it internally (1..8).
3. The DAC clocks are NOT here; both DACs take CMOS clocks, which the FPGA generates with their data.
4. Every value on this sheet is justified in docs/CLOCK_SPEC.md.
Low-Jitter SI549 250 MHz XO & ADCLK948 Clock Tree
KV260-IAS2RF
Sheet: /CLOCK/
File: CLOCK.kicad_sch
Title: CLOCK — master XO, reference select, fan-out
Size: A3
Date:
Rev: Rev08.1
KiCad E.D.A. 10.0.6
Id: 4/13

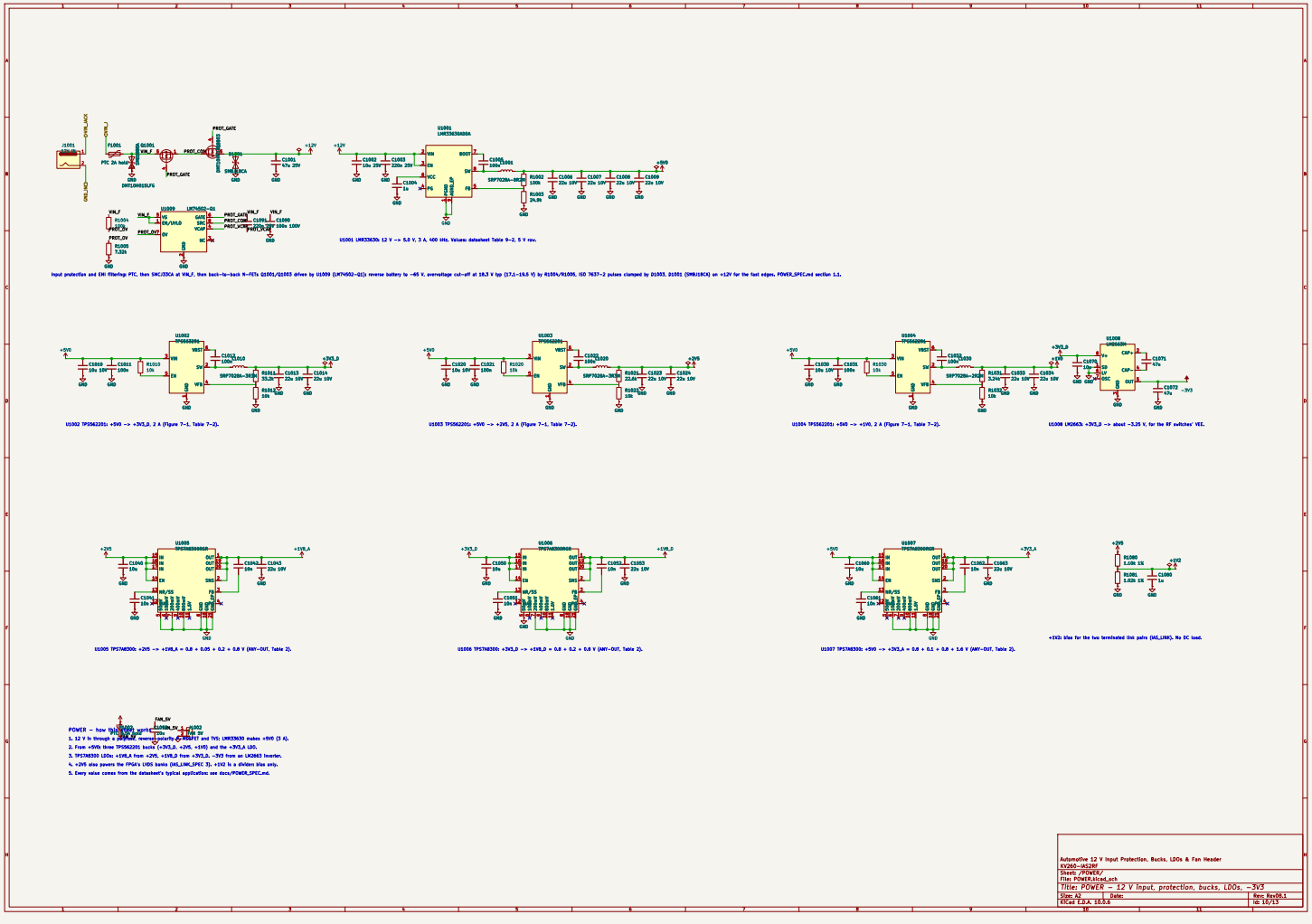

+5V0
FB501
600R@100MHz
+5V_IFR
C520 10u
C505 100n
C506 100n
C514 100n
C515 100n
+1V8_A
FB502
220R@100MHz
+1V8_ADCR_A
C521 10u
C522 100n
C523 100n
C524 100n
C525 100n
C526 100n
C527 100n
C528 100n
C529 100n
C530 100n
C531 100n
C532 100n
+1V8_D
FB503
220R@100MHz
+1V8_ADCR_D
C533 10u
C534 100n
C535 100n
C536 100n
GND
C505/C506: at U502 VCC pins 8/13. C514/C515: at U503 VCC pins 8/13 (AD8352 eval board).
C522–C532: one at each AVDD pin, C534–C536: one at each DRVDD pin (AD9484 eval board).
IF_RX_BD
C501
R501 64.9
R502 200
R504 68
C503 0.6p
R505 4.3k
C502
R503 24.9
C504 100n
U502
AD8352ACPZ
C507 100n
C508 100n
R506 200
R507 200
C509 100n
C510 100n
C511 100n
U502: single-ended in, 15 dB (AD8352 Fig. 26, Table 7)
C512 0.2p
R509 4.3k
R508 115
C513 100n
U503
AD8352ACPZ
C516 100n
C517 100n
R510 200
R511 200
R512 24
R513 24
C519 2.7p
ADCR_VCM
C518 100n
R515 20k
R514 10Ω
CLK_ADCR_PD
CLK_ADCR_ND
CONV_SPI_SDIO
CONV_SPI_SCLK
CONV_SPI_CSB_RD
U503: differential, 10 dB (AD8352 Table 5)
Input network: AD9484 Fig. 30
U501
AD9484BCPZ-500
ADCR_D0_P
ADCR_D0_N
ADCR_D1_P
ADCR_D1_N
ADCR_D2_P
ADCR_D2_N
ADCR_D3_P
ADCR_D3_N
ADCR_D4_P
ADCR_D4_N
ADCR_D5_P
ADCR_D5_N
ADCR_D6_P
ADCR_D6_N
ADCR_D7_P
ADCR_D7_N
ADCR_OR_P
ADCR_OR_N
ADCR_DCO_P
ADCR_DCO_N
To the FPGA: 100 ohm across each pair at the receiver (AD9484 p.16).
ADC_RADAR — how this sheet works
1. The radar IF (120 MHz, AERIS-10) arrives single-ended on IF_RX_B from the routing switch.
2. Two AD8352s give 25 dB, as AERIS-10's two cascaded stages: the first also converts to differential.
3. U501 samples at 400 MSPS (radar) or 500 MSPS (SDR plan): the clock comes from CLOCK, Q0.
4. CONV_SPI_* are 1.8 V signals: AD9484 abs. max DRVDD + 0.2 V. The FPGA must drive them from a 1.8 V bank.
5. Every value on this sheet is justified in docs/ADC_RADAR_SPEC.md.
AD9484 8-bit 400/500 MSPS Radar IF Digitizer & AD8352 Driver
KV260-IAS2RF
Sheet: /ADC_RADAR/
File: ADC_RADAR.kicad_sch
Title: ADC_RADAR — AD9484 radar ADC and its AD8352 drivers
Size: A3
Date:
Rev: RevOB.1
KiCad E.D.A. 10.0.6
Id: 5/13

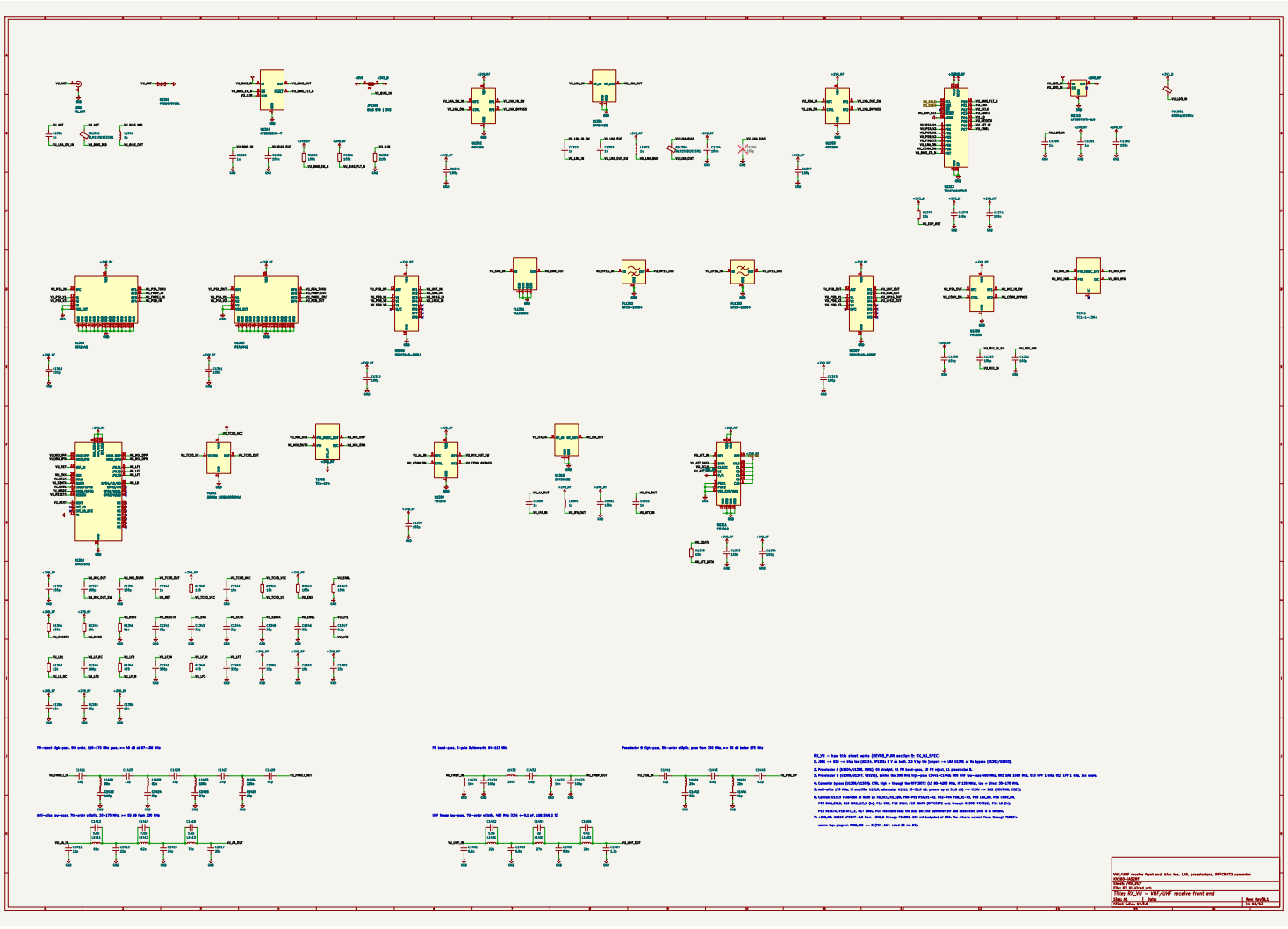

+5V0
FB601
600R@100MHz
+5V_IFS
C660 10u
C661 100n
C662 100n
C663 100n
C664 100n
C661/C662 at U602 VCC 8/13, C663/C664 at U603. C666–C672 one per AVDD pin, C674/C675 one per DRVDD pin.
+1V8_A
FB602
220R@100MHz
+1V8_ADCS_A
C665 10u
C666 100n
C667 100n
C668 100n
C669 100n
C670 100n
C671 100n
C672 100n
+1V8_D
FB603
220R@100MHz
+1V8_ADCS_D
C673 10u
C674 100n
C675 100n
IF_RX_AD
C601
R601 64.9
R602 200
R604 120
C603 0.3p
R605 4.3k
C602
R603 24.9
C604 100n
U602
AD8352ACPZ
C605 100n
C606 100n
R606 200
R607 200
R609 33
R610 33
C607 100n
R608 200
ADCS_VCM
C608 5p
C643 100n
C642 100n
C641 1u
R641 10k 1%
R642 10
CLK_ADCS_PD
CLK_ADCS_ND
CONV_SPI_SDIO
CONV_SPI_SCLK
CONV_SPI_CSB_SD
U601
AD9253BCPZ-125
D0+B
D0-B
D1+B
D1-B
DCO+
DCO-
FCO+
FCO-
D0+A
D0-A
D1+A
D1-A
D0+C
D0-C
D1+C
D1-C
D0+D
D0-D
D1+D
D1-D
ADCS_D0_P
ADCS_D0_N
ADCS_D1_P
ADCS_D1_N
ADCS_DCO_P
ADCS_DCO_N
ADCS_FCO_P
ADCS_FCO_N
Channel A: U602, single-ended in, 12 dB (AD8352 Fig. 26, Table 7)
IF_RX_CD
C621
R621 64.9
R622 200
R624 120
C623 0.3p
R625 4.3k
C622
R623 24.9
C624 100n
U603
AD8352ACPZ
C625 100n
C626 100n
R626 200
R627 200
R629 33
R630 33
C627 100n
R628 200
C628 5p
Channel B: U603, the same
Channels C, D unused: inputs held at VCM
ADC_SDR — how this sheet works
1. Two SDR inputs. IF_RX_A and IF_RX_C, single-ended 50 ohm, each through an AD8352 (12 dB).
2. The AD9253 divides the 500 MHz master clock by 8: 62.5 MSPS, one-lane mode (register 0x21, SPI).
3. One-lane; channel A leaves on D0+−B, channel B on D1+−B (AD9253 Table 8, footnote 1).
4. The inputs are not biased inside the AD9253: centre taps go to its VCM pin through 200 ohm (Fig. 58).
5. CONV_SPI_* are 1.8 V signals (abs. max 2.0 V). LVDS terminated at the FPGA, 100 ohm per pair.
AD9253 Dual 14-bit 125 MSPS SDR I/Q ADC & Front-End Drivers
KV260-IAS2RF
Sheet: /ADC_SDR/
File: ADC_SDR.kicad_sch
Title: ADC_SDR — AD9253 SDR ADC, two channels, AD8352 drivers
Size: A3
Date:
Rev: RevOB.1
KiCad E.D.A. 10.0.6
Id: 6/13

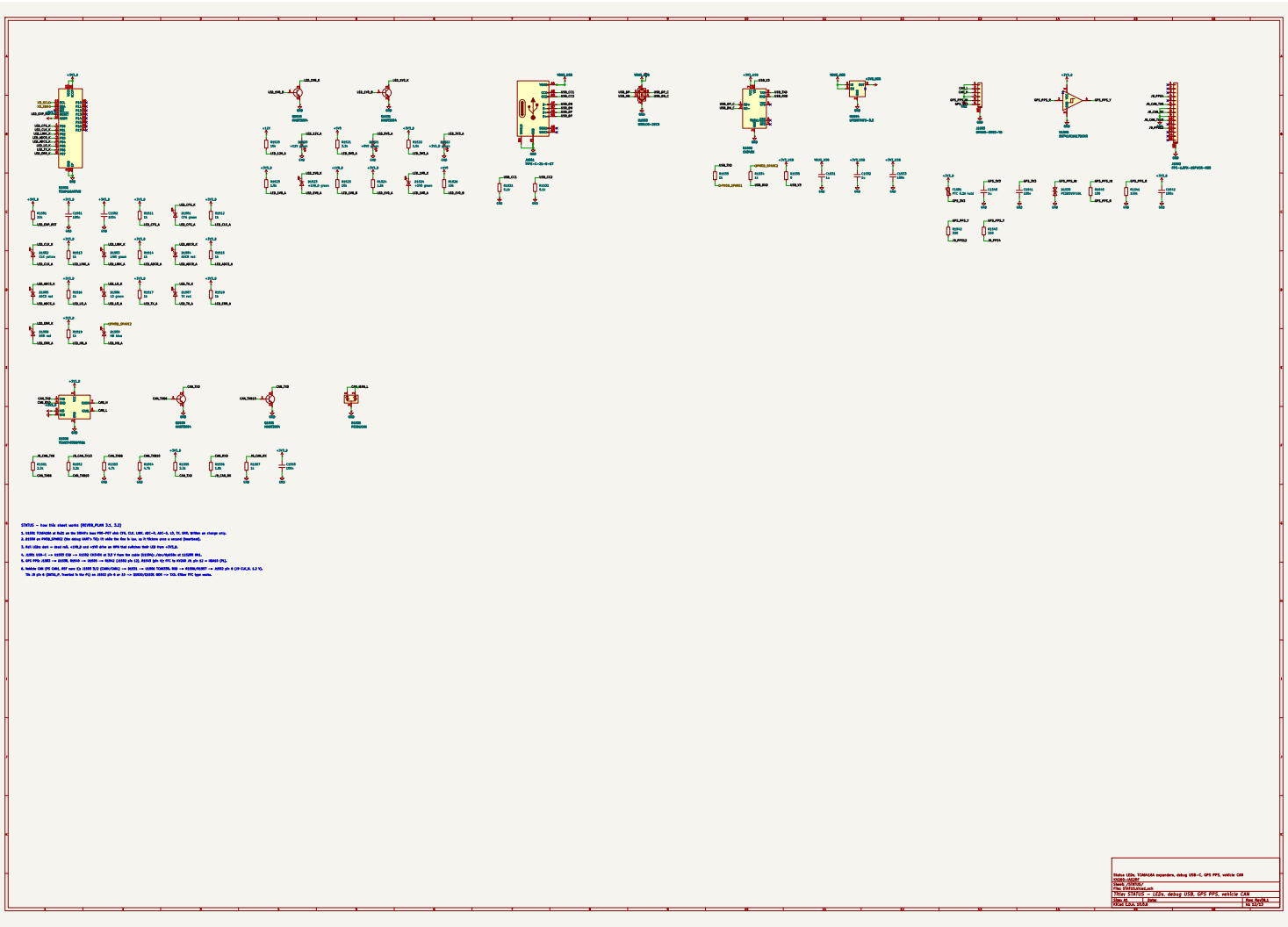

+3V3_A
C702
10u
C703
100n
GND
GND
+3V3_D
C704
100n
GND
+3V3_A is the analogue LDO; no extra filter (AD9708 figure 22 is for a shared supply).
+3V3_D
+3V3_A
C701
100n
DVDD
AVDD
COMP1
DACR_D7D
DACR_D6D
DACR_D5D
DACR_D4D
DACR_D3D
DACR_D2D
DACR_D1D
DACR_D0D
DACR_CLKD
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
CLOCK
SLEEP
NC
U701
AD9708AR
IOUTA
IOUTB
REFIO
FS_ADJ
COMP2
REFLO
ACOM
R702
49.9
R703
49.9
C707
22p
C708
22p
C709
8.2p
L701
270n
L702
270n
L703
270n
L704
270n
C710
62p
C711
20p
SEC_DOT
PRI_DOT
SEC_CT
SEC
PRI
NC
IF_TX_B
T701
ADT2-1T+
C705
100n
R701
1.91k 1%
C706
100n
Reconstruction filter: AERIS-10's, as designed (107.3 nH, 32.8/106/22 pF).
DAC_RADAR — how this sheet works
1. The FPGA sends 8-bit samples and their clock (3.3 V CMOS); series 22 ohm slt at the FPGA end. on CONTROL.
2. Internal 1.2 V reference (REFLO to ACOM). RSET 1.91 kohm: 20 mA full scale. AERIS-10 differs here. see the spec.
3. 50 ohm loads, then AERIS-10's differential LC reconstruction filter, then a 2:1 balun to 50 ohm single-ended.
4. Every value is justified in docs/DAC_RADAR_SPEC.md.
AD9708 8-bit 160 MSPS Radar LFM Chirp TX & 7th-Order Elliptic LPF
KV260-IAS2RF
Sheet: /DAC_RADAR/
File: DAC_RADAR.kicad_sch
Title: DAC_RADAR — AD9708 radar chirp DAC, reconstruction filter, balun
Size: A3
Date:
Rev: RevOB.1
KiCad E.D.A. 10.0.6
Id: 7/13

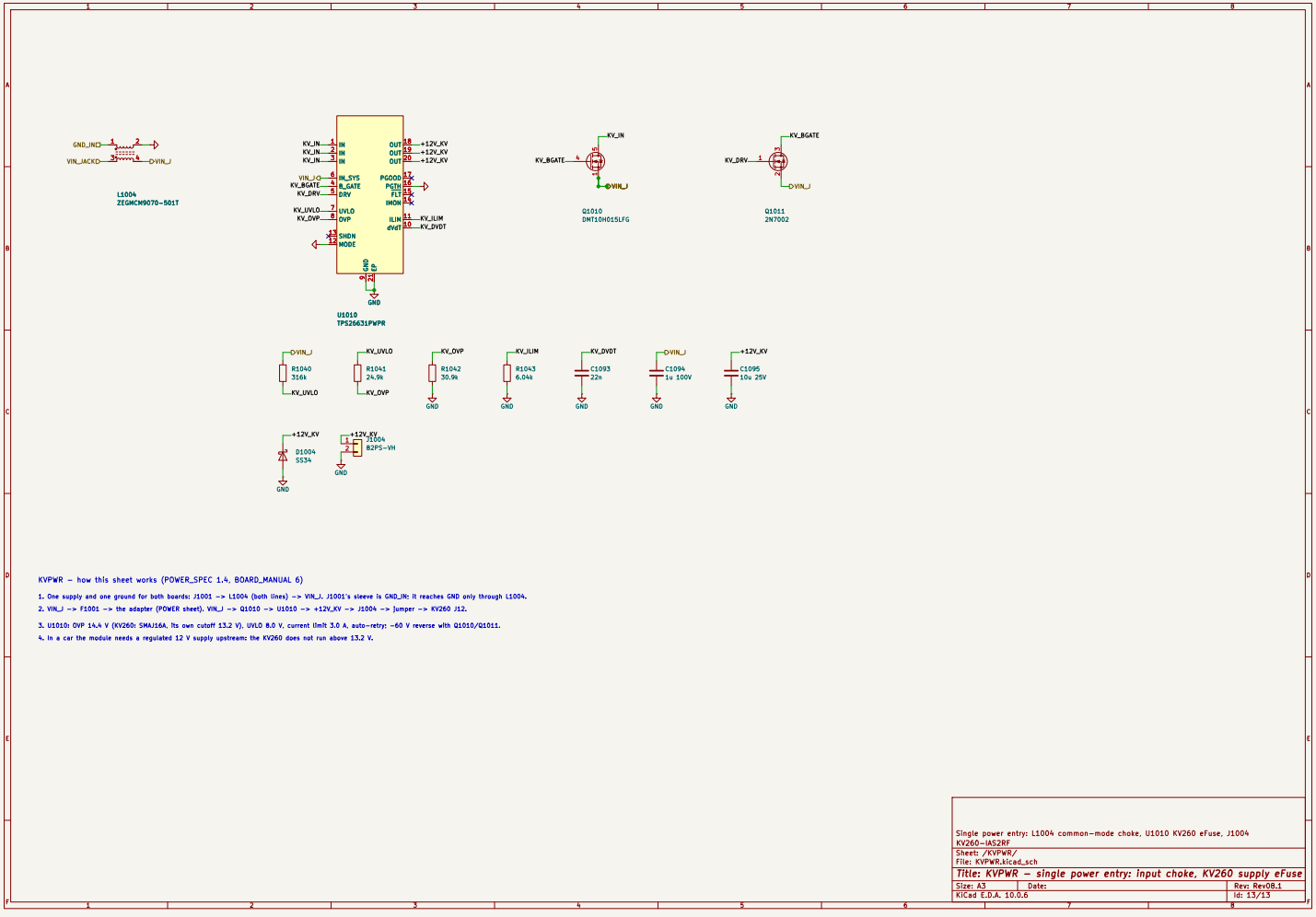

+3V3_A
+3V3_D
C804 10u
C805 100n
C806 100n
C807 100n
C808 10u
C805 at AVDD pin 47; C806, C807 at DVDD1/DVDD2 pins 16/22.
UB01
AD9767ASTZ
DACS_D13
DACS_D12
DACS_D11
DACS_D10
DACS_D9
DACS_D8
DACS_D7
DACS_D6
DACS_D5
DACS_D4
DACS_D3
DACS_D2
DACS_D1
DACS_D0
DACS_IQWRT
DACS_IQCLK
DACS_IQRESET
DACS_IQSEL
IOUTA1
IOUTB1
IOUTA2
IOUTB2
R811 49.9
R812 49.9
R831 49.9
R832 49.9
C811 22p
C812 22p
C831 22p
C832 22p
C813 8.2p
C833 8.2p
C814 62p
C834 62p
C815 20p
C835 20p
L811 270n
L812 270n
L813 270n
L814 270n
L831 270n
L832 270n
L833 270n
L834 270n
T801
ADT2-1T+
T802
ADT2-1T+
SEC_DOT
PRI_DOT
SEC_CT
SEC
PRI
IF_TX_A
IF_TX_C
DAC1 -> IF_TX_A. DAC2 -> IF_TX_C. Filters: AERIS-10's, as on DAC_RADAR.
C801 100n
R801 3.83k
R802 255
R803 3.83k
R804 255
C802 22n
C803 22n
DAC_SDR — how this sheet works
1. Interleaved mode (MODE low): the FPGA writes I and Q alternately on one 14-bit port; IQSEL steers each word.
2. IQCLK is divided by 2 inside; IQRESET aligns the pair. Series 22 ohm on the data slt at the FPGA, on CONTROL.
3. Internal 1.2 V reference; RSET 3.83 kohm per DAC = 10 mA. 0.5 V on 49.9 ohm: best distortion (p.24).
4. Every value is justified in docs/DAC_SDR_SPEC.md.
AD9767 Dual 14-bit 125 MSPS SDR I/Q TX & Elliptic LPFs
KV260-IAS2RF
Sheet: /DAC_SDR/
File: DAC_SDR.kicad_sch
Title: DAC_SDR — AD9767 dual SDR DAC, interleaved, filters and baluns
Size: A3
Date:
Rev: RevOB.1
KiCad E.D.A. 10.0.6
Id: 8/13


SW1: IF_RX_A. RF1 when SW_CTRL0 is low (default), RF2 when high.
SW2: IF_RX_B. RF1 when SW_CTRL1 is low (default), RF2 when high.
SW3: IF_TX_A. RF1 when SW_CTRL2 is low (default), RF2 when high.
SW4: IF_TX_B. RF1 when SW_CTRL3 is low (default), RF2 when high.
U901 M3SWA2-34DR+
U902 M3SWA2-34DR+
U903 M3SWA2-34DR+
U904 M3SWA2-34DR+
+3V3_D
-3V3
GND
IF_RX_A
IF_RX_B
IF_TX_A
IF_TX_B
SW_CTRL0
SW_CTRL1
SW_CTRL2
SW_CTRL3
J911 SDR_RX_A
J912 AERIS_IF_A
J921 AERIS_IF
J922 SDR_RX_WB
J931 SDR_TX_A
J932 AERIS_TX_A
J941 AERIS_TX
J942 SDR_TX_WB
IF_VU
Rev08 (REV08_PLAN 5.7): two sources for SW2's RF2 throw.
As built C927 is fitted (IF_VU from RX_VU over the L6 line)
and C926 (J922) is DNP; swap them for the Rev07 J922 input.
Second SDR channels: straight to their SMAs. DC-blocked.
IF_RX_C_AAF
IF_TX_CD
J951 SDR_RX_C
J952 SDR_TX_C
ROUTING — how this sheet works
1. Each SPDT connects a converter to its own chain (RF1, default)
or to the other one (RF2), under SW_CTRL0..3 from the FPGA.
2. Supply and control networks: M3SWA2 datasheet Figure 2, per switch.
3. Every SMA is DC-blocked: 'All RF-ports must be DC blocked or held at 0 V DC'.
4. The switches need VDD +3.3 V and VEE −3.3 V (B-03).
5. Values and sources: docs/ROUTING_SPEC.md.
Anti-alias low-pass on IF_RX_C (Rev07): 7th-order elliptic, 50 ohm, flat to 30 MHz,
60 dB or more from 50 MHz. ROUTING_SPEC 1.1, SIGNAL_INTEGRITY 9.9.
IF_RX_C_AAF
IF_RX_C
L951 220n
L952 270n
L953 330n
82p
150p
160p
100p
50-ohm Coplanar Waveguide RF Switch Matrix, SMAs & ESD Protection
KV260-IAS2RF
Sheet: /ROUTING/
File: ROUTING.kicad_sch
Title: ROUTING — 4 x M3SWA2 SPDT channel routing, IF SMAs
Size: A3
Date:
Rev: Rev08.1
KiCad E.D.A. 10.0.6
Id: 9/13


Input protection and EMI filtering: PTC, then SMCJ33CA at VIN_F, then back-to-back N-FETs Q1001/Q1003 driven by U1009 (LM74502-Q1): reverse battery to −65 V, overvoltage cut-off at 18.3 V typ (17.1–19.5 V) by R1004/R1005. ISO 7637-2 pulses clamped by D1003. D1001 (SMBJ18CA) on +12V for the fast edges. POWER_SPEC.md section 1.1.
U1001 LMR33630: 12 V -> 5.0 V, 3 A, 400 kHz. Values: datasheet Table 9-2, 5 V row.
U1002 TPS562201: +5V0 -> +3V3_D, 2 A (Figure 7-1, Table 7-2).
U1003 TPS562201: +5V0 -> +2V5, 2 A (Figure 7-1, Table 7-2).
U1004 TPS562201: +5V0 -> +1V0, 2 A (Figure 7-1, Table 7-2).
U1008 LM2663: +3V3_D -> about −3.25 V, for the RF switches' VEE.
U1005 TPS74K300: +2V5 -> +1V8_A = 0.8 + 0.05 + 0.2 + 0.8 V (ANY-OUT, Table 2).
U1006 TPS74K300: +3V3_D -> +1V8_D = 0.8 + 0.2 + 0.8 V (ANY-OUT, Table 2).
U1007 TPS74K300: +5V0 -> +3V3_A = 0.8 + 0.1 + 0.8 + 1.6 V (ANY-OUT, Table 2).
+1V2: bias for the two terminated link pairs (MC_LINK), No DC load.
POWER — how this board is powered
1. 12 V in through a 30 A blade connector and TVS: LMR33630 makes +5V0 (3 A).
2. From +5V0: three TPS562201 bucks (+3V3_D, +2V5, +1V0) and the +3V3_A LDO.
3. TPS74K300 LDOs: +1V8_A from +2V5, +1V8_D from +3V3_D, −3V3 from an LM2663 inverter.
4. +2V5 also powers the FPGA's LVDS banks (MC_LINK_SPEC 3). +1V2 is a divider bias only.
5. Every value comes from the datasheet's typical application; see docs/POWER_SPEC.md.
Automotive 12 V Input Protection, Bucks, LDOs & Fan Header
KV260-IAS2RF
Sheets /POWER/
Files POWER.kicad_sch
Title: POWER — 12 V Input, protection, bucks, LDOs, −3V3
Size: A2 Date: Rev: Rev08.1
KiCad E.D.A. 10.0.0 Id: 15/15



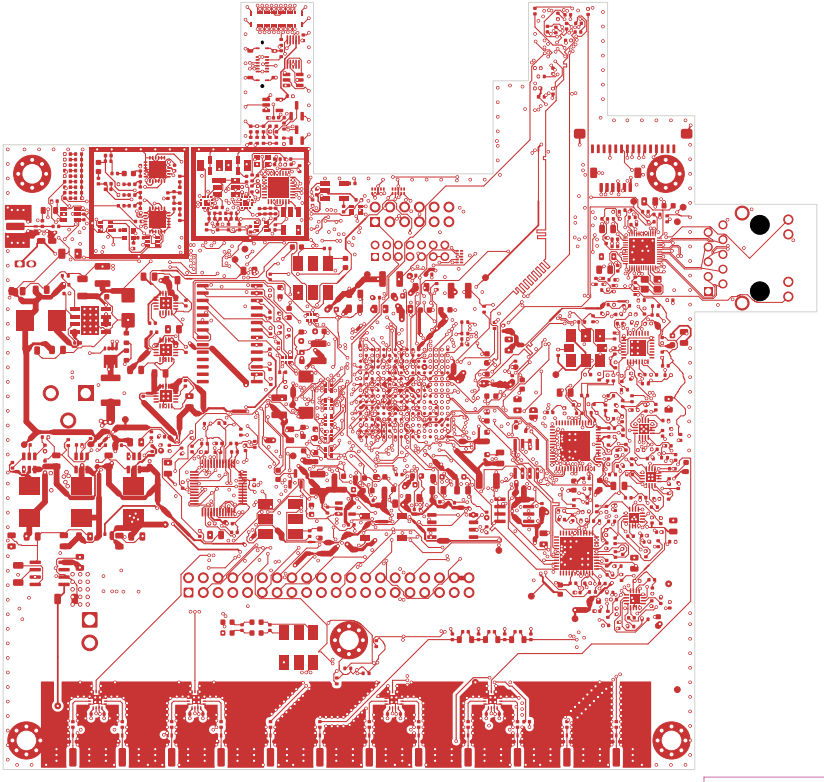

STATUS — how this sheet works (REVB8_PLAN 3.1, 3.2)
1. U1201 TCA9548A at 0x72 on the SDA/SCL bus PB6–PB7 after CFG, CLK, LRC, ADC-A, ADC-B, LD, TP, GND, 100nm on change etc.
2. D1202 on PB30_GPADC2 (for debug SAFE: TP2: 0 while the flow is low, as TI failure over a second (heartbeat).
3. Ref LEDs: dual red, +3V3_D and +3V3 after an RPU that indicates that LED from +3V3_D.
4. U1201 USB-C → U1202 USB → U1203 CP2102 at 3.3 V from the cable D1201, Vbus/Vbat/Vbus at U1204 PB1.
5. GPS PPS: J1201 → U1205, R1910 → U1205 → PB2N2 (J1202 pin 12), R1910 (pin 4) PPS to PC2 in U1205 J5, pin 12 → GND5 (%).
6. Vehicle CAN (P1 CAN, RSP core J1 J1202 5/2 (CAN/CAN) → U1201 → U1206 TCAN330, RSD → U1205/U1207 → J1202 pin 9 (J9 CAN_L) 1/2 %.
TP: J9 pin 6 (3V3_F, headed to the P1) at J1202 pin 6 at J9 → U1201/U1205 RSD → TCA. Other PC type units.
Vehicle CAN, TCAN1044 expanders, debug USB-C, GPS PPS, vehicle CAN
Sheet: 13/14
File: KV260_IAS2RF.kicad_sch
Title: STATUS — LEDs, debug USB, GPS PPS, vehicle CAN
Size: A1
Rev: Rev B.1
KiCad 8.0.4


GND_IN
VIN_JACK
VIN_J
L1004
ZEGMCM9070-501T
KV_IN
KV_BGATE
KV_DRV
KV_UVLO
KV_OVP
VIN_J
IN_SYS
G_GATE
DRV
UVLO
OVP
SHDN
MODE
OUT
PGOOD
PGTH
FLT
IMON
ILIM
dVdT
+12V_KV
KV_ILIM
KV_DVDT
GND
U1010
TPS26631PWPR
Q1010
DMT10H015LFG
Q1011
2N7002
R1040
316k
R1041
24.9k
R1042
30.9k
R1043
6.04k
C1093
22n
C1094
1u 100V
C1095
10u 25V
D1004
SS34
J1004
B2PS-VH
KVPWR — how this sheet works (POWER_SPEC 1.4, BOARD_MANUAL 6)
1. One supply and one ground for both boards: J1001 -> L1004 (both lines) -> VIN_J. J1001's sleeve is GND_IN: it reaches GND only through L1004.
2. VIN_J -> F1001 -> the adapter (POWER sheet). VIN_J -> Q1010 -> U1010 -> +12V_KV -> J1004 -> jumper -> KV260 J12.
3. U1010: OVP 14.4 V (KV260: SMAJ16A, its own cutoff 13.2 V). UVLO 8.0 V, current limit 3.0 A, auto-retry: ~60 V reverse with Q1010/Q1011.
4. In a car the module needs a regulated 12 V supply upstream: the KV260 does not run above 13.2 V.
Single power entry: L1004 common-mode choke, U1010 KV260 eFuse, J1004
KV260-IAS2RF
Sheet: /KVPWR/
File: KVPWR.kicad_sch
Title: KVPWR — single power entry: input choke, KV260 supply eFuse
Size: A3
Date:
Rev: Rev08.1
KiCad E.D.A. 10.0.6
Id: 13/13

Appendix D: 8-Layer PCB Layout (JLC08161H-2116C)

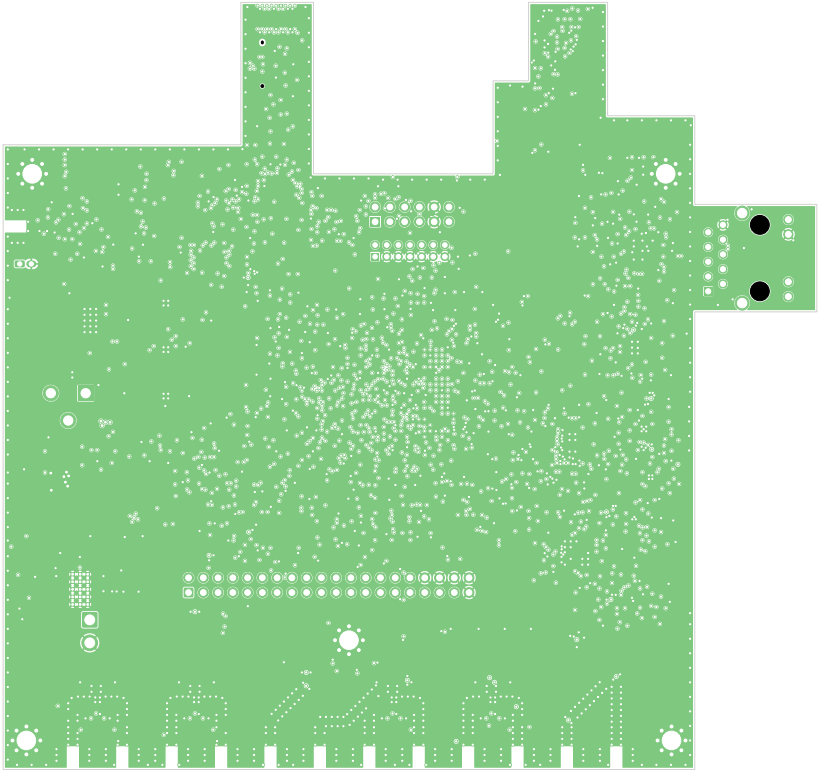
L1..L8 individual copper layers, all 8 layers combined & transparent signal routing (vector)

Page 1/10 | L1 SIG · F.Cu (RF microstrip to the SMAs, BGA fan-out, LVDS pairs) JLC08161H-2116C | outer 1 oz | 0.119 mm to L2 GND



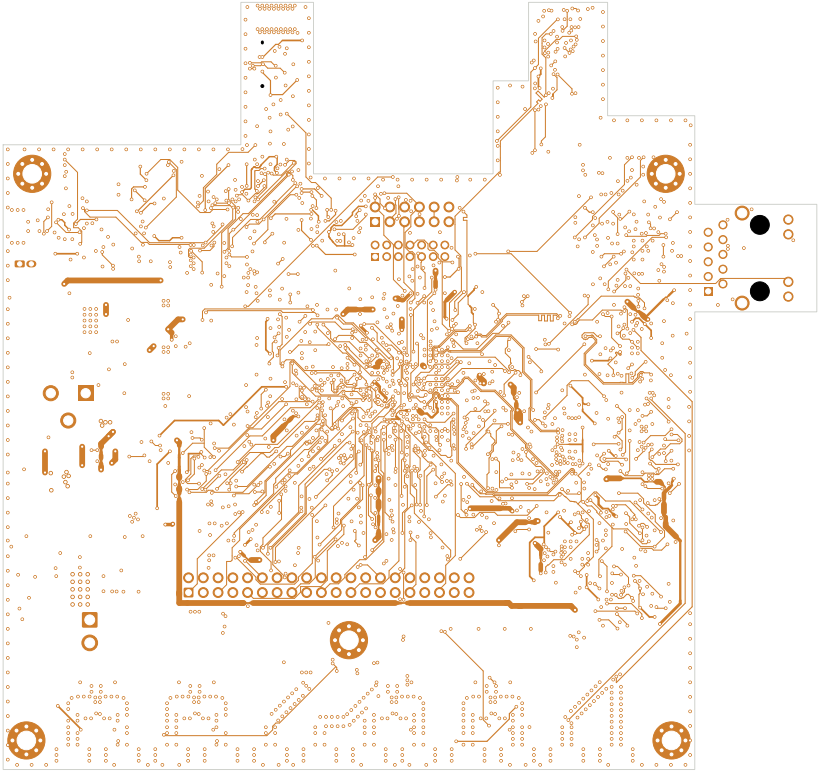
8-Layer RF/Radar/SDR Front-End for Kria KV260 (Apache-2.0)
KV260-IAS2RF
Sheet:
File: KV260-IAS2RF.kicad_pcb
Title: KV260-IAS2RF
Size: A3 | Date: | Rev: Rev08.1
KiCad E.D.A. 10.0.6 | Id: 1/1

Page 2/10 | L2 GND · In1.Cu (solid reference for L1 and L3) 0.5 oz inner Cu



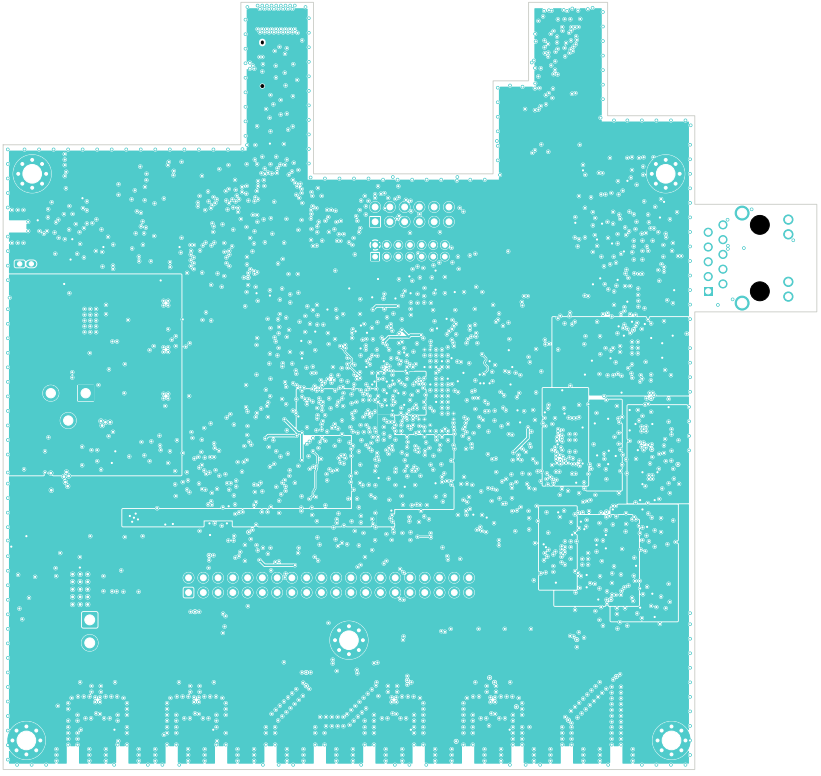
8-Layer RF/Radar/SDR Front-End for Kria KV260 (Apache-2.0)
KV260-IAS2RF
Sheet:
File: KV260-IAS2RF.kicad_pcb
Title: KV260-IAS2RF
Size: A3 | Date: | Rev: Rev08.1
KiCad E.D.A. 10.0.6 | Id: 1/1

Page 3/10 | L3 SIG · In2.Cu (DAC buses, radar ADC LVDS, SPI and switch control, supply fingers) 0.5 oz | 0.13 mm to L2 GND, 0.37 mm to L4



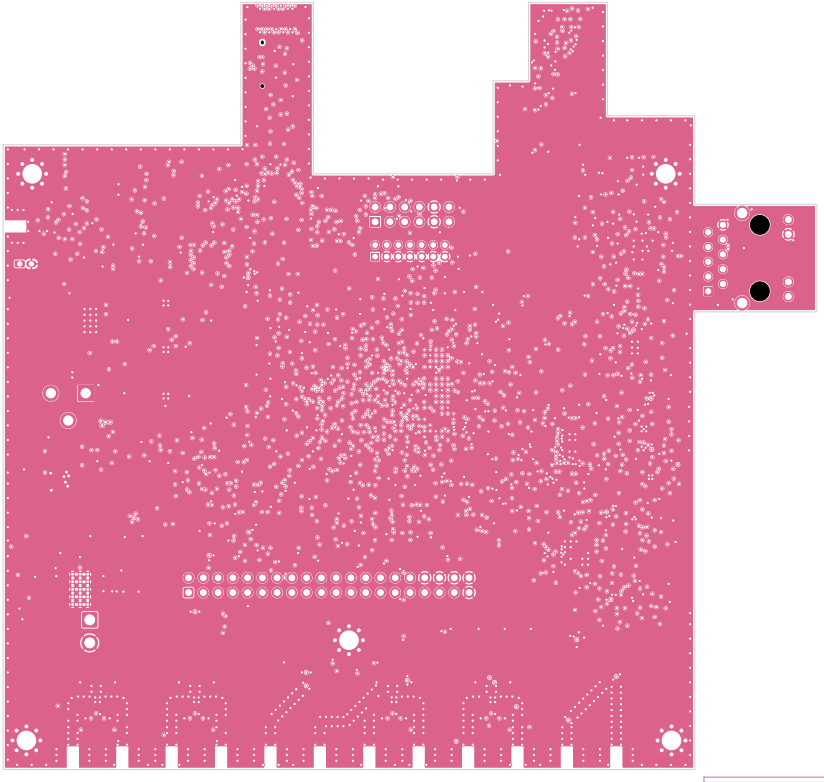
8-Layer RF/Radar/SDR Front-End for Kria KV260 (Apache-2.0)
KV260-IAS2RF
Sheet:
File: KV260-IAS2RF.kicad_pcb
Title: KV260-IAS2RF
Size: A3 | Date: | Rev: Rev08.1
KiCad E.D.A. 10.0.6 | Id: 1/1

Page 4/10 | L4 PWR · In3.Cu (split planes: +3V3_D, +1V, +1V8_D) 0.5 oz inner Cu



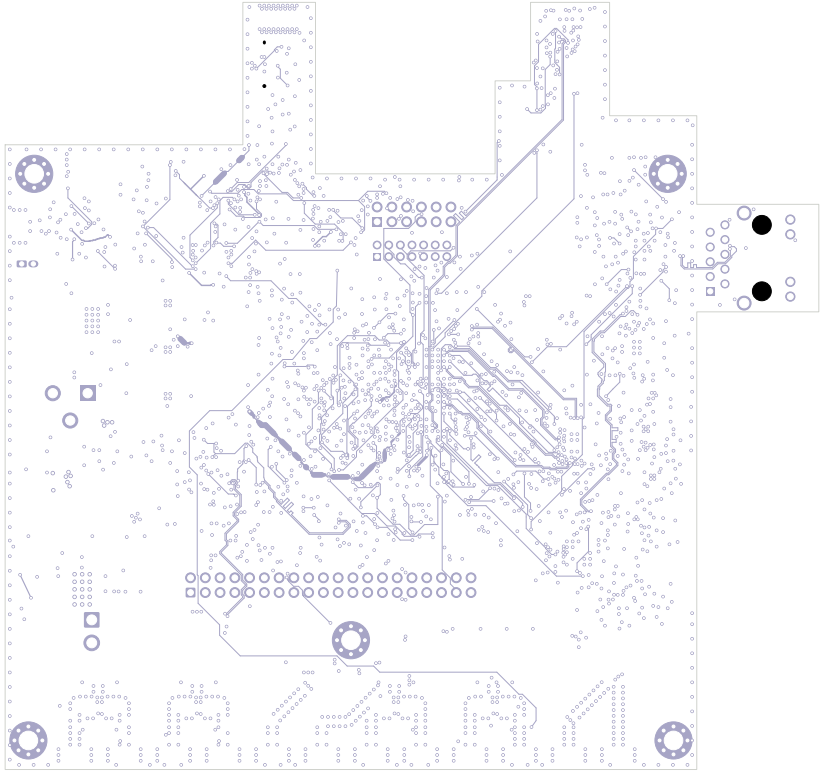
8-Layer RF/Radar/SDR Front-End for Kria KV260 (Apache-2.0)
KV260-IAS2RF
Sheet:
File: KV260-IAS2RF.kicad_pcb
Title: KV260-IAS2RF
Size: A3 | Date: | Rev: Rev08.1
KiCad E.D.A. 10.0.6 | Id: 1/1

Page 5/10 | L5 GND · In4.Cu (solid reference for L6) 0.5 oz inner Cu



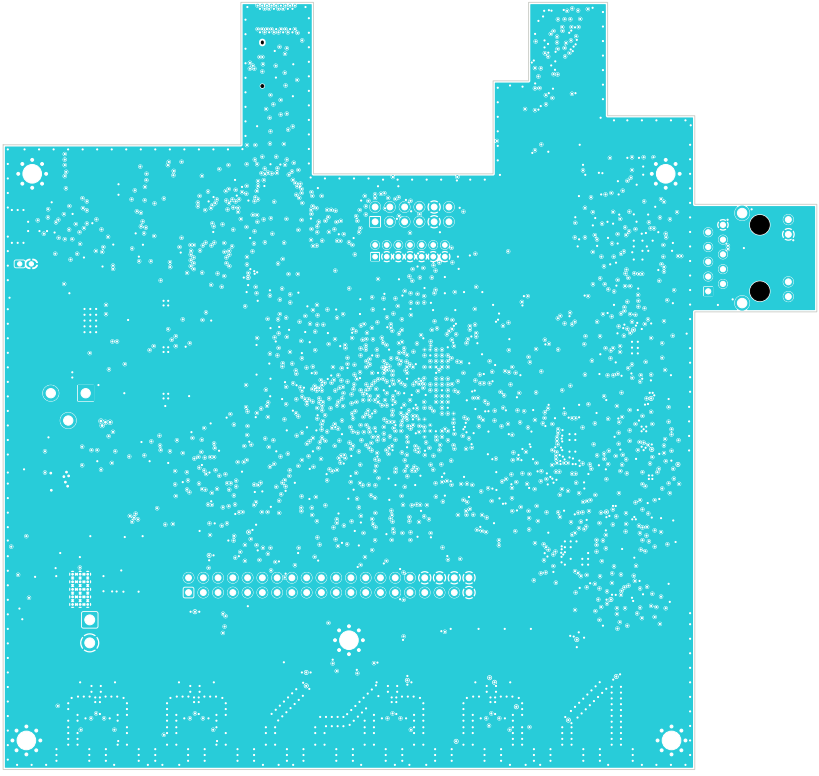
8-Layer RF/Radar/SDR Front-End for Kria KV260 (Apache-2.0)
KV260-IAS2RF
Sheet:
File: KV260-IAS2RF.kicad_pcb
Title: KV260-IAS2RF
Size: A3 | Date: | Rev: Rev08.1
KiCad E.D.A. 10.0.6 | Id: 1/1

Page 6/10 | L6 SIG · In5.Cu (ADC LVDS and clocks, LINK_RX_CLK, SGMII TX, flash, I2C) 0.5 oz | 0.13 mm to L7 GND, 0.37 mm to L5 GND



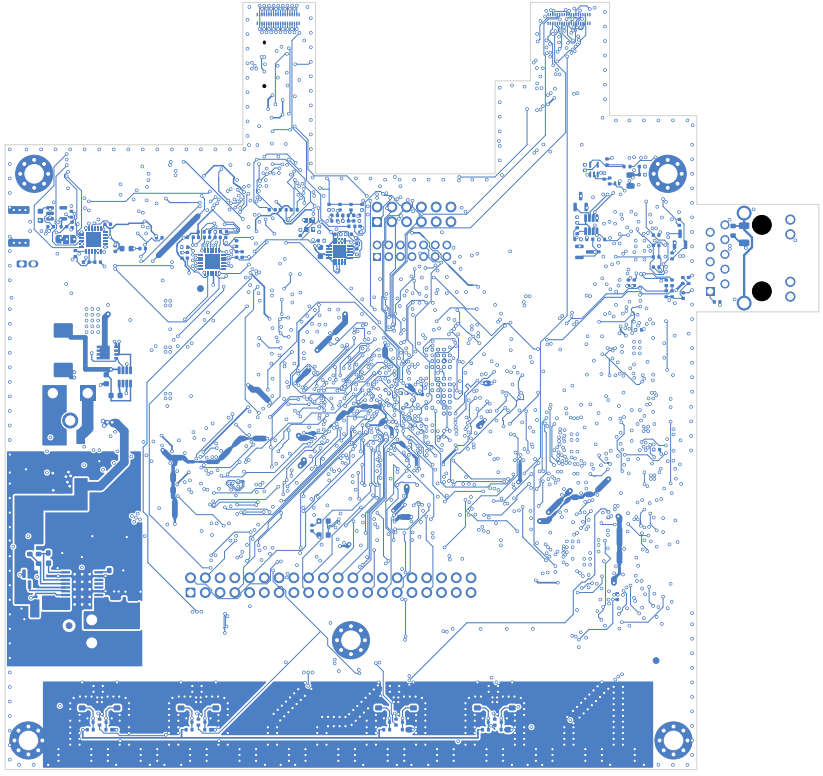
8-Layer RF/Radar/SDR Front-End for Kria KV260 (Apache-2.0)
KV260-IAS2RF
Sheet:
File: KV260-IAS2RF.kicad_pcb
Title: KV260-IAS2RF
Size: A3 | Date: | Rev: Rev08.1
KiCad E.D.A. 10.0.6 | Id: 1/1

Page 7/10 | L7 GND · In6.Cu (solid reference for L6 and L8) 0.5 oz inner Cu



8-Layer RF/Radar/SDR Front-End for Kria KV260 (Apache-2.0)
KV260-IAS2RF
Sheet:
File: KV260-IAS2RF.kicad_pcb
Title: KV260-IAS2RF
Size: A3 | Date: | Rev: Rev08.1
KiCad E.D.A. 10.0.6 | Id: 1/1

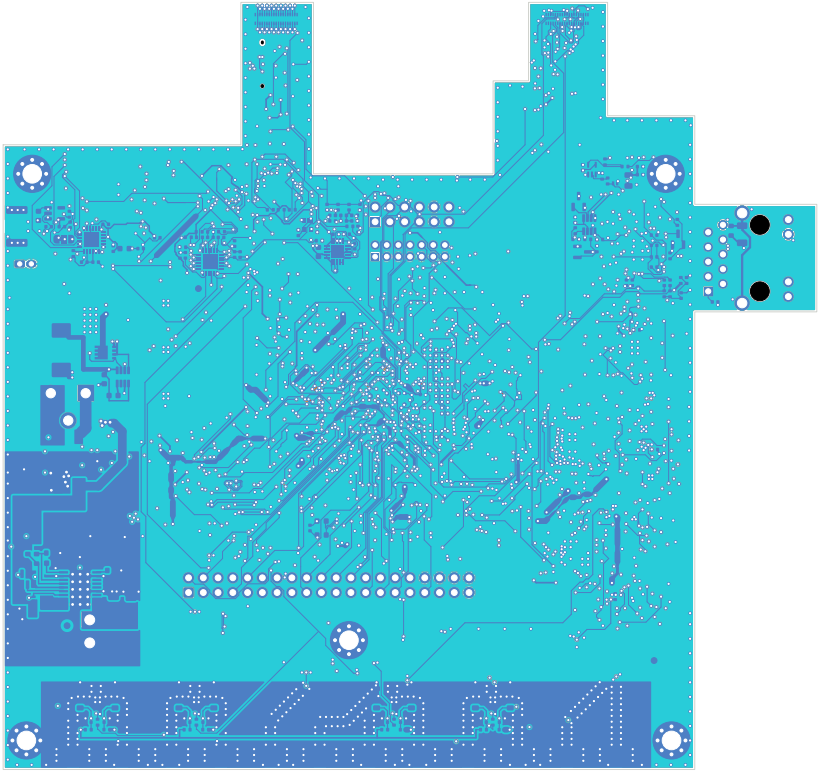
Page 8/10 | L8 SIG · B.Cu (BGA decoupling, fan-out, LVDS pairs) outer 1 oz | 0.119 mm to L7 GND | 1.6 mm board



8-Layer RF/Radar/SDR Front-End for Kria KV260 (Apache-2.0)
KV260-IAS2RF
Sheet:
File: KV260-IAS2RF.kicad_pcb
Title: KV260-IAS2RF
Size: A3 | Date: | Rev: Rev08.1
KiCad E.D.A. 10.0.6 | Id: 1/1

Page 9/10 | All 8 Copper Layers Combined (L1·L8 Stacked + Board Outline)

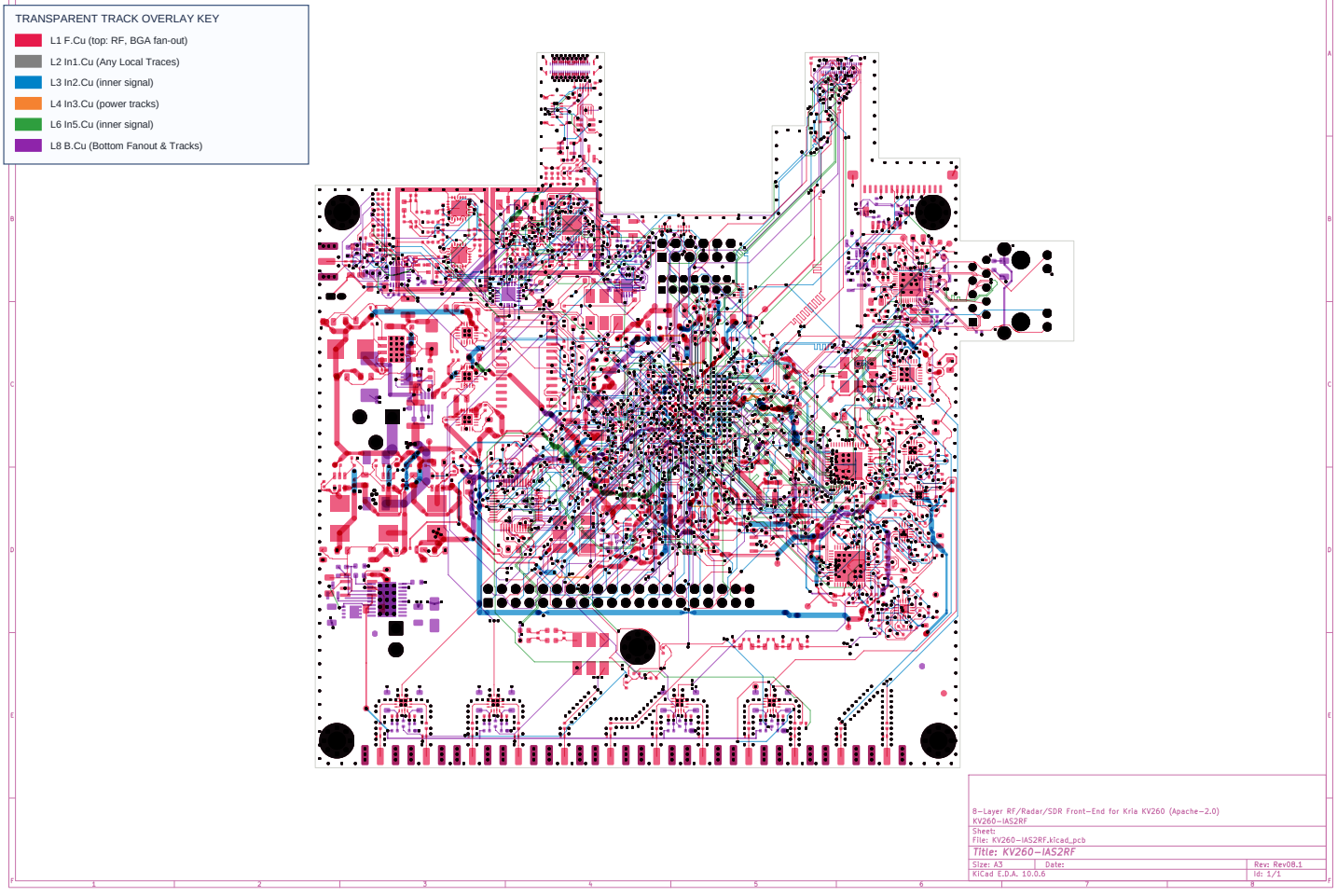
Complete 8-Layer Composite | Includes GND & Power Planes



8-Layer RF/Radar/SDR Front-End for Kria KV260 (Apache-2.0)
KV260-IAS2RF
Sheet:
File: KV260-IAS2RF.kicad_pcb
Title: KV260-IAS2RF
Size: A3 | Date: | Rev: Rev08.1
KiCad E.D.A. 10.0.6 | Id: 1/1

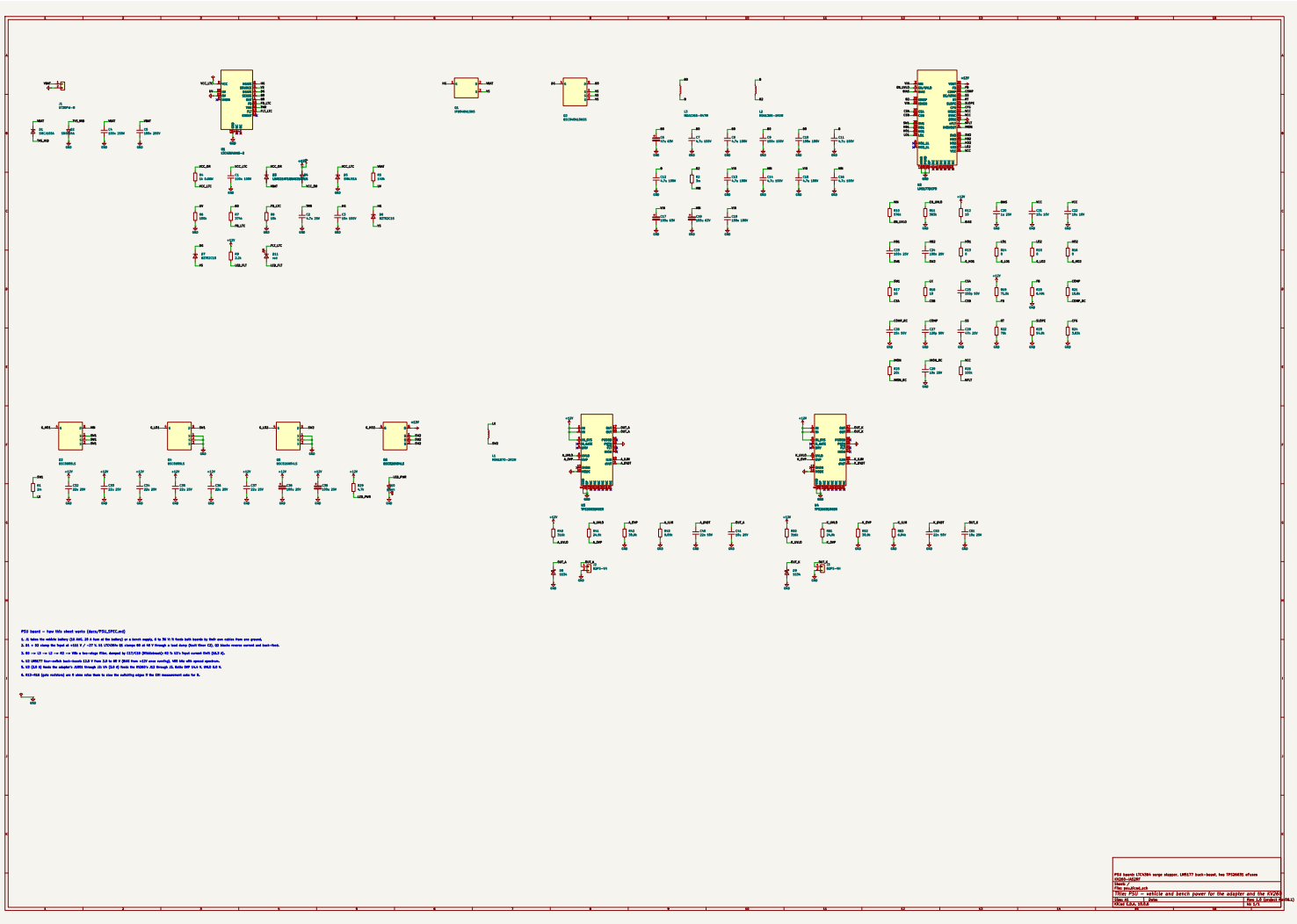
Page 10/10 | All Signal Tracks Combined · Transparent Multi-Layer View (GND L2/L5/L7 & Power L4 Planes Removed)

100% Vector Multiply-Blend Overlay | Signal & Power Traces Only



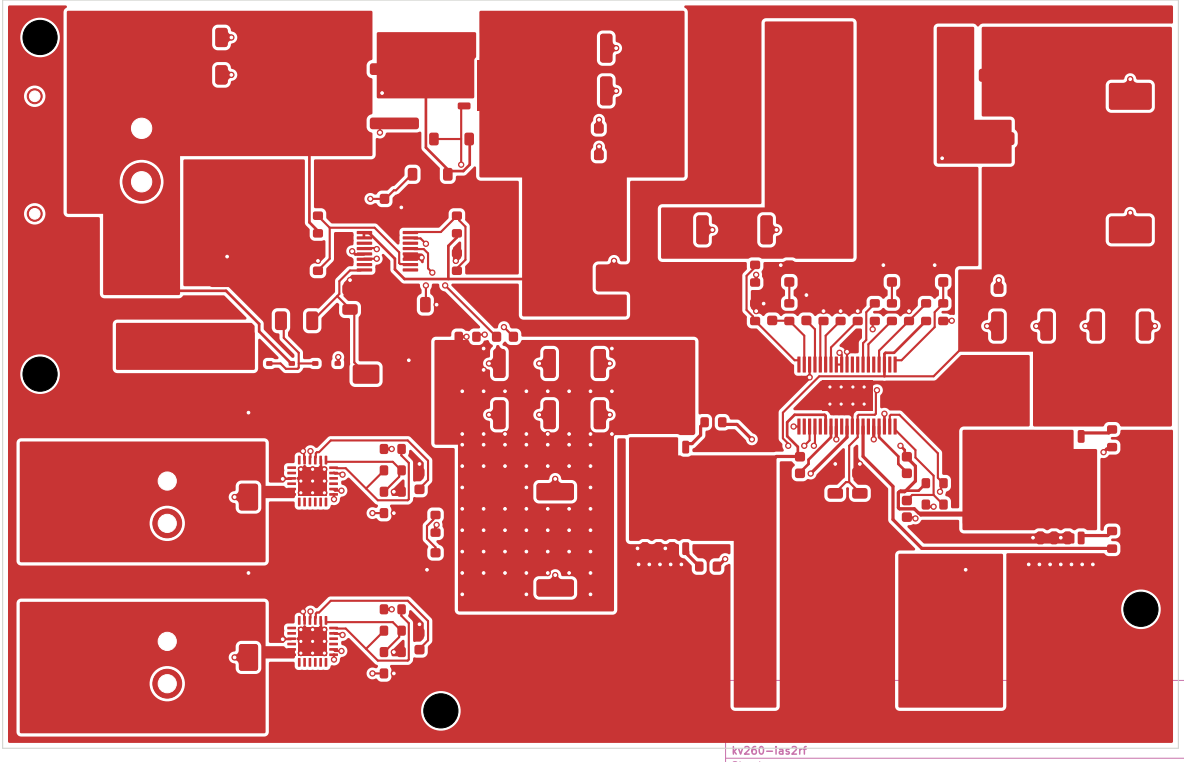
Appendix E: PSU Board Schematic & Layout

The vehicle supply for both boards: LTC4364 surge stopper, LM5177 buck-boost, two TPS26631; schematic and f



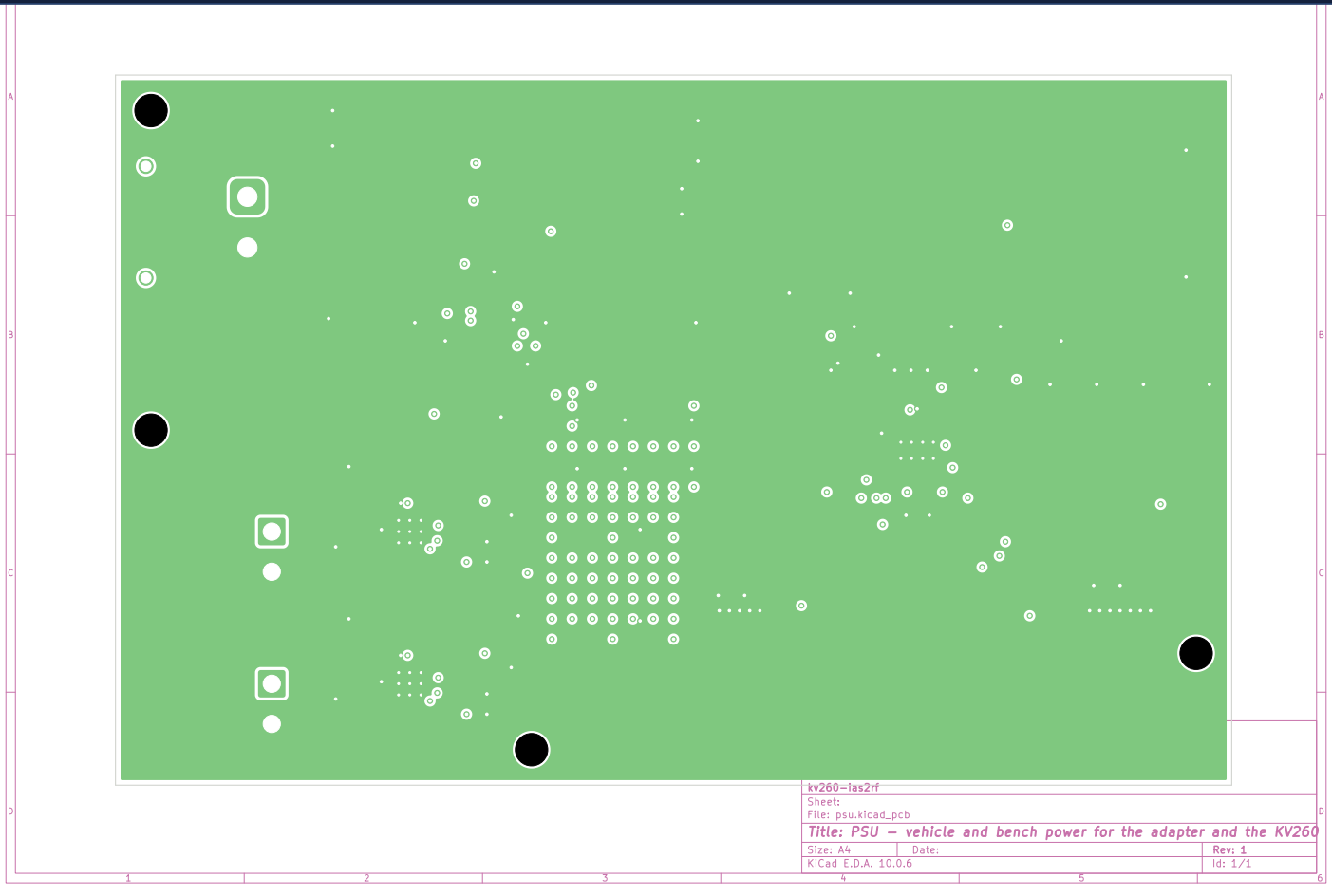
Page 1/5 | PSU L1 - F.Cu (parts, power pours: VBAT, VS, switch nodes, +12V)

2 oz outer Cu | 0.21 mm to L2 GND



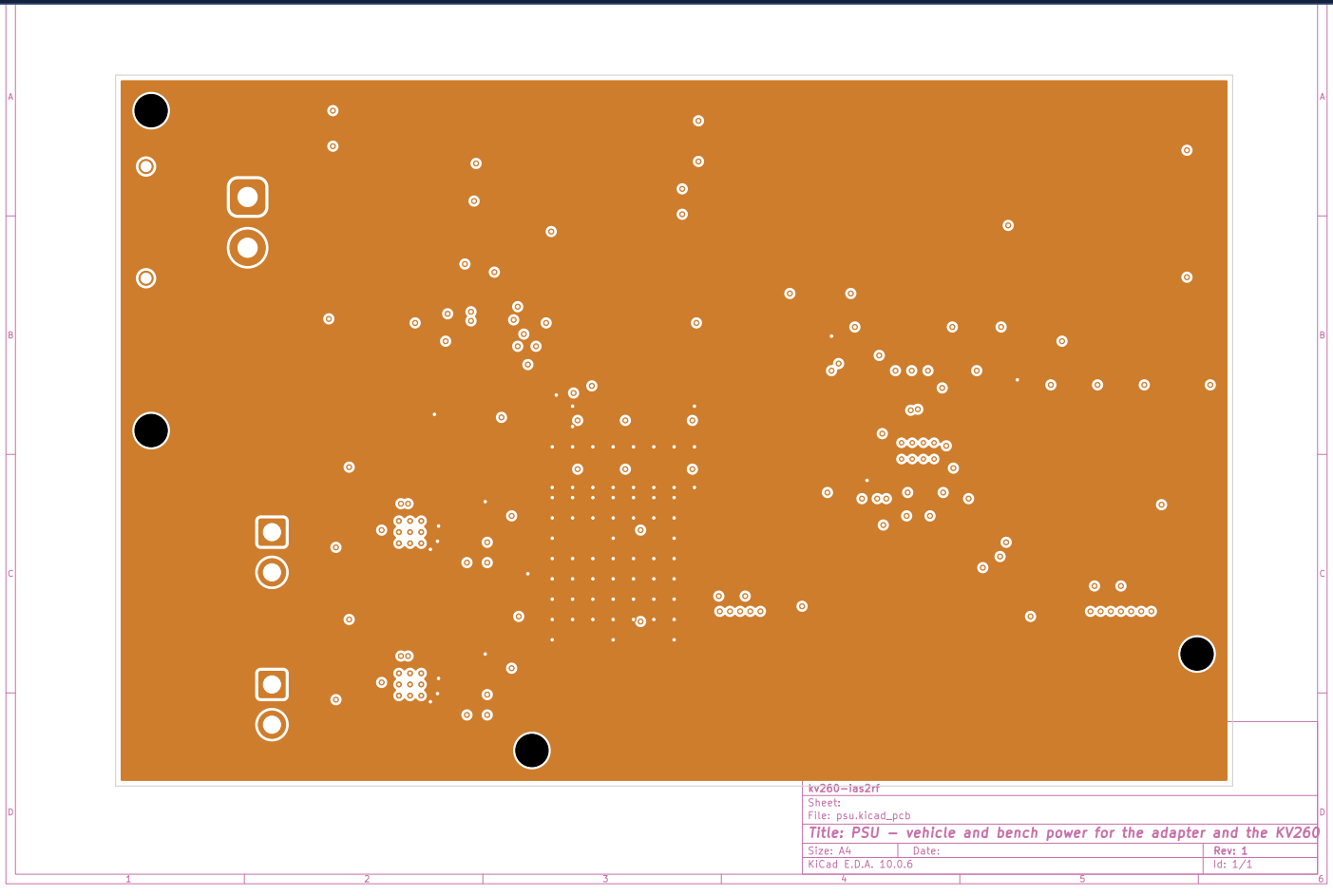
Page 2/5 | PSU L2 - In1.Cu (solid ground under the power stage)

0.5 oz inner Cu



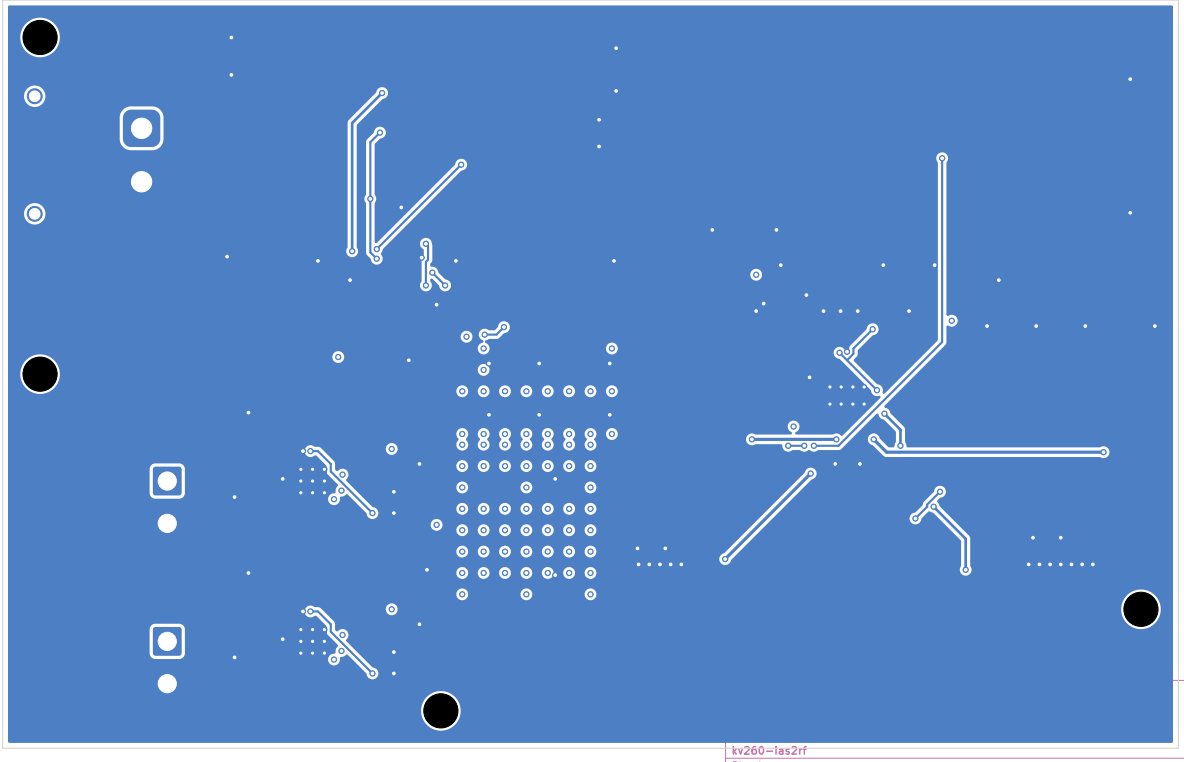
Page 3/5 | PSU L3 - In2.Cu (+12V output plane to J2 and J3)

0.5 oz inner Cu | 1.07 mm core to L2



Page 4/5 | PSU L4 - B.Cu (ground pour and short signal runs)

2 oz outer Cu | 1.6 mm board



Page 5/5 | PSU - All 4 Copper Layers, Translucent Overlay

Multiply blend | vector

